Power model update of Final Pixel Chip

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OUTLINE

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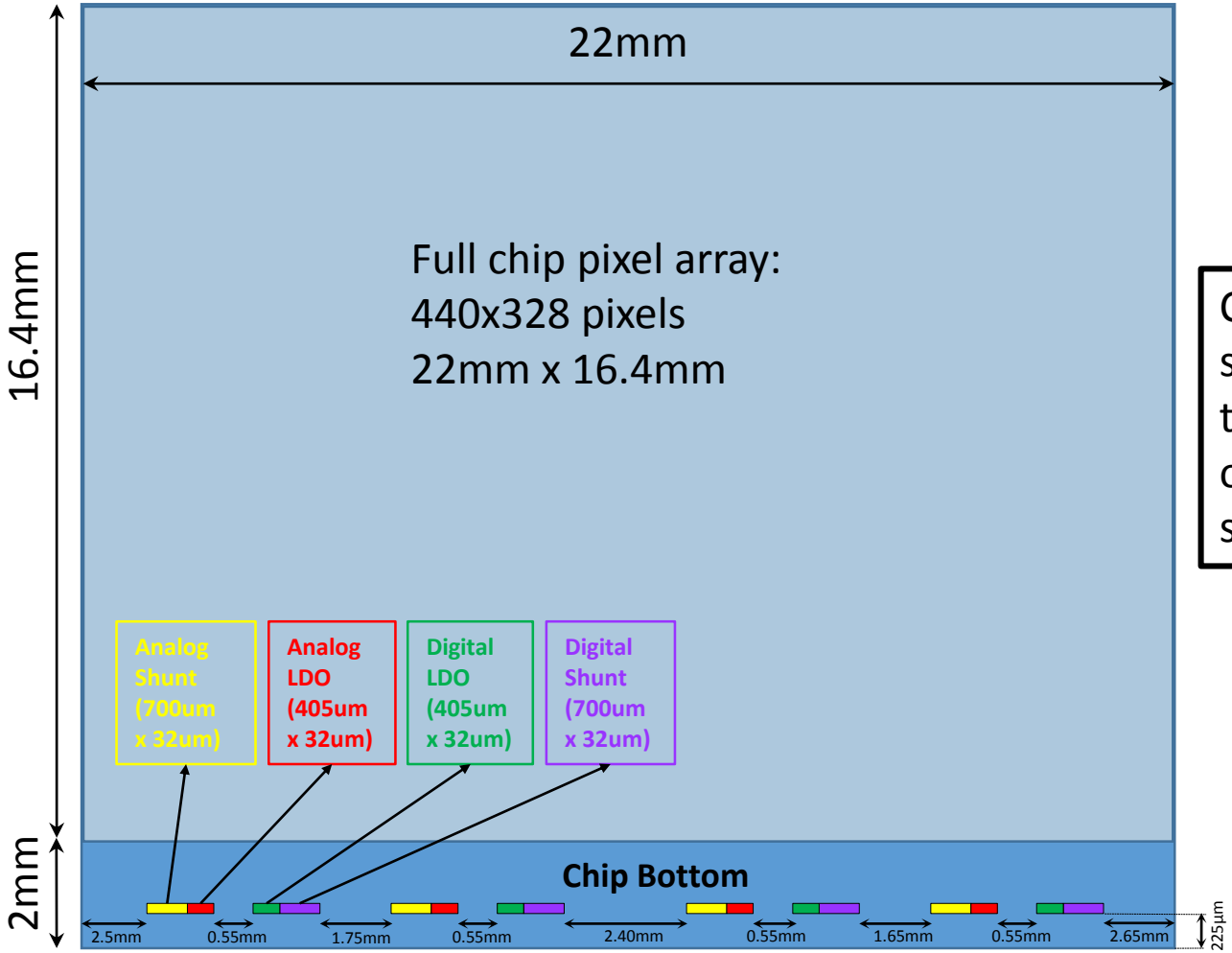
1.1 Power model description



Analog and Digital shuntLDOs interleaved

CMS phase 2 chip simplified layout for thermal model, based on TDR and RD53A submitted floorplan

1.1 Power model description

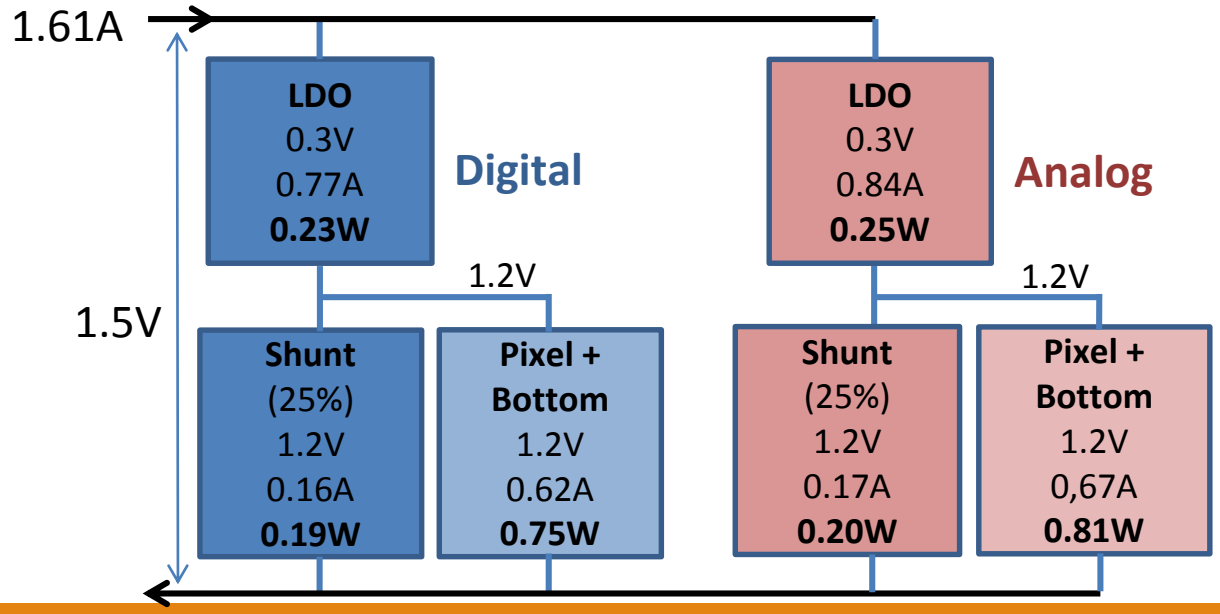
- Pixel array: 440x328 pixels + chip bottom (22mm x 18.4mm) -> **for thermal studies consider uniform the sum of analog and digital power along the entire surface of the chip**
- Shunt-LDOs at bottom of chip interleaved analog/digital (see scheme).
  Each shunt-LDO is split into 4 blocks to improve power dissipation
  - Analog shunt-LDO: 4 blocks of 0.5A = Max 2A
  - Digital shunt-LDO: 4 blocks of 0.5A = Max 2A
  - Shunt blocks (NMOS): 700um x 32um (yellow/red)
  - LDO blocks (PMOS): 405um x 32um (green/purple)
- Power is dissipated in thin top layer of Silicon
- Pixel chip thickness: ~100um
- Heat removal from back side of pixel chip

1.1 Power model description

- Nominal chip consumption of CMS final chip (update from F. Loddo & S. Marconi):

Element	Opt	Nom	Cons
Per pixel analog	3.1 µA	3.6 µA	4.2 µA
Per pixel digital	3.1 µA	3.6 µA	4.2 µA
Analog Chip bottom	130 mA	150 mA	180 mA
Digital Chip bottom	70 mA	100 mA	150 mA
TOTAL 440x328 chip	**1.10 A**	**1.30 A**	**1.54 A**
+10% SLDO headroom (to be tested)	1.21 A	1.43 A	1.70 A
+25% SHUNT-LDO Headroom	**1.38 A**	**1.61 A**	**1.93 A**

- Typical power consumption for a hit rate of 3Ghz/cm2 and 1MHz trigger rate (~inner layer activity).
- Assumption: pixel current equally shared between analog and digital -> Actual ratio depends on FE (TBD)
- 10% headroom case has to be tested (tolerances + overcurrent protection issues)



Total power (opt):
1.5V x 1.38A= 2.07W

-15%

Total power (nom):
1.5V x 1.61A= 2.42W

+20%

Total power (cons):
1.5V x 1.93A= 2.90W

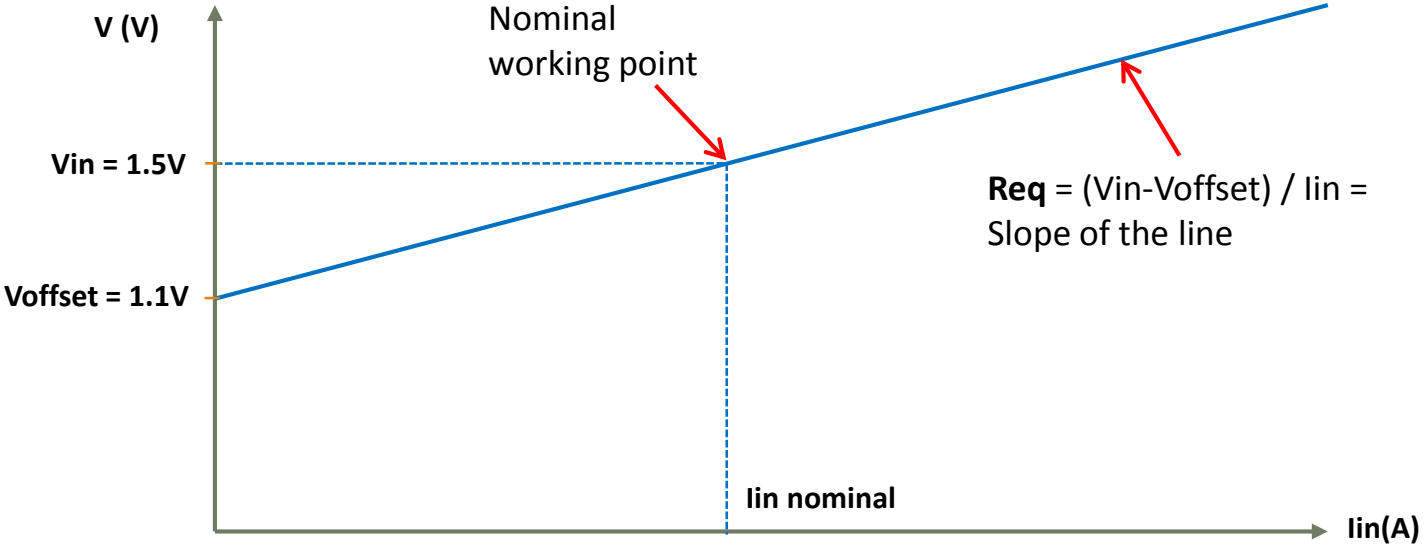
1.1 Power model description

Shunt-LDO configuration:

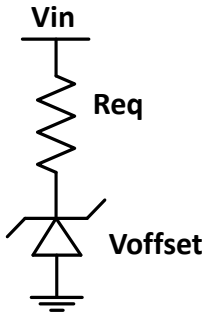
- **Nominal Vin = 1.5V** (it has been increased from previous 1.4V to get more margin for LDO to work properly) -> Final value to be discussed
- **Voffset = 1.1V** (increased from previous 1.0V to keep the same V-I slope)
- **25% of shunted current (nominal head-room) (possibility of lower values is under study)**
- Req adapted to get always the nominal working point of Vin = 1.5V
  - Analog shuntLDO -> Req = 0.55Ω/0.48Ω/0.41Ω
  - Digital shuntLDO -> Req = 0.62Ω/0.51Ω/0.42Ω
  - **Total chip -> Req = 0.29Ω/0.25Ω/0.21Ω**

Adapted for opt/nom/cons cases
Consumption scenarios

- **LDOs output voltage = 1.2V**



SLDO input equivalent circuit:



1.2 Working modes power distribution

Cases of study for thermal analysis:

1- ALL THE MODULES IN NORMAL CASE

2- ALL THE MODULES IN NO LOAD CASE (mis-configuration)

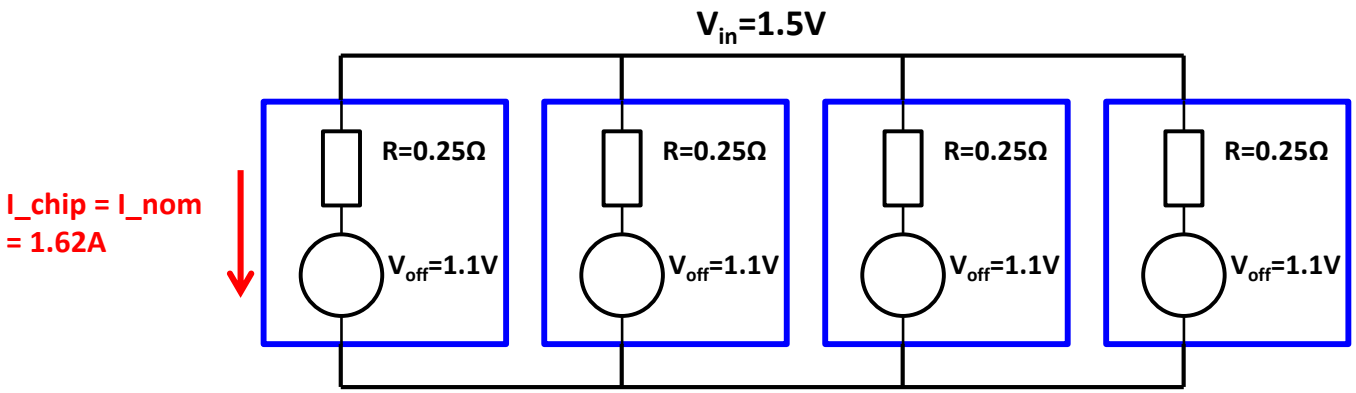
3- ONLY ONE 4chips MODULE FAILURE AND THE REST IN NORMAL CASE

4- ONLY ONE 2chips MODULE FAILURE AND THE REST IN NORMAL CASE

- Nominal power consumption has been used in all cases
- To get the power dissipated in the other 2 scenarios:
  - Optimum = Nominal – 15%
  - Conservative = Nominal + 20%

1.2 Working modes power distribution

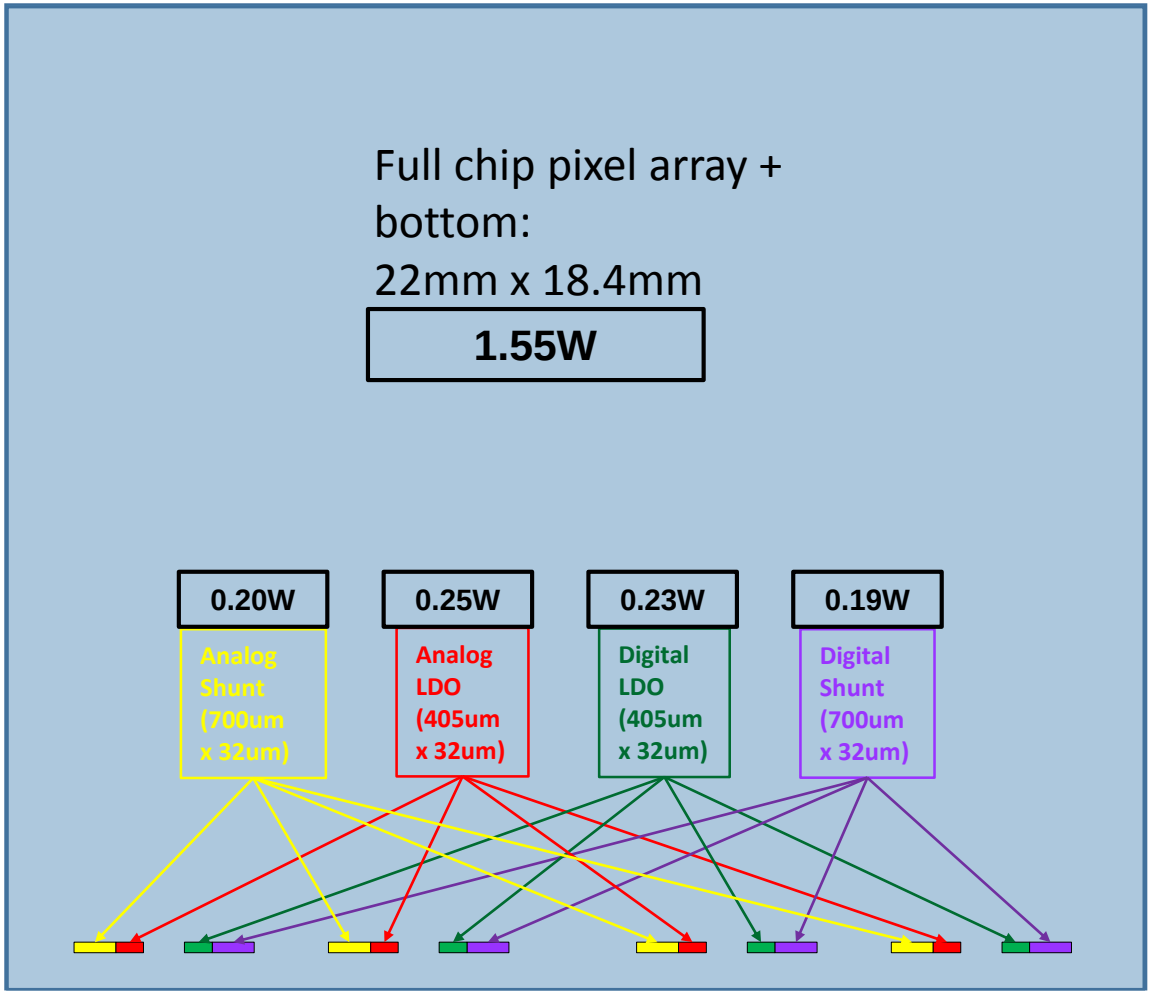
4 CHIP MODULE
NOMINAL CASE



*R=X.XXΩ (eq. resistance for nominal chip consumption)

1.2 Working modes power distribution

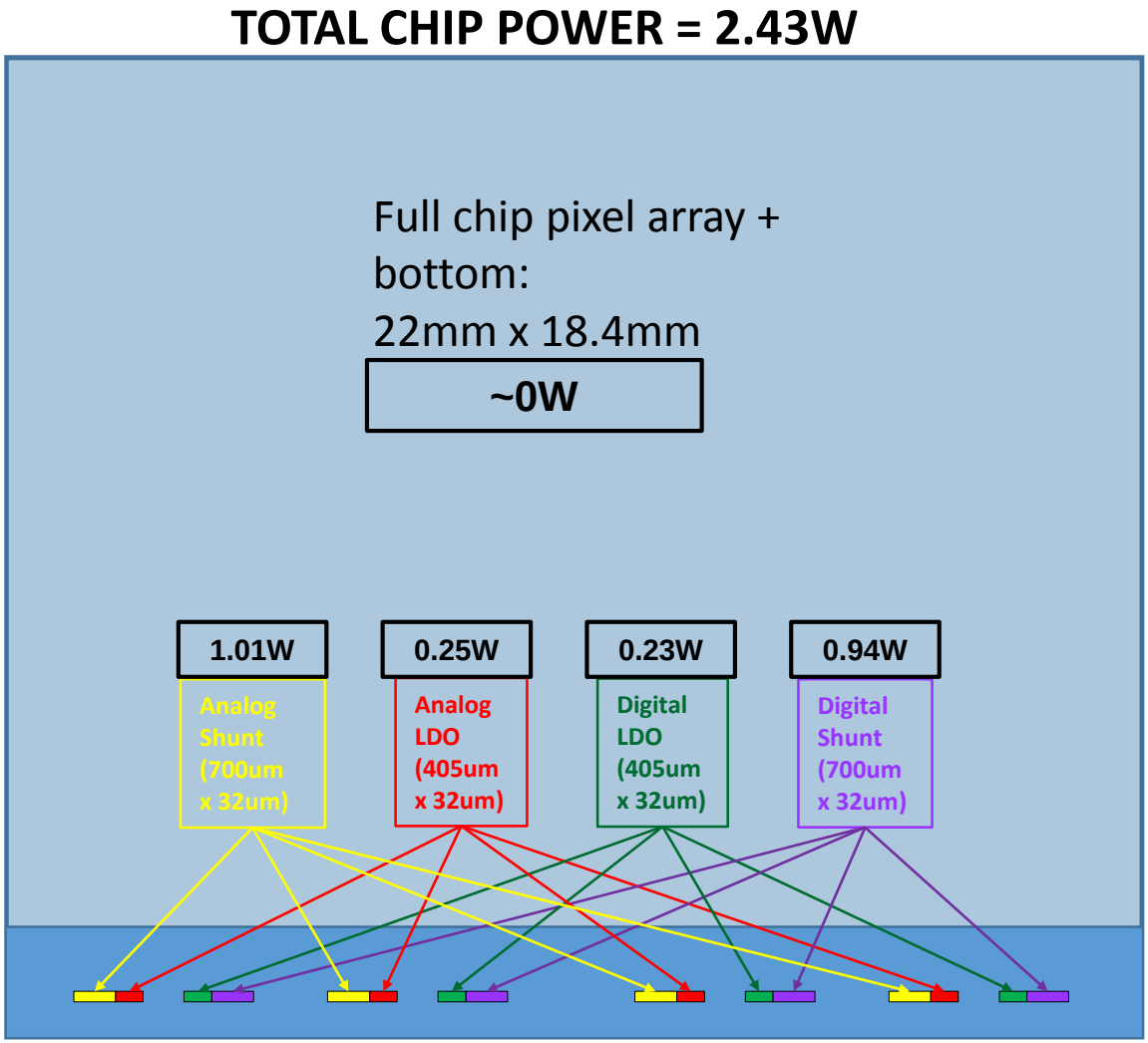
TOTAL CHIP POWER = 2.43W



NORMAL CASE

- Dissipated power in each chip
- Power dissipated in shunts and LDOs is distributed among the 4 blocks
- In normal mode all the chips dissipate the same power

1.2 Working modes power distribution

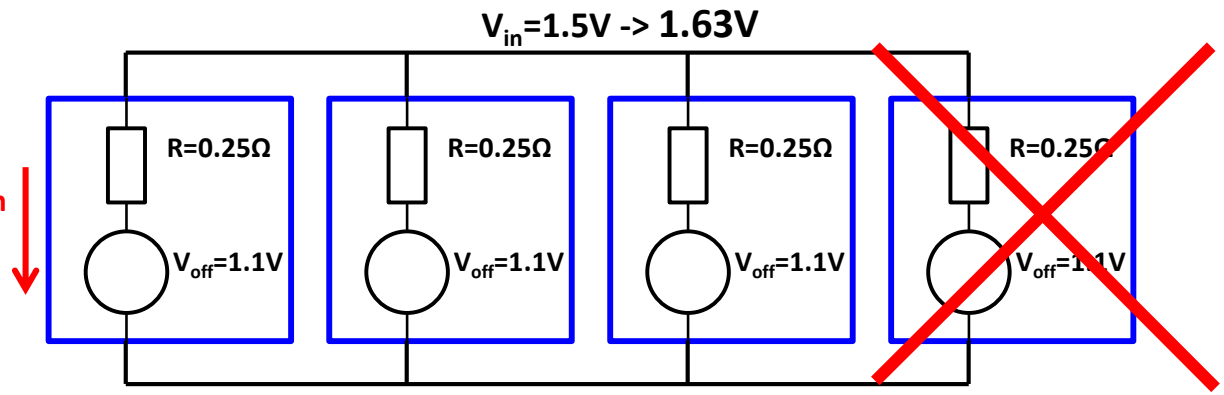


NO LOAD CASE

- **Case of extreme mis-configuration of chip with almost no active load**
- All the power is dissipated in the SLDOs (mainly on shunts)
- Power dissipated in shunts and LDOs is distributed among the 4 blocks
- In normal mode all the chips dissipate the same power

1.2 Working modes power distribution

4-CHIP MODULE
WITH 1 CHIP FAILURE

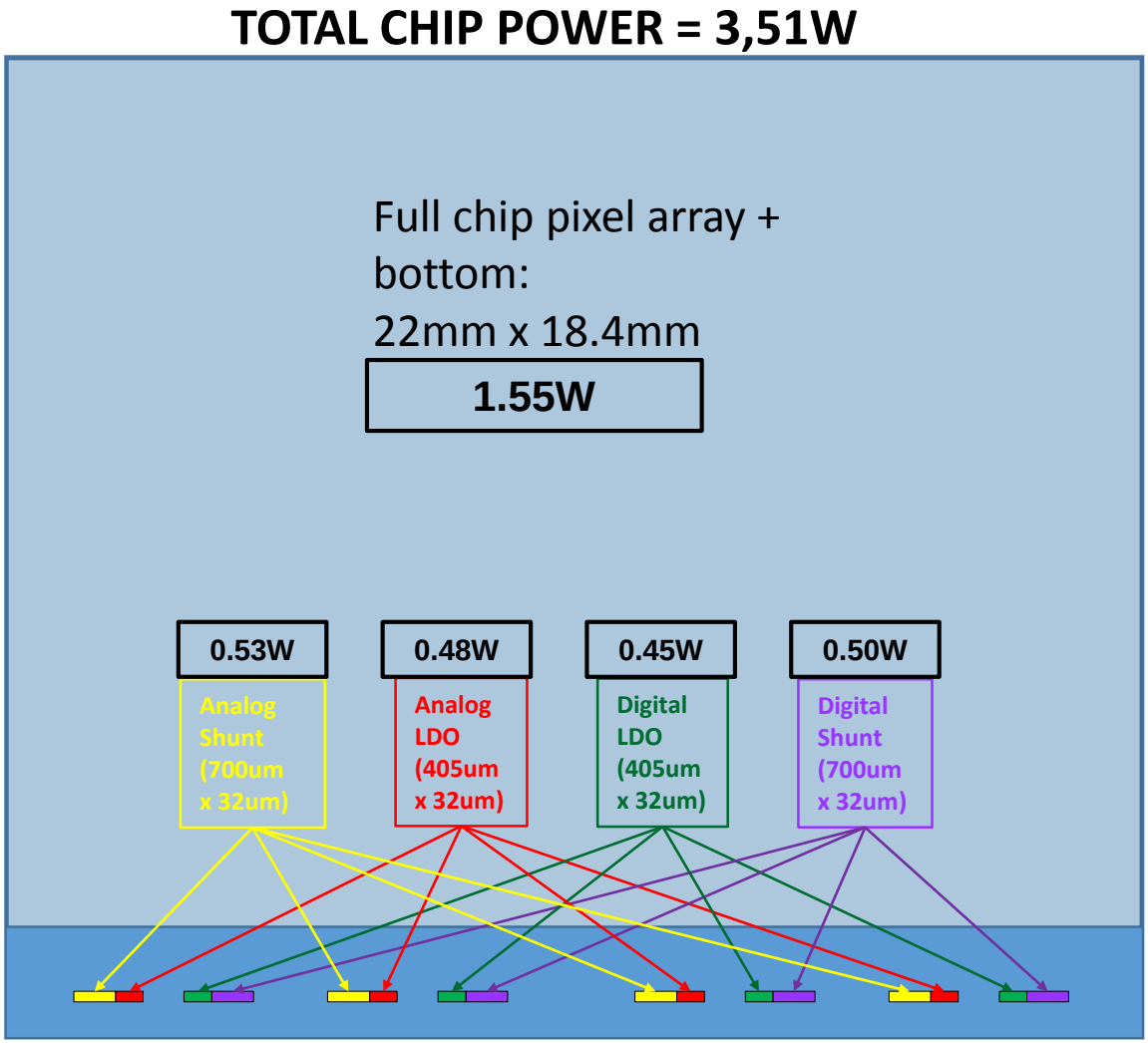


I_chip = 1.33 x I_nom = 2.16A

1 OF 4 CHIPS FAILURE

*R=X.XXΩ (eq. resistance for nominal chip consumption)

1.2 Working modes power distribution

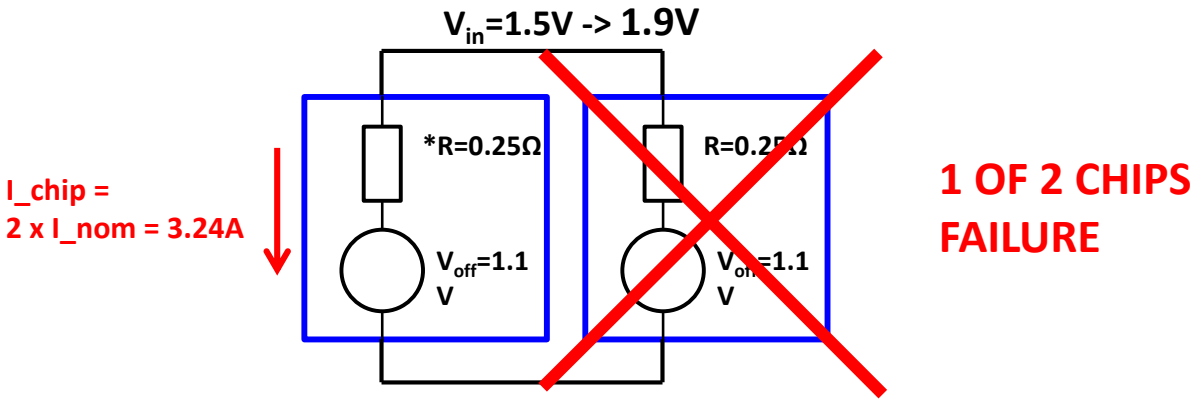


1 OF 4 CHIPS FAILURE

- Shown nominal dissipated power in each working chip of the module with failure
- Power dissipated in shunts and LDOs is distributed among the 4 blocks
- **For thermal simulations, consider a failure in 1 module and the rest in normal mode**

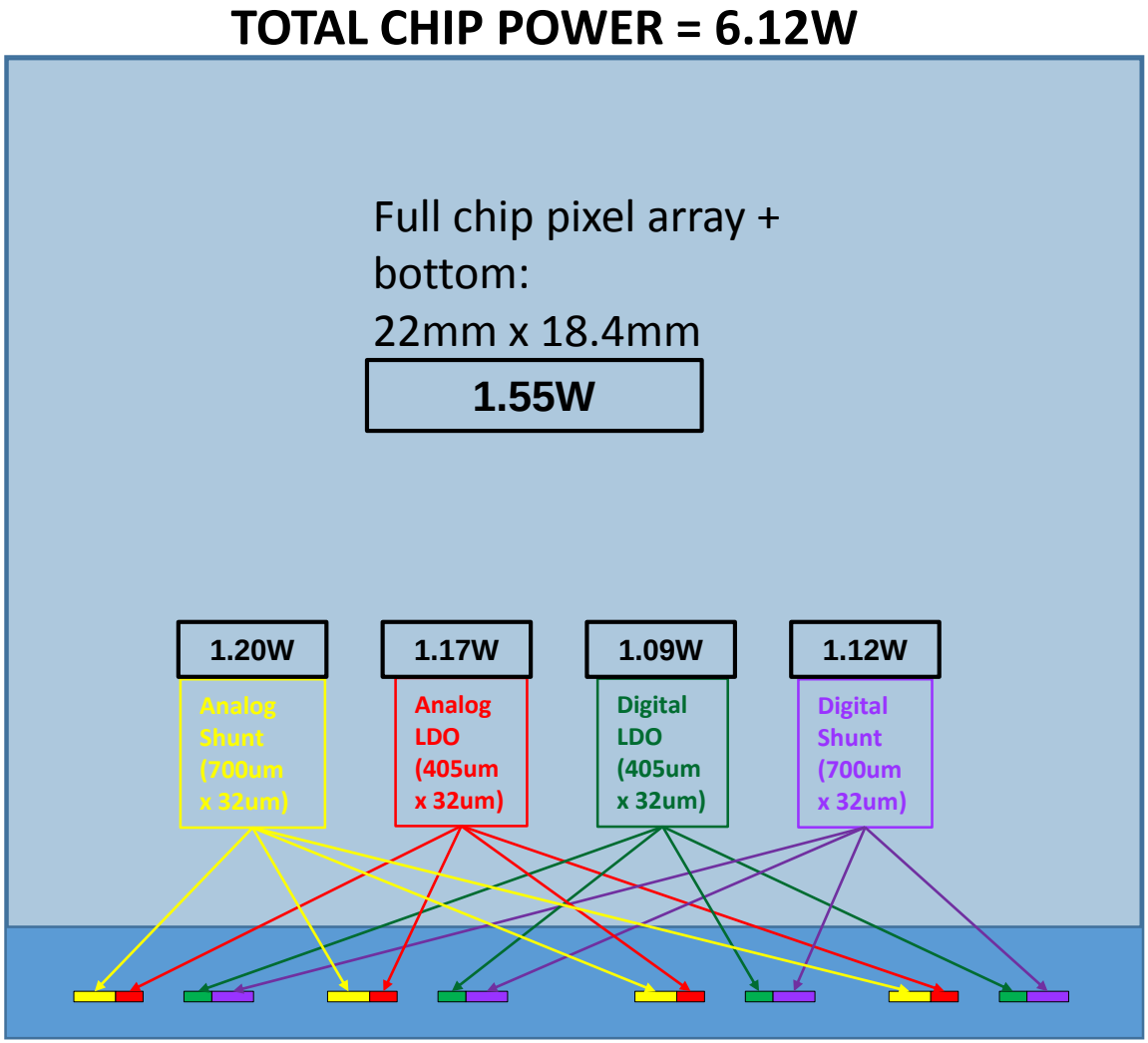
1.2 Working modes power distribution

2-CHIP MODULE
WITH 1 CHIP FAILURE



*R=X.XXΩ (eq. resistance for nominal chip consumption)

1.2 Working modes power distribution



1 OF 2 CHIPS FAILURE

- Shown the nominal dissipated power in the working chip in a module with failure
- Power dissipated in shunts and LDOs is distributed among the 4 blocks
- **For thermal simulations, consider a failure in 1 module and the rest in normal mode**

1.3 Power dissipation density (chip hot spots)

- Power dissipation is not uniform distributed, even in normal modes it is very concentrated in the SLDOs area. This should be taken into account for the cooling system design.
- Total chip area = **~405mm2**
- SLDOs area = **~0.3mm2**
- **Some fast numbers of chip power density:**
  1. Nominal case:
     - Pixel array + bottom -> ~4 mW/mm2
     - SLDO -> ~ 3000mW/mm2
  2. 1 of 2 chips failure case:
     - Pixel array + bottom -> ~4 mW/mm2
     - SLDO -> ~ 15000mW/mm2
- To get optimum cooling performance (max temp and gradient) -> **thermal simulations**

1.4 Proposed temperature constrains (to be verified)

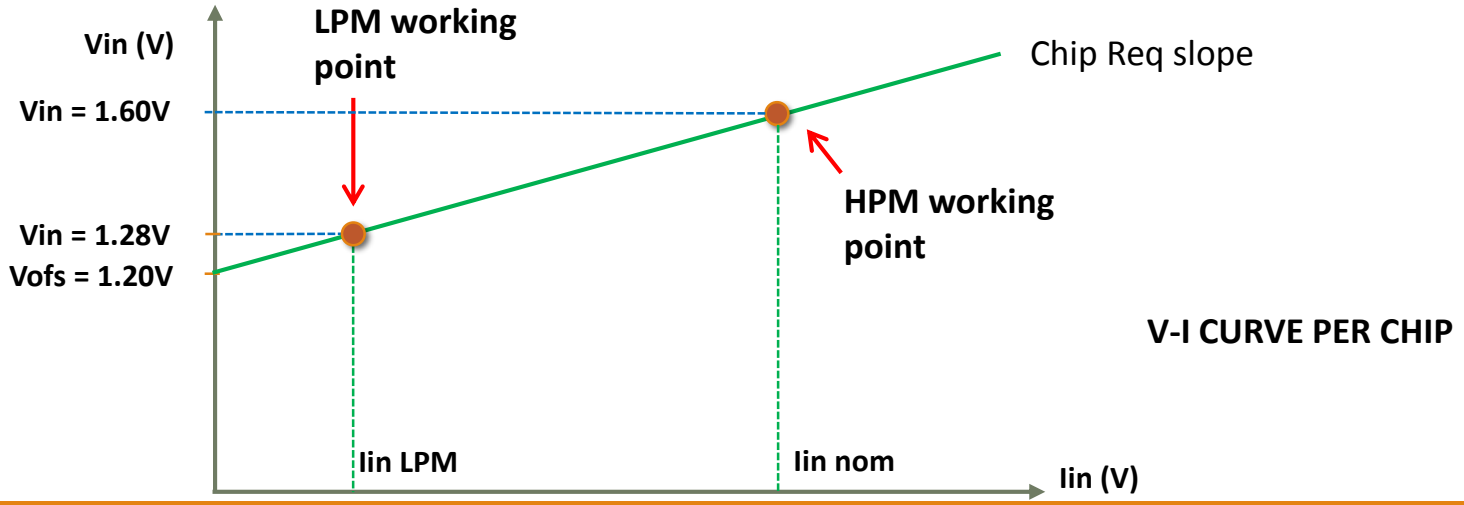
	Max SLDO temp.	Max pixel temp.	Max chip gradient	Max pixel array gradient
Normal operation	0 C	-20 C	15 C	5 C
Failure (degraded) mode	20 C	0 C	20 C	10 C
Absolute maximum ratings	50 C	30 C	40 C	20 C

- Max SLDO temperature: hottest admissible point in SLDO transistors
- Max pixel temperature: hottest admissible point in pixel array
- Max chip gradient: Highest temperature difference inside the chip
- Max pixel array gradient: Highest temperature difference along the pixel array

1.5. Low Power Mode

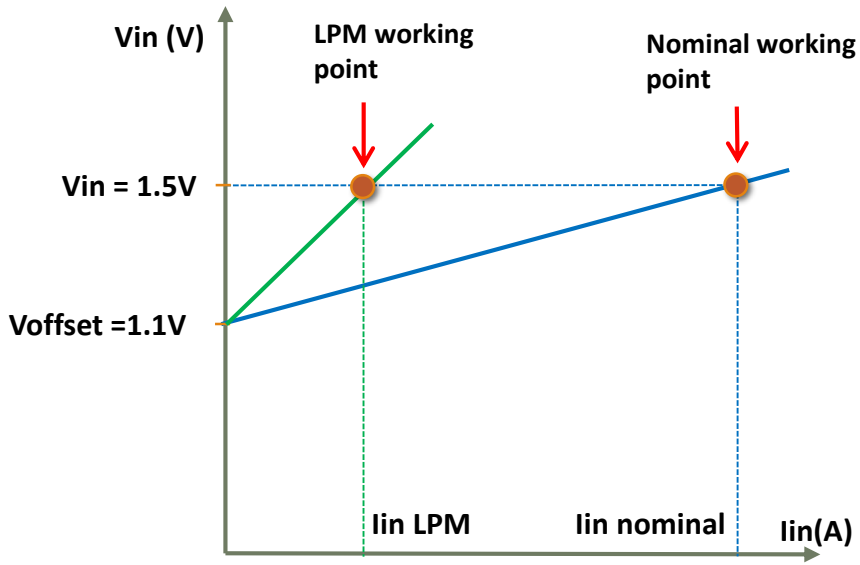
- LPM is a minimum functionality mode of the CHIP, with reduced power consumption, to quick test of interconnects without CO2 cooling (air cooling required)
- **Chip power ~20% of Nominal** (possibility of lower power is under study) -> should be safe to run (based on Atlas FEI4 prototype tests)
- Serial Powering -> **Power dissipation is always defined by SLDO** configuration (V-I curve)
- Different solutions are being studied (must converge within next ~3 months)

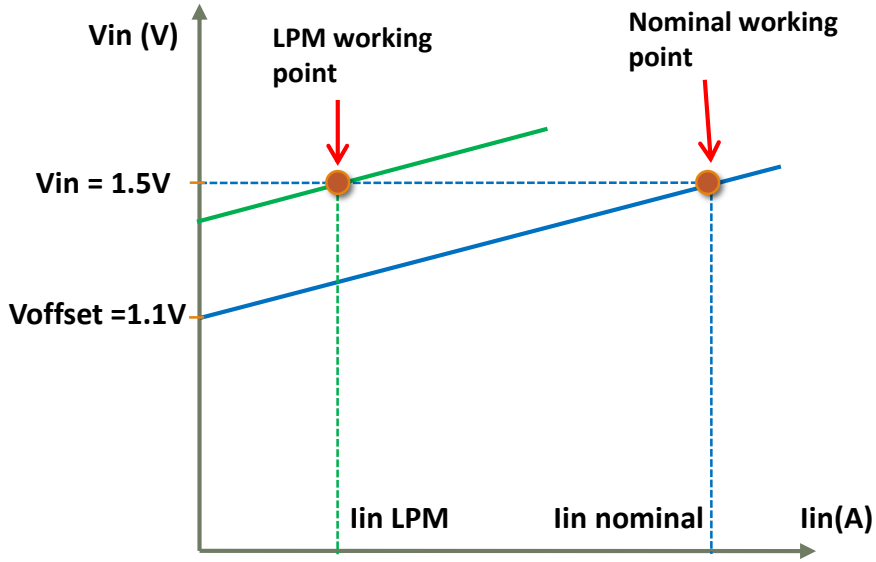
1. **Fixed SLDO V-I curve with high Voffset** to get higher Vin in low current:
   - No need of extra circuits but limited config options (limited Vin in LPM)
   - 2 options: Lower slope (Iin sharing issues) / Similar slope (higher power in HPM)



1.5. Low Power Mode

2. **Different SLDO slopes (or Voffsets) depending on the working mode (LPM or HPM)**. This working mode should be selected somehow:
   - **External signal:**
     - Extra signal line connected to all chips in a chain is needed
     - Selection is done before powering-up
   - **Internal signal (based on supplied current)**
     - No need of extra signals
     - Selection is done during power-up with added circuitry





1.6. Conclusions

- Power dissipation model has been updated: **Previous absolute worst case scenarios have been removed** because they were based on non-realistic corners scenarios
- Updated model takes into account the maximum hit rate scenario typical consumption (inner layer)
- **Optimum, nominal and conservative** consumption will depend on the electronics architecture of final chip
- Further efficiency improvements are under study / TBD (head-room reduction)
- Hot spots at SLDO transistors should be carefully taken into account for the cooling system design (max temps and gradients)
- LPM possibilities are under discussion