Joint RD53A Serial Power Tests at CERN

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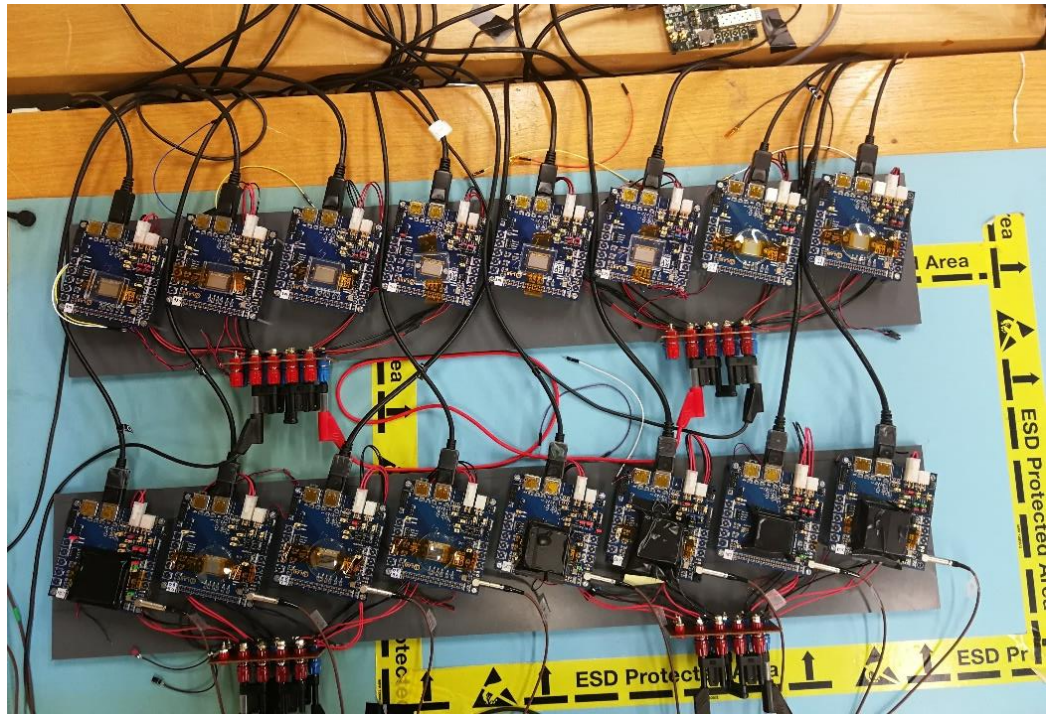
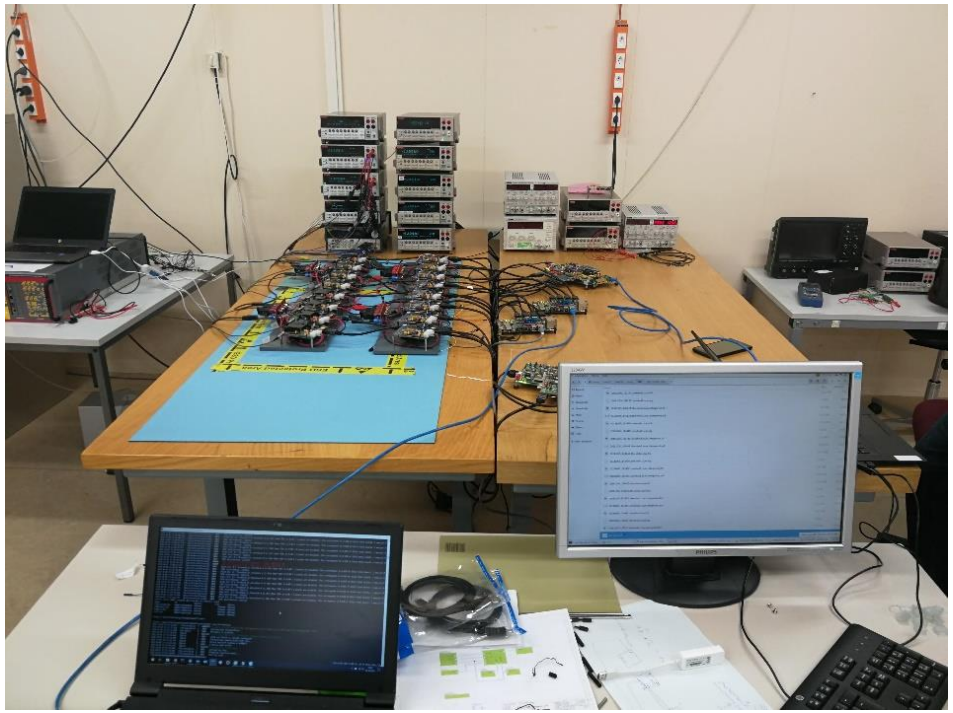
https://indico.cern.ch/event/755140/

Outline

- Introduction & test setup
- Measurements
  - Voltage drops on modules
  - Power up and current sharing
  - HV distribution
  - Operation of chain (threshold scans)
- Conclusion and takeaways

Introduction





- Joint RD53A Serial Power Test among ATLAS and CMS institutes at CERN (Oct 1-5 2018)
- Goal to get first experience operating long chain of RD53A chips
- And start systematic serial power chain tests with RD53A chips

Single chip configuration and pre-measurements

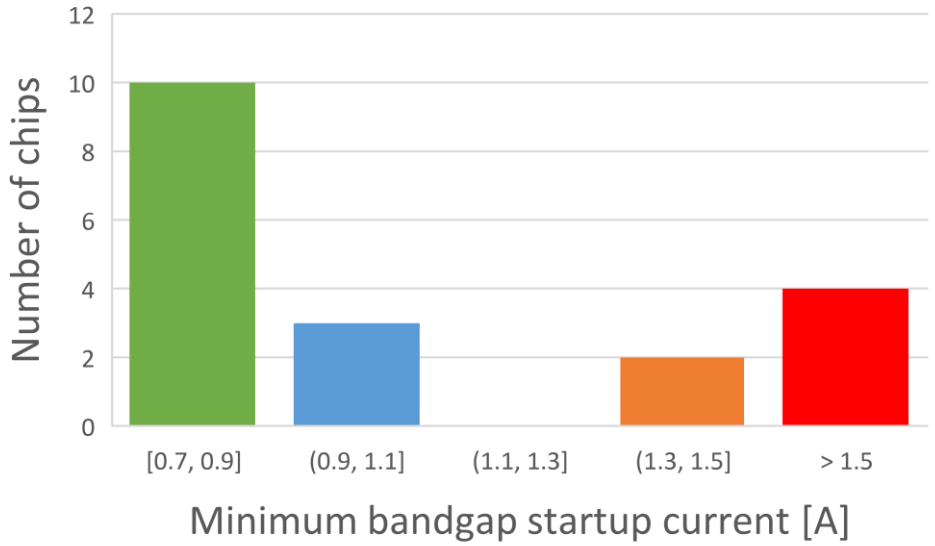
- All chips configured the same:
  - Slope resistors Rext = 806 Ohm
  - Offset resistors Riofs = 250kOhm (=> Vofs ≈ 1V)

$VIN_{chip} \approx 1.4V$ @ 1A

(RD53A max current consumption ≈ 1A)

- Applied VREFA-Bandgap hack for better communication
- Remove DC coupling resistors (if mounted)
  - Shield, GND and sensing connections through DisplayPorts

- Measured minimum chip input current to start up bandgaps for each chip:
  - Some bandgaps need more current (voltage) to „start-up“



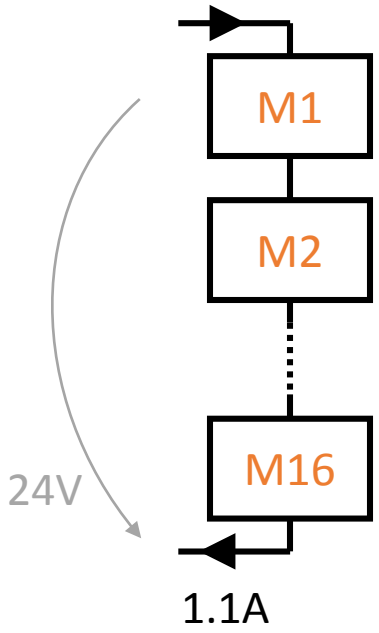
=> Drives the minimum current that has to be put into whole chain in the beginning

- Note RD53A max total current ≈1A
  => Some BGPs need much more

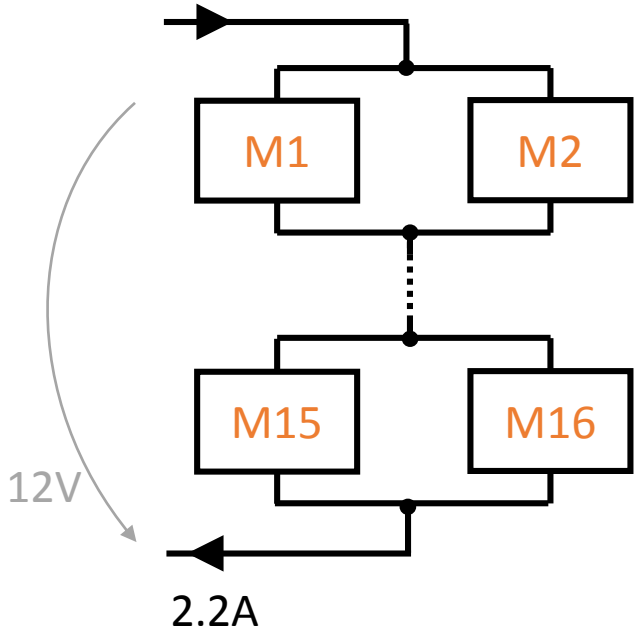
Long chain of 16 SCC

- Tests with 16 chips:
  - 8 with various planar sensors
  - 8 bare chips
- Gradually increased number of chips in chain to 16
- Ultimately tested three constellations:

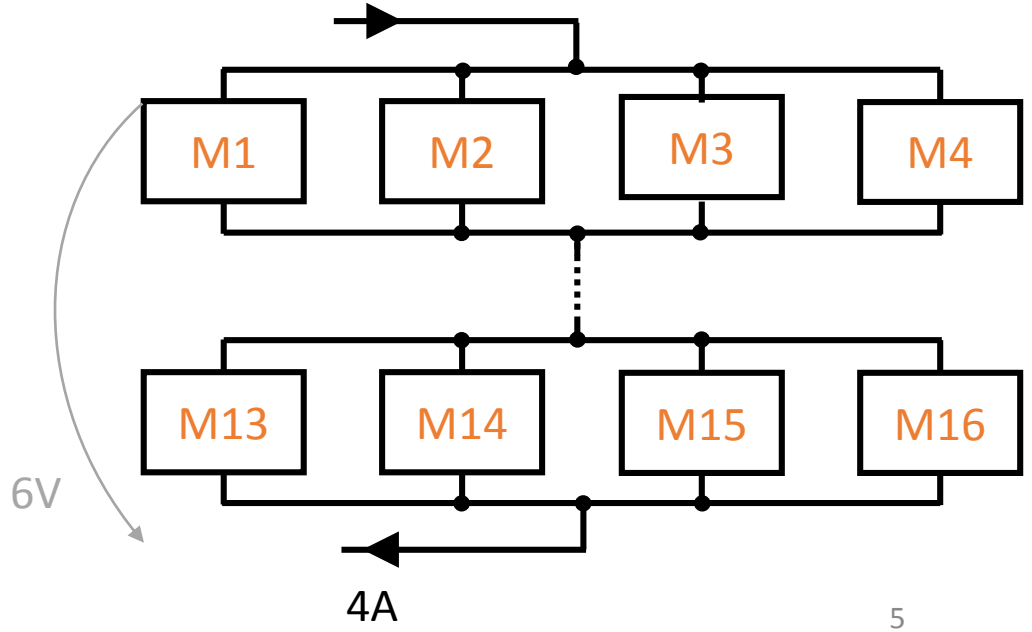
a) 16x1
16x “Single-chip-modules”



b) 8x2
8x “Double-chip-modules”



c) 4x4
4x “Quad-chip-modules”



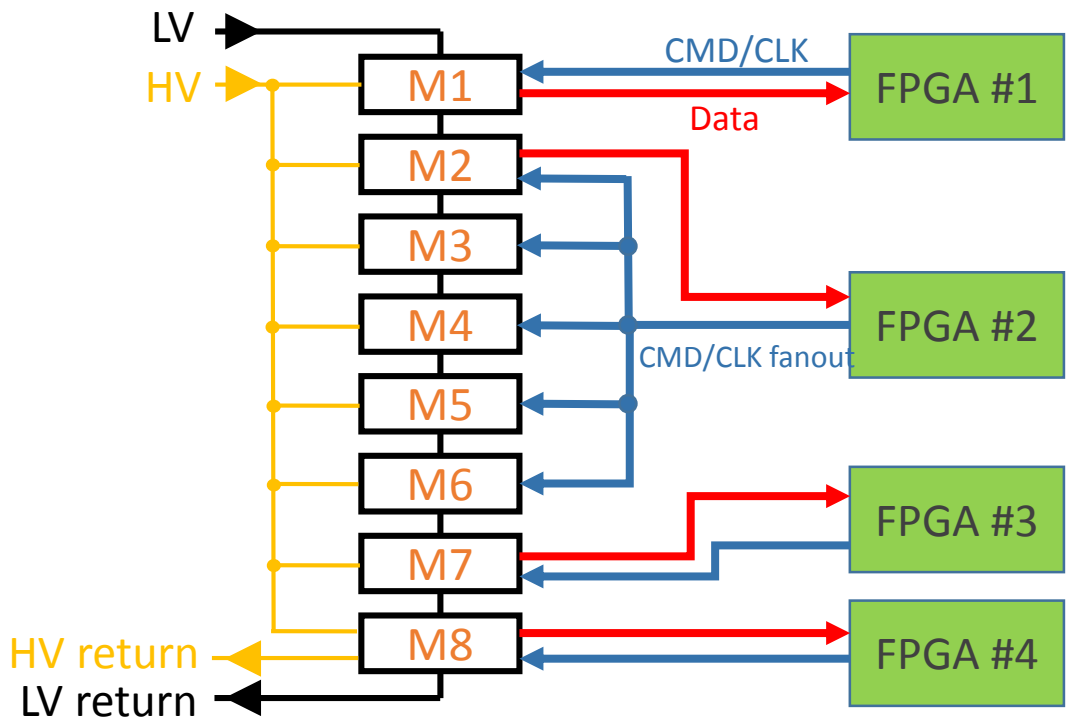
Readout systems

- 4 BDAQ53 readout systems:
  - 2x BDAQ boards
  - 2x KC705 boards + CERN FMC + Ohio FMC

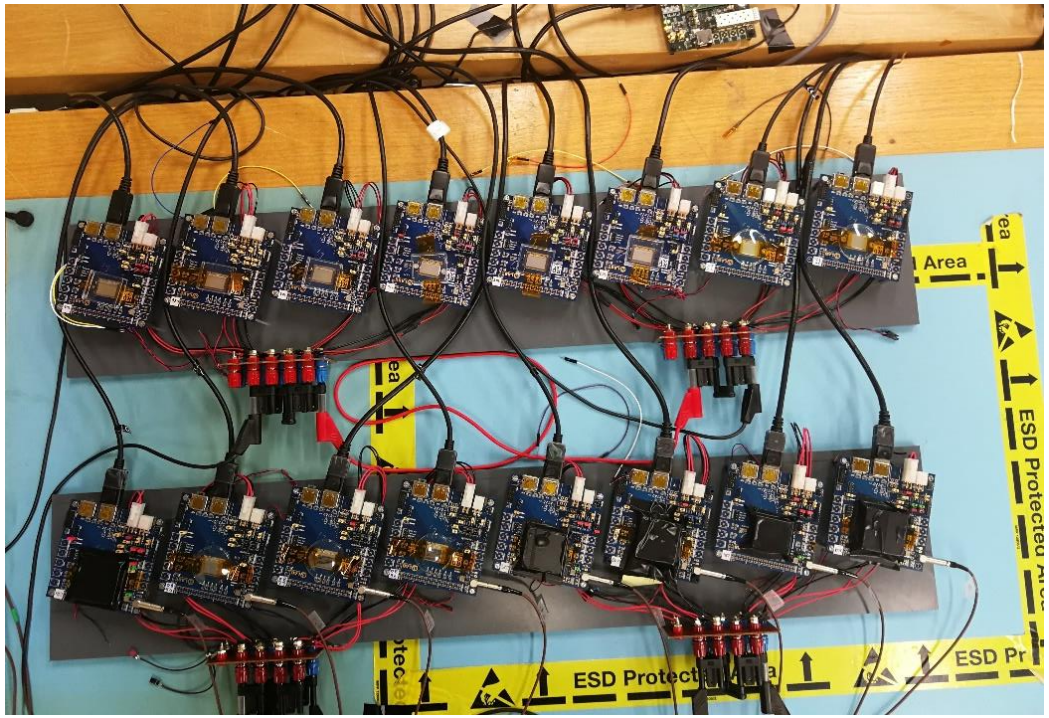
} 4 readout + up to 18 cmd/clk

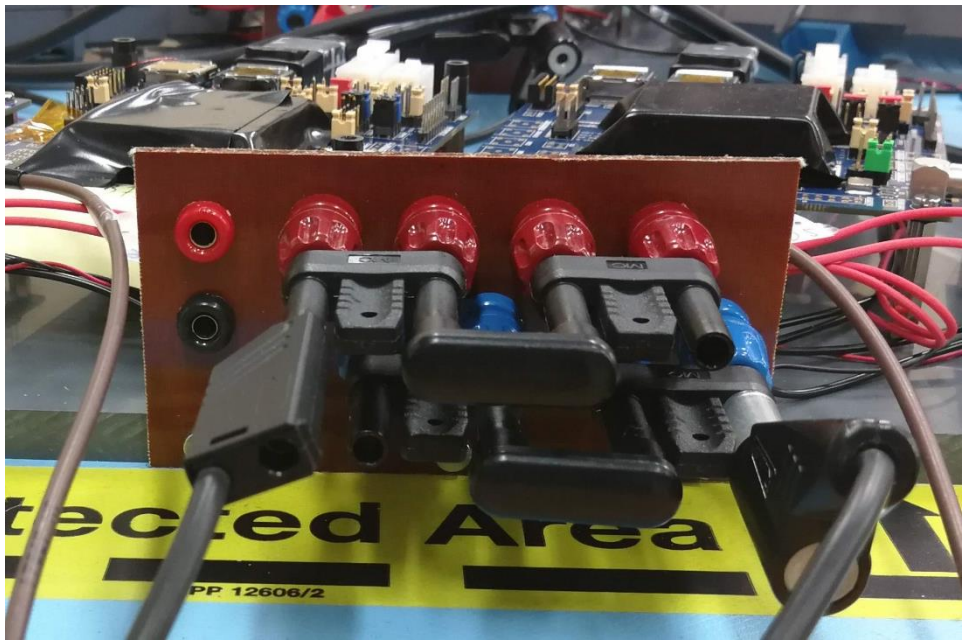
- Only 1 readout per board supported so far => bottle neck for some measurements
- CMD/CLK fanout: Commands are mirrored => 1 command stream per board

- Example of a 8x1 chain setup:
  - Different LV supplies used
  - Keithley Sourcemeters for HV



Test setup - Mechanics





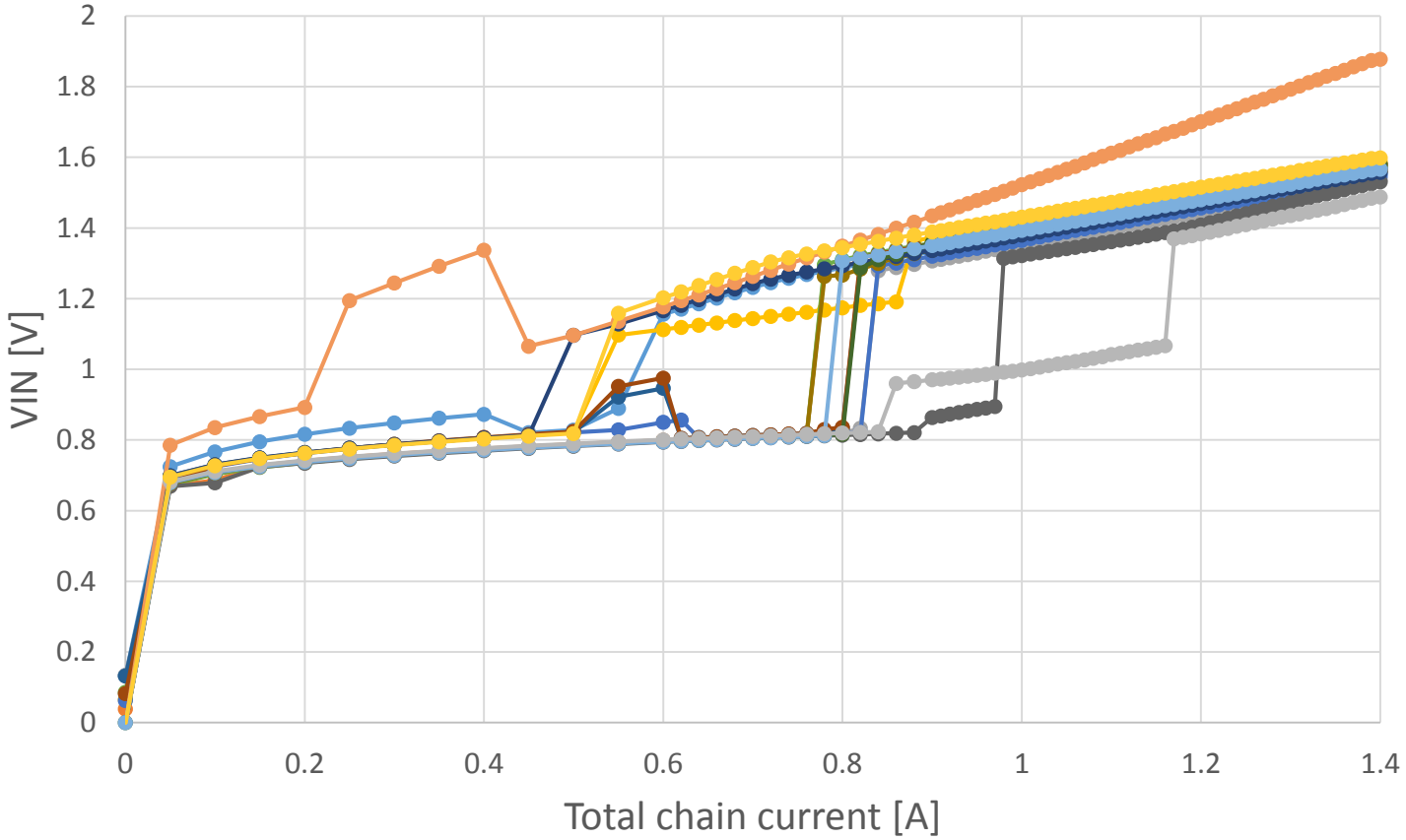
- Two mechanical structures designed by Bane
- Each can hold 8 SCCs
- Molex to banana adaptation for low voltage
  => Easily changeable between single/serial/parallel chain operation
- Cooling via heatsinks

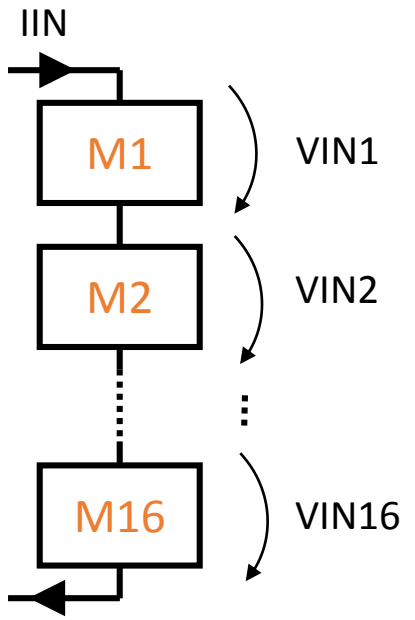
Voltage drops on modules – IV curves

- Instruments
  - 8 Keithley Sourcemeters / Multimeters
  - 1 Keithley 2230G LV Power supply
- For each setup
  - Increase current to chain
  - Measure Voltage drop on SCC (Chip VIN)
    - Measurement point = input jumper against PCB GND

    => Not closest point to chip: Trace impedance missmatches between chips possible

IV curves for 16x1

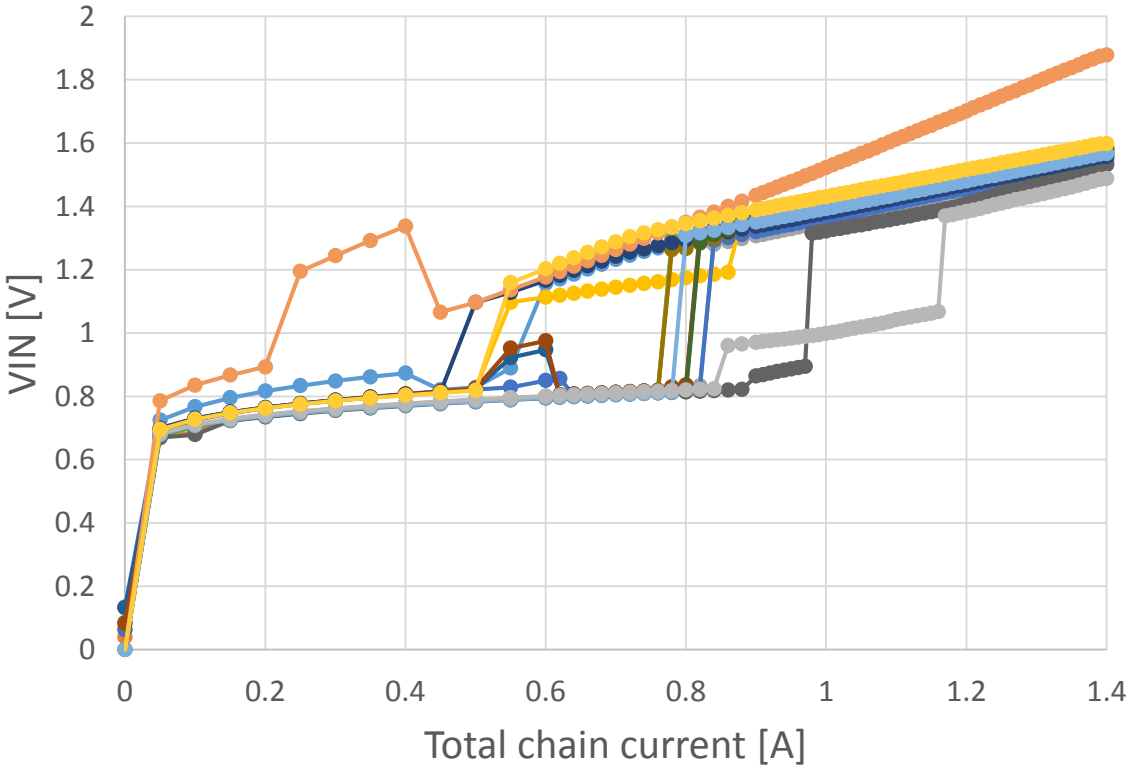




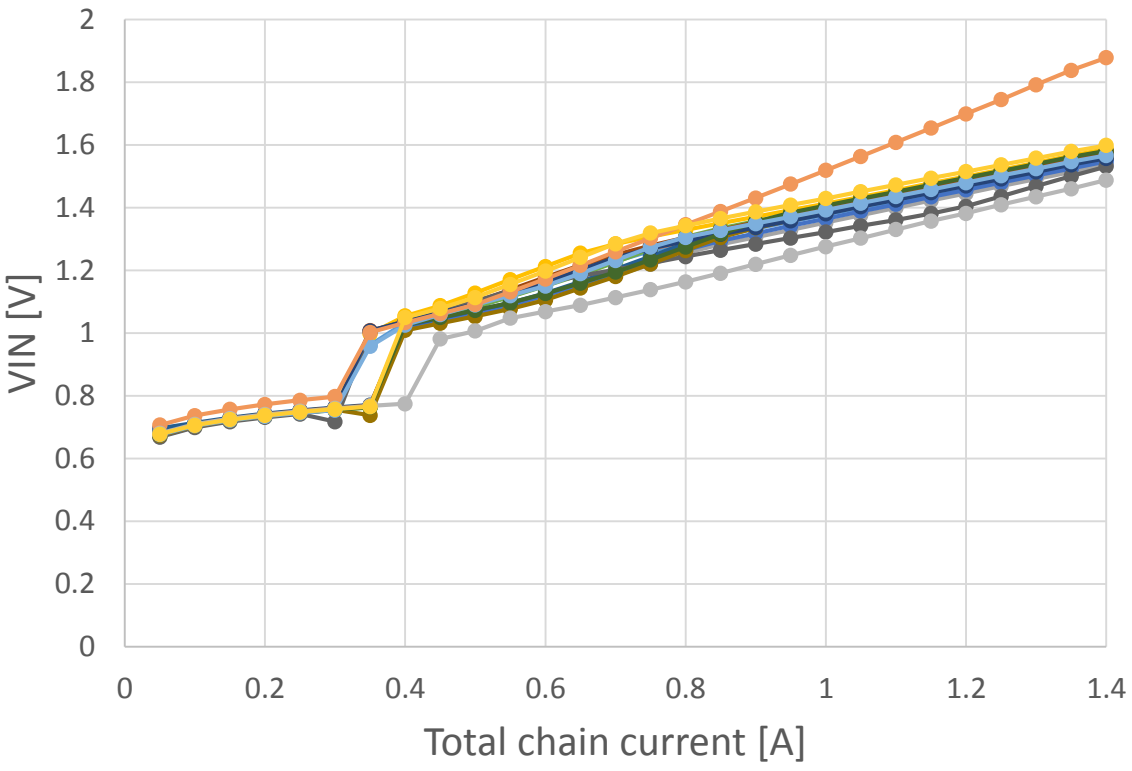
- Sharp jumps up in VIN-curve are start-ups of bandgap voltages => expected differences
- One bad behaving chip => different slope, and fluctuations in the beginning

  => After checking analog regulator is bad (more in backup)
- Slope and offset extraction ongoing

IV curves for 16x1: Ramp up and ramp down



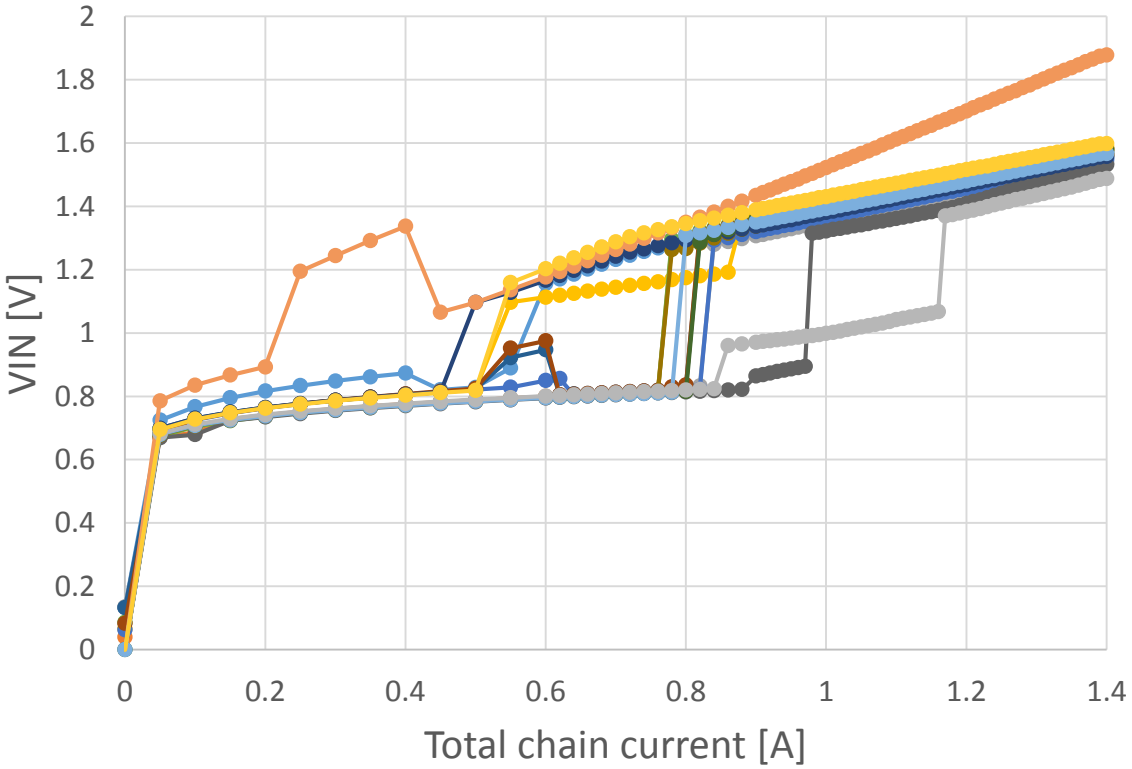
Ramp up

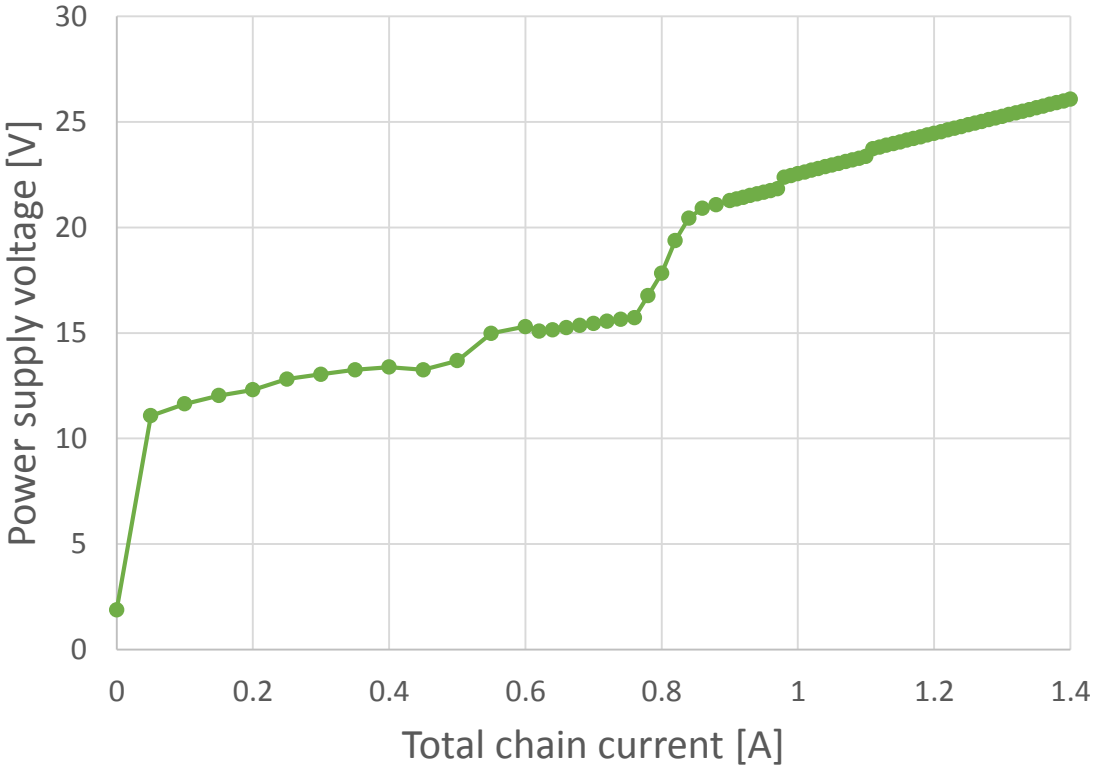


Ramp down

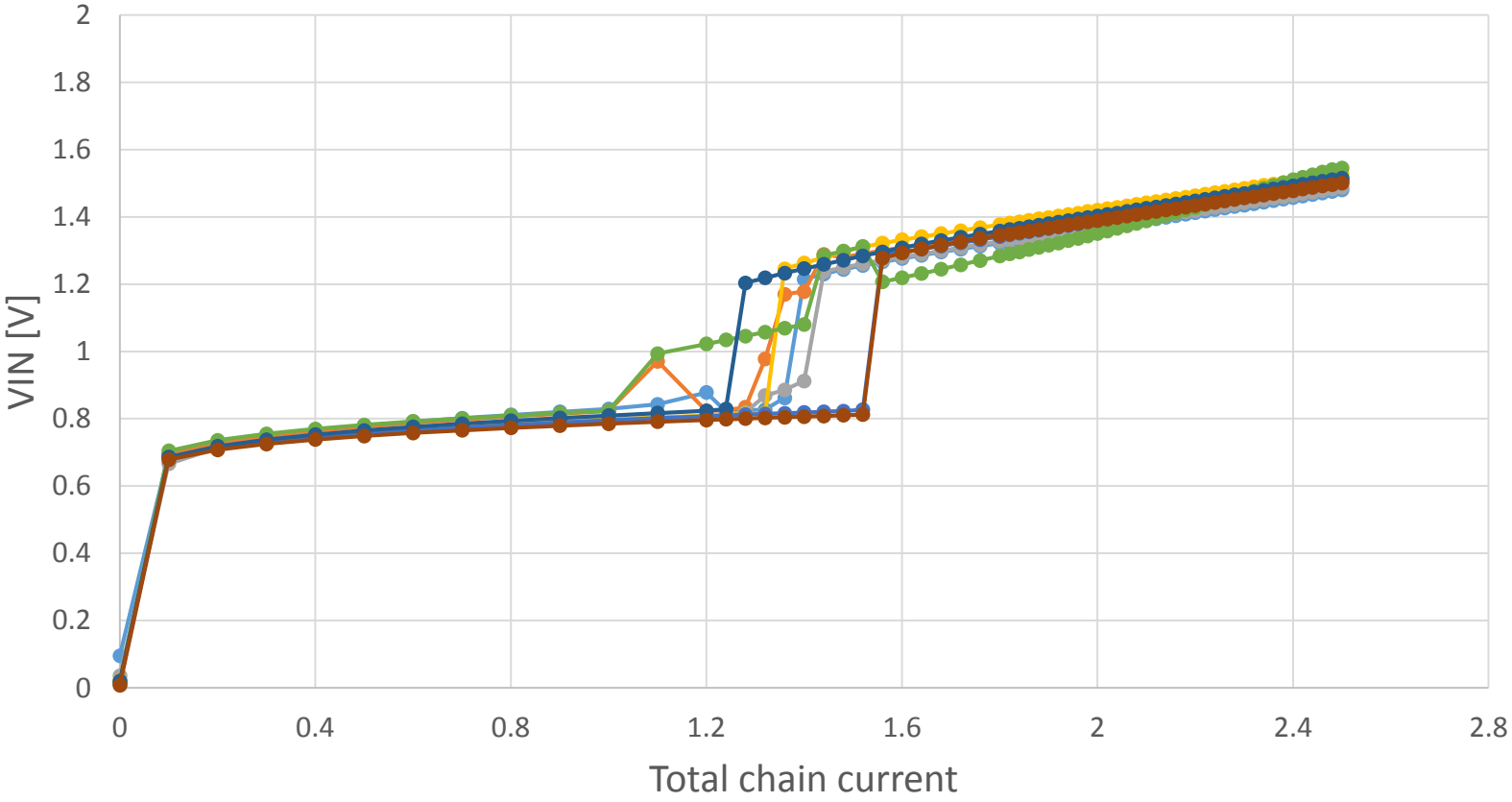
- For comparison adding ramp down => after bandgaps started IV curve is much smoother

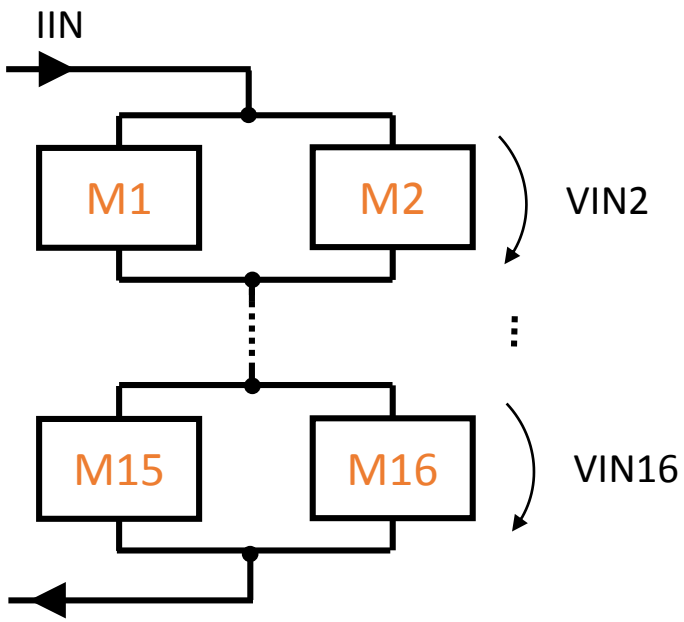
IV curves for 16x1: Power supply voltage





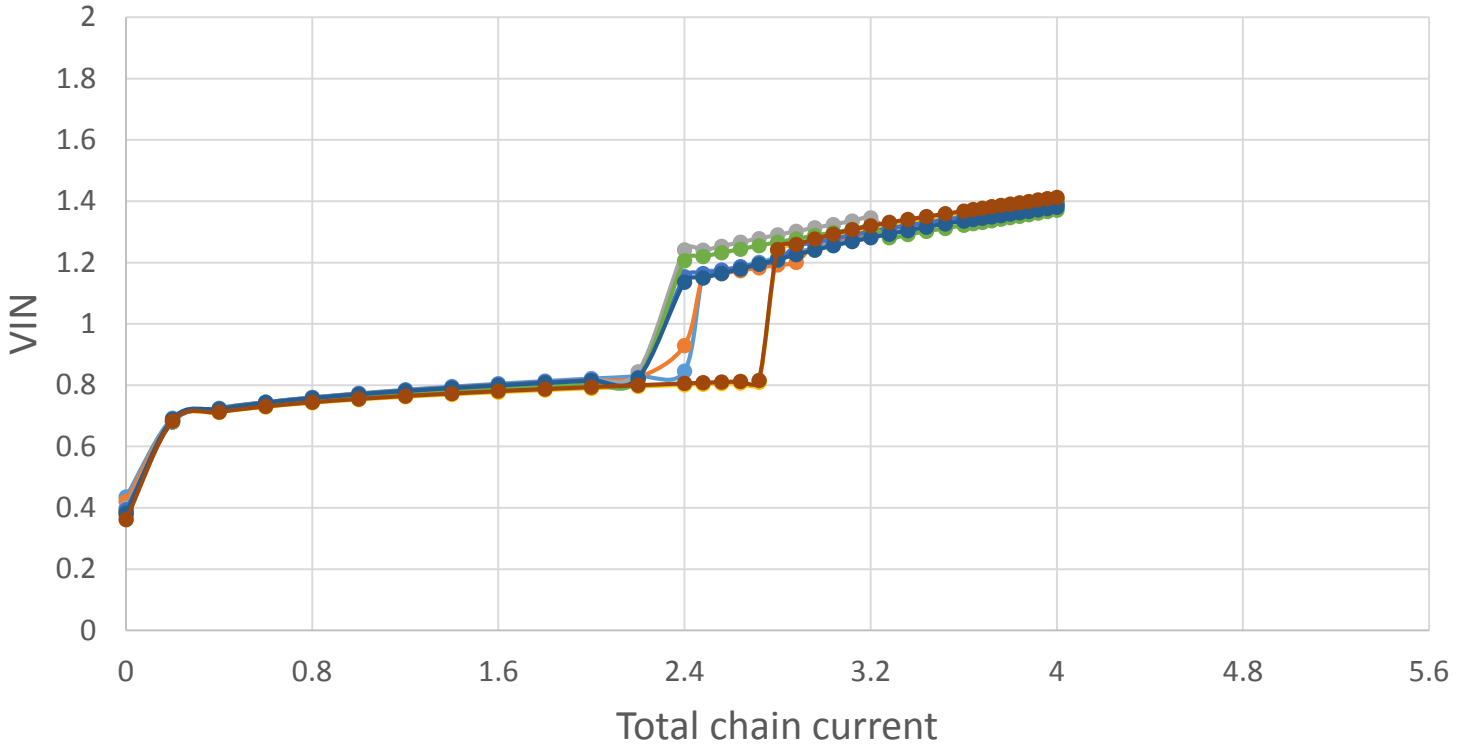
IV curves for 8x2

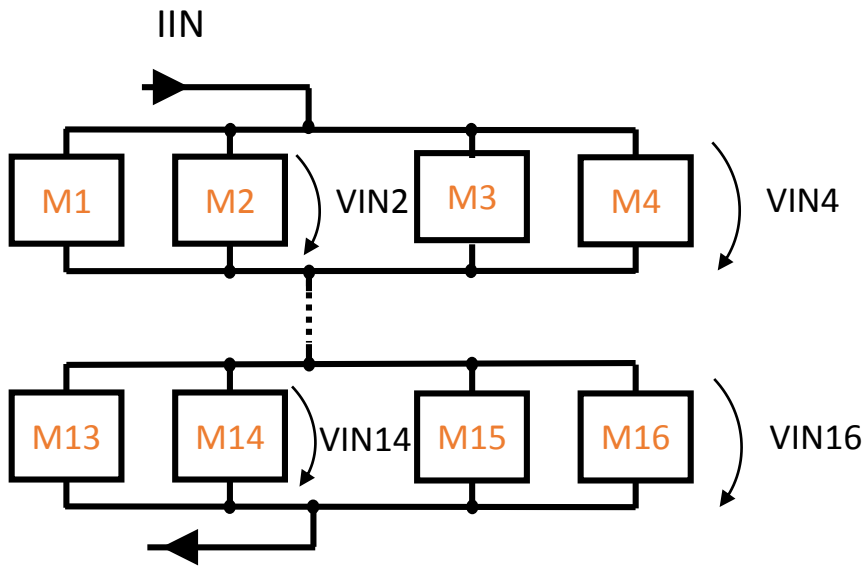




- Measured one VIN per two chips on same level in chain
- IV curve is smoother, jumps are closer together:
  - Parallel operation works in favor of “late” Vofs bandgaps
  - (No effect on “late” Vref bandgaps)

IV curves for 4x4





- Measured two VIN per four chips on same level in chain
- Reached PS voltage limitation (6V) at 4A
- Small differences between VINs on the same level:
  - Combination of current sharing variations or current path impedance mismatch

Power and current sharing

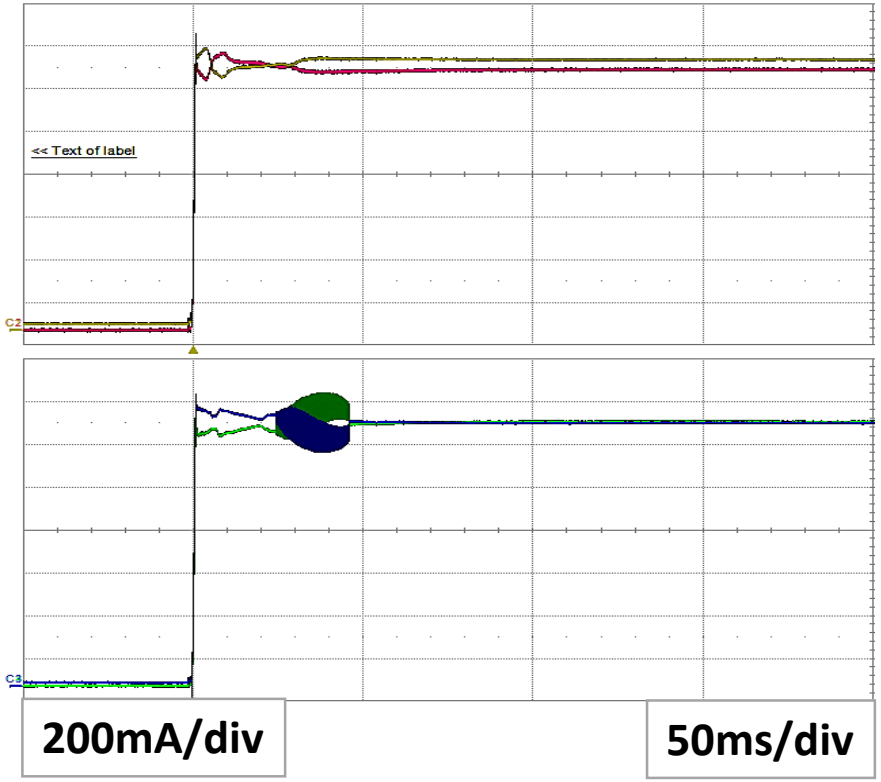
- Instruments
  - Lecroy HDO6104 Oscilloscope with 4 current probes
  - 1 TTI PL303QMD power supply
- Fast power up with power supply
  - Measured each chip Iin for 8x2 and 4x4 chain constellation
  - Not all SCCs had reduced filter capacitors for chip VOUT and VIN

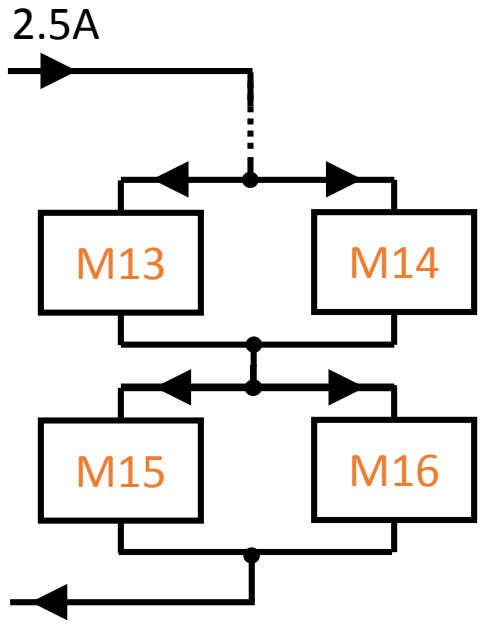
    => Repeat measurements with reduced / minimum capacitors

Start up of 8x2 chain

Iin of M13 & M14

Iin of M15 & M16

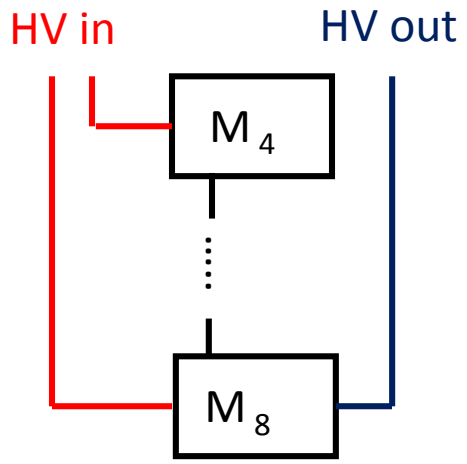




- Observed oscillations in some chip pairs
  - Seen ~175kHz and ~375kHz
- Does not propagate down the chain
- To be investigated more

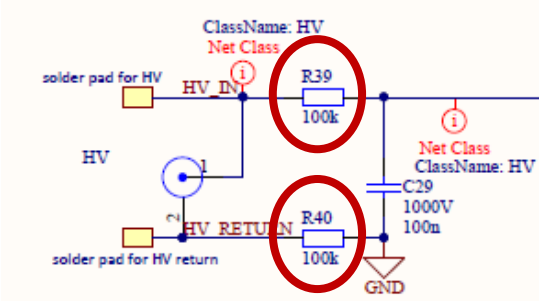
HV Distribution schemes

- Tested different HV distribution schemes with 8-module-chain
  - Module positions 2,3 and 4 exposed to ambient light
  - Common HV line with dedicated return
  - Common HV line with common return
  - 2 HV lines with common return
  - 2x4 and 4x2 common HV lines



- 2 HV lines with common return

- For each setup measure
  - Voltage drop over sensor
  - „Incoming“ and „outgoing“ leakage current using bias resistors (100k) on SCC
  - Using different „off-mode“ of HV power supply (high-ohmic & short)



HV Distribution schemes – Common HV

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-9.5	-3	0
2	201	-8.1	-49	0
3	196	-6.6	-44	0
4	198	-5.2	-58	0
5	282	-3.7	-1.6	0
6	313	-2.25	-1.7	0
7	284	-0.76	-2	0
8	308	**0.73**	**162**	0.6

High-ohmic off mode

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-9.8	-2.7	0
2	201	-8.4	-49	0
3	196	-7	-42	0
4	198	-5.6	-59	0
5	282	-4.15	-1.4	0
6	313	-2.72	-1.5	0
7	284	-1.304	-1.9	0
8	308	0.04	-1.2	158.7

Low-ohmic off mode

HV Distribution schemes – 2HV lines

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-3.89	-2.1	0
2	201	-2.56	-44	0
3	196	-1.17	-37	0
4	198	**0.253**	**85**	0.5
5	282	-3.77	-1.3	0
6	313	-2.37	-1.5	0
7	284	-0.94	-1.8	0
8	308	**0.445**	**4.7**	0.6

High-ohmic off mode

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-4.15	-2.3	0
2	201	-2.71	-43	0
3	196	-1.32	-35	0
4	198	0.63	-46	126
5	282	-4.29	-1.5	0
6	313	-2.88	-1.7	0
7	284	-1.43	-2.2	0
8	308	0.02	-1.3	6.7

Low-ohmic off mode

HV Distribution schemes – 4 HV lines

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-1.36	-1.2	0
2	201	0.09	-3.4	5.1
3	196	-1.27	-26	0
4	198	**0.179**	**24**	0.7
5	282	-0.98	-0.9	0
6	313	**0.454**	**0.7**	0.7
7	284	-1.02	-2	0
8	308	**0.466**	**1.6**	0.5

High-ohmic off mode

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-1.4	-1.3	0
2	201	0.03	-16	19
3	196	-1.36	-27	0
4	198	0.04	-16	41
5	282	-1.42	-0.9	0
6	313	0.01	-1.1	2.6
7	284	-1.47	-2.2	0
8	308	0.001	-1.3	3.5

Low-ohmic off mode

HV Distribution schemes – 2 HV lines with common return

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-4.1	-2.4	0
2	201	-2.67	-39	0
3	196	-1.25	-35	0
4	198	**0.21**	**70**	0
5	282	-3.92	-1.6	0
6	313	-2.46	-1.9	0
7	284	-0.99	-2	0
8	308	**0.49**	**5.1**	5.6

High-ohmic off mode

Pos in chain	SCC	Sensor voltage [V]	V(Iin) [mV]	V(Iout) [mV]
1	281	-10.1	-3	0
2	201	-8.7	-42	0
3	196	-7.2	-38	0
4	198	-5.8	-39	0
5	282	-4.3	-1.7	0
6	313	-2.8	-2	0
7	284	-1.3	-2.1	0
8	308	0.03	-1.1	155

Low-ohmic off mode

HV Distribution schemes

General behaviour as expected

- Current loop through last module in HV line for high ohmic off-mode
  - If local GND shifted enough!
- All leakage current returned normally for low-ohmic off-mode
- No significant difference between different HV schemes observed
- Exposed 8th module in Common HV setup to current loop (forward bias) over night
  - Needed power cycling in the morning (VDDD & VDDA < 1V), alive afterwards
  - Unfortunately did not check the other modules
  - Repeat measurement

Threshold scans and FE tuning

- Comparison of FE performance in different setups with three modules
  - Chain of single chips (8x1, 16x1), double chips (8x2), quad chips (4x4)
- Compare achievable threshold & noise levels
  - In each setup: retune FE with new configuration, store configuration (& masks)
  - Threshold scan for all stored configurations
  - Only for linear FE
- No significant deviation in achievable threshold / noise levels evident
  - More measurements to understand better

Conclusion and takeaways

- Good first experience with long chains
- Could test all relevant serial power chain constellations and HV schemes with 16 chips
- Limited by readout
  - Cmd/clk fanout possible, but currently only 1 readout / 1 fpga board
  - Hard to validate and monitor that chip receives cmd/clk if not read out

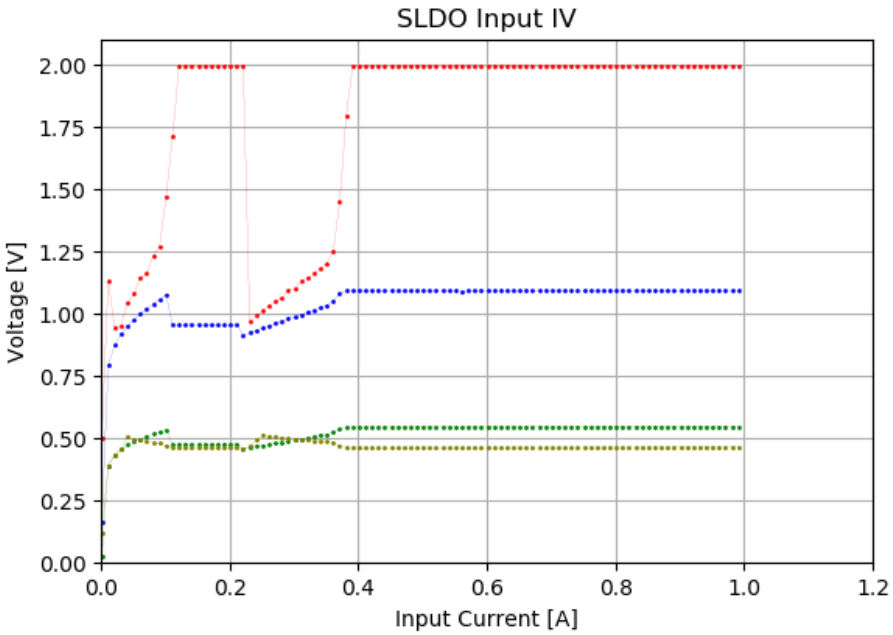
Outlook

- Add modifications and improve DAQ
  - Simultaneous scans with all chips
- Minimum shunt headroom studies
- Noise studies
  - Make chips in chain noisy and monitor others

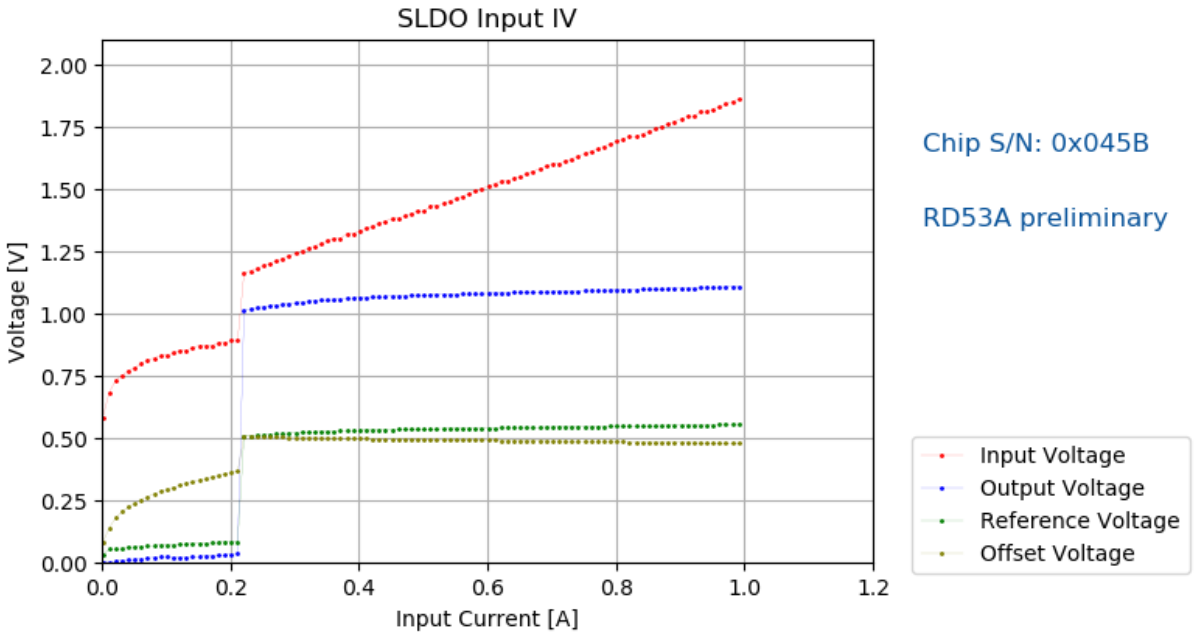
Backup

IV curves – The bad chip

Analog regulator (Independent)



Digital regulator (Independent)



Chip S/N: 0x045B

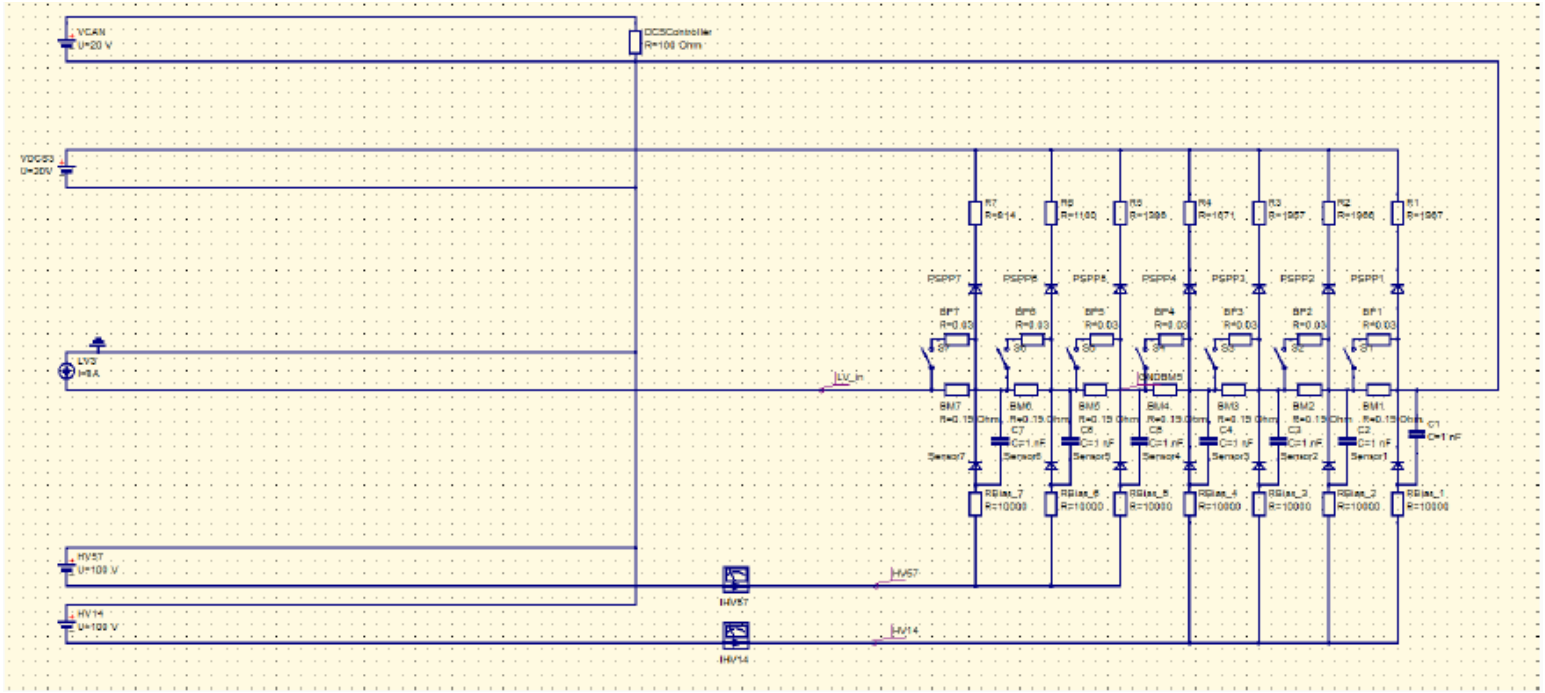
RD53A preliminary

- Strange behavior of analog regulator
- Explains behavior seen in chain

HV Distribution schemes

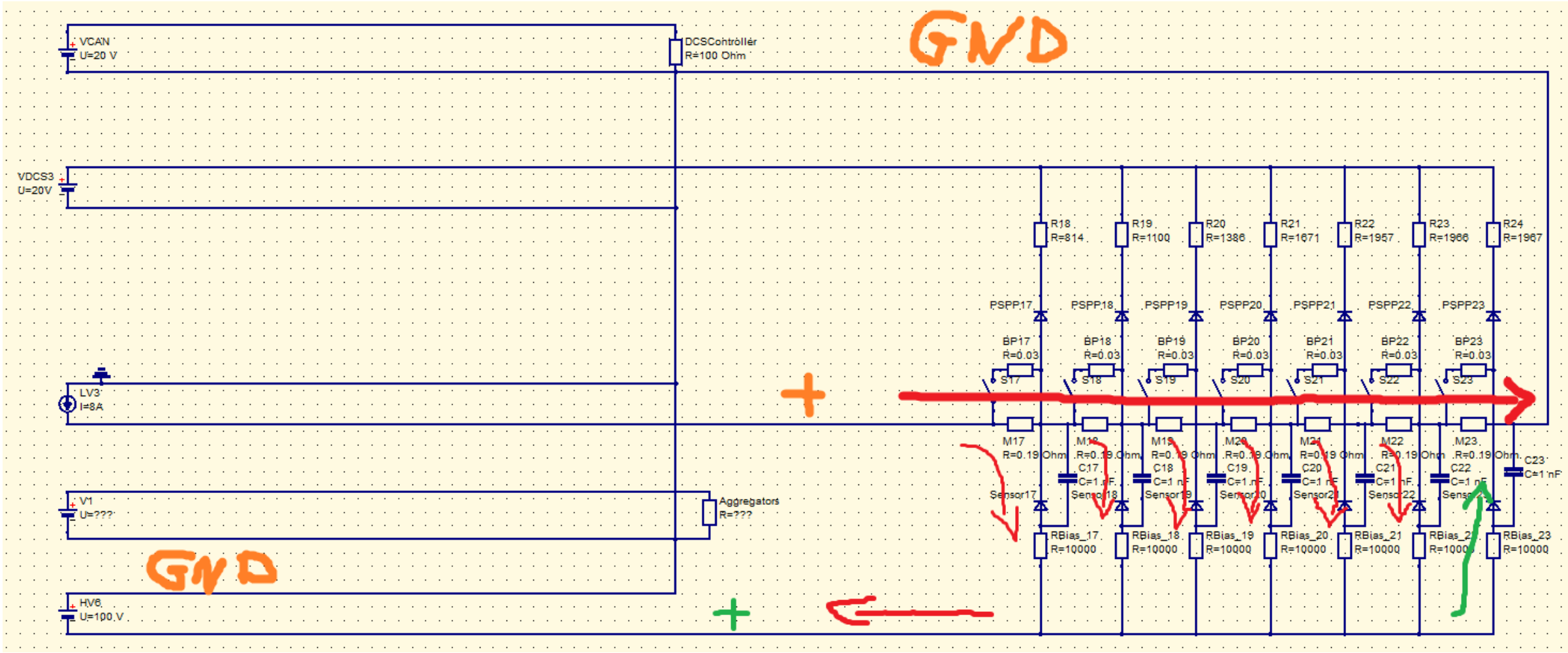
- Lesson learnt from the ITk Outer Barrel Demonstrator
  - 7 FE-I4b Quad modules in serial powering chain
  - 2 HV lines with common returns: HV_modules 1-4 & HV_modules 5-7
  - ISEG HV power supply, high ohmic off mode
- If FE supply voltage (LV) is switched on & HV is switched off:
  - Small sensor bias due to different GND levels in serial powering chain
  - Leakage current does not return through high-omic PSU, but through current loop in last module in HV line (causing forward bias)
  - Could be avoided by using a low-ohmic off-mode for the HV

HV Distribution schemes



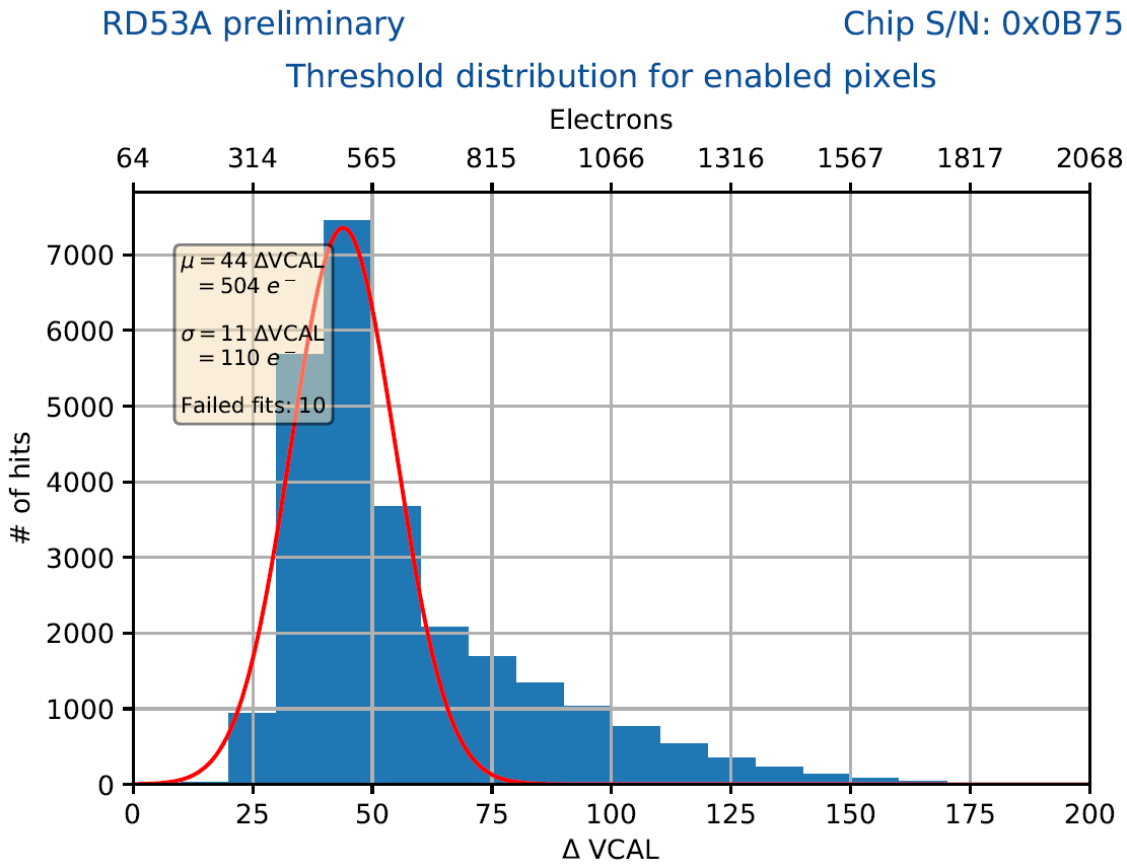
VDCS [V]	LV [V]	RHV [Ohms]	VHV57 [V]	VHV14 [V]
20,0	0,0	6,8M	0,0064	0,032
20,0	12,9	6,8M	7,0000	0,336
20,0	0,0	10k	0,0005	0,0058
20,0	12,9	10k	0,0460	0,0705
20,0	0,0	open	0,1930	0,032
20,0	12,9	open	9,0000	0,337
0,0	0,0	any	0,0000	0

Backup

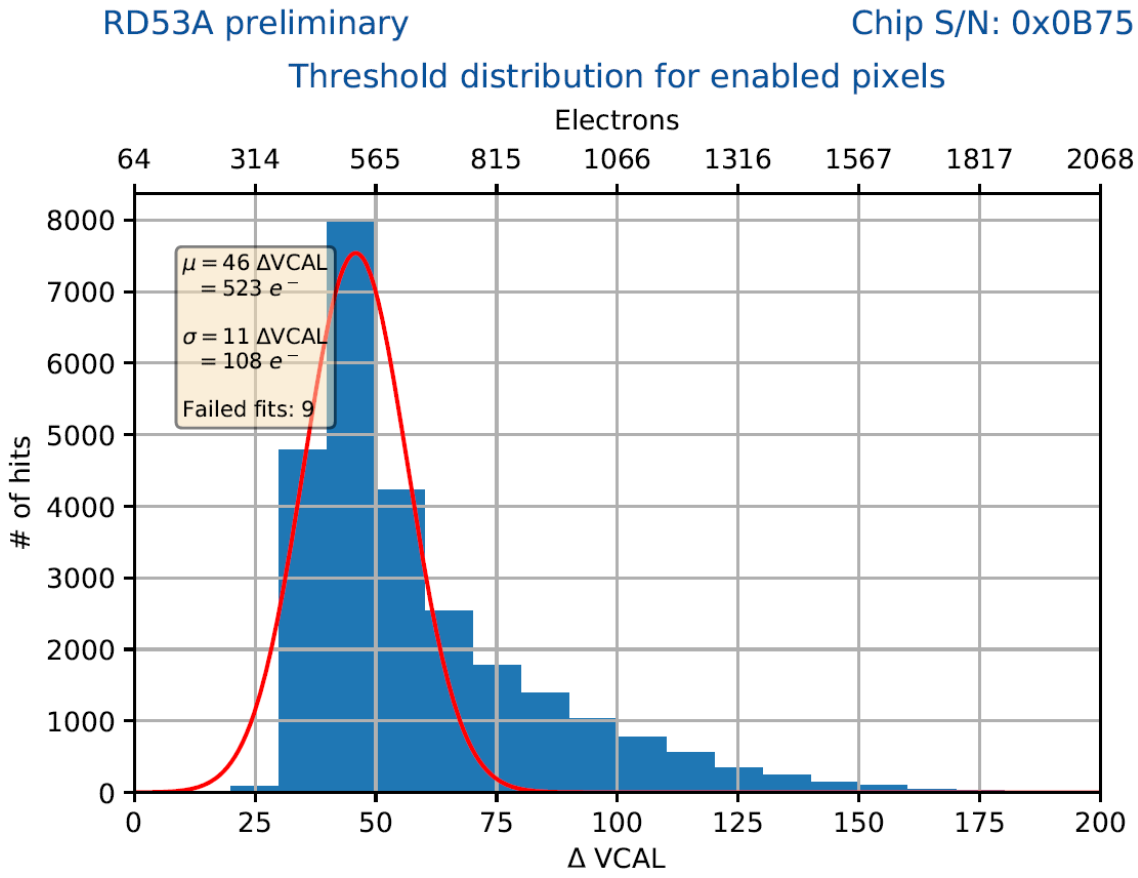

VCAN
U=20 V
DCSController
R=100 Ohm
GND
VDCS3
U=20V
LV3
I=8A
V1
U=???
Aggregators
R=???
GND
HV6
U=100 V
R18
R=814
R19
R=1100
R20
R=1386
R21
R=1671
R22
R=1957
R23
R=1966
R24
R=1967
PSPP17
PSPP18
PSPP19
PSPP20
PSPP21
PSPP22
PSPP23
BP17
R=0.03
BP18
R=0.03
BP19
R=0.03
BP20
R=0.03
BP21
R=0.03
BP22
R=0.03
BP23
R=0.03
S17
S18
S19
S20
S21
S22
S23
M17
R=0.19 Ohm
M18
R=0.19 Ohm
M19
R=0.19 Ohm
M20
R=0.19 Ohm
M21
R=0.19 Ohm
M22
R=0.19 Ohm
M23
R=0.19 Ohm
C17
C=1 nF
C18
C=1 nF
C19
C=1 nF
C20
C=1 nF
C21
C=1 nF
C22
C=1 nF
C23
C=1 nF
Sensor17
Sensor18
Sensor19
Sensor20
Sensor21
Sensor22
RBias_17
R=10000
RBias_18
R=10000
RBias_19
R=10000
RBias_20
R=10000
RBias_21
R=10000
RBias_23
R=10000

Backup

- Comparison of FE performance in different setups



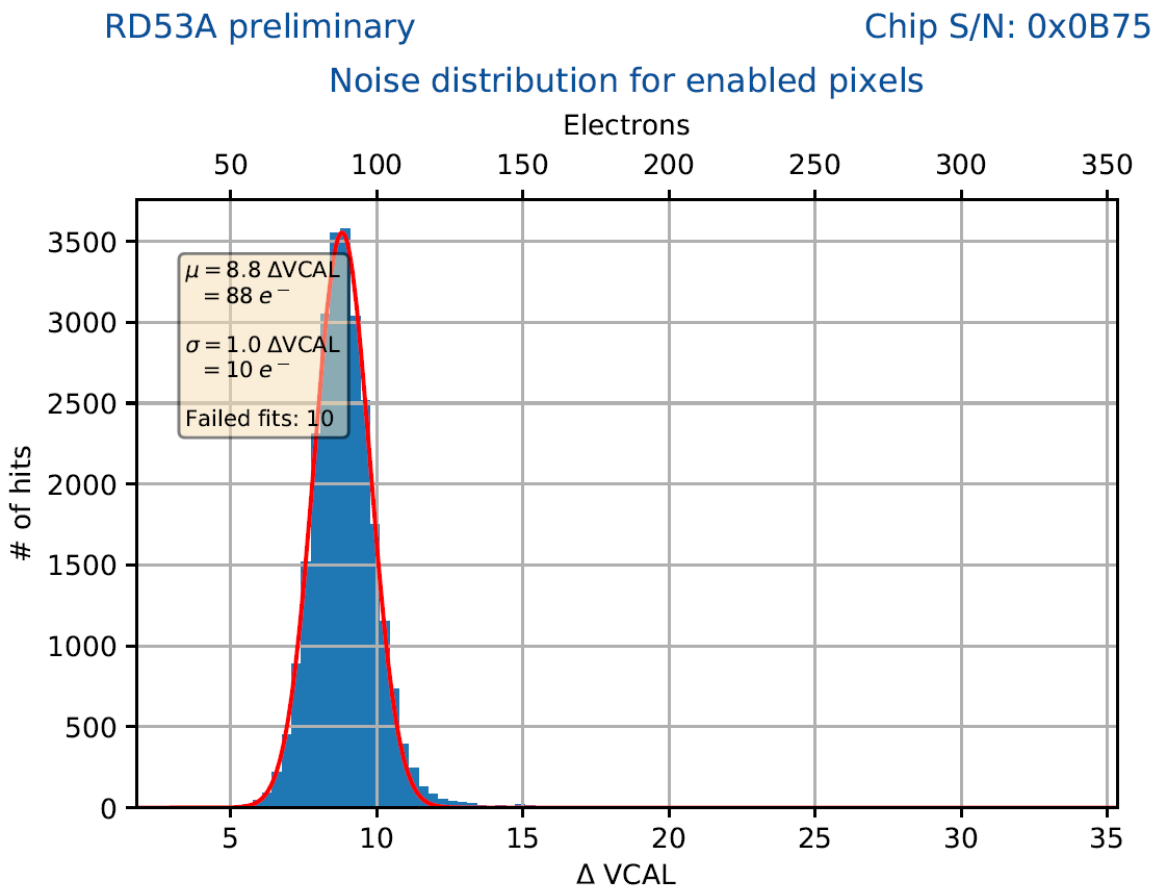
16x1



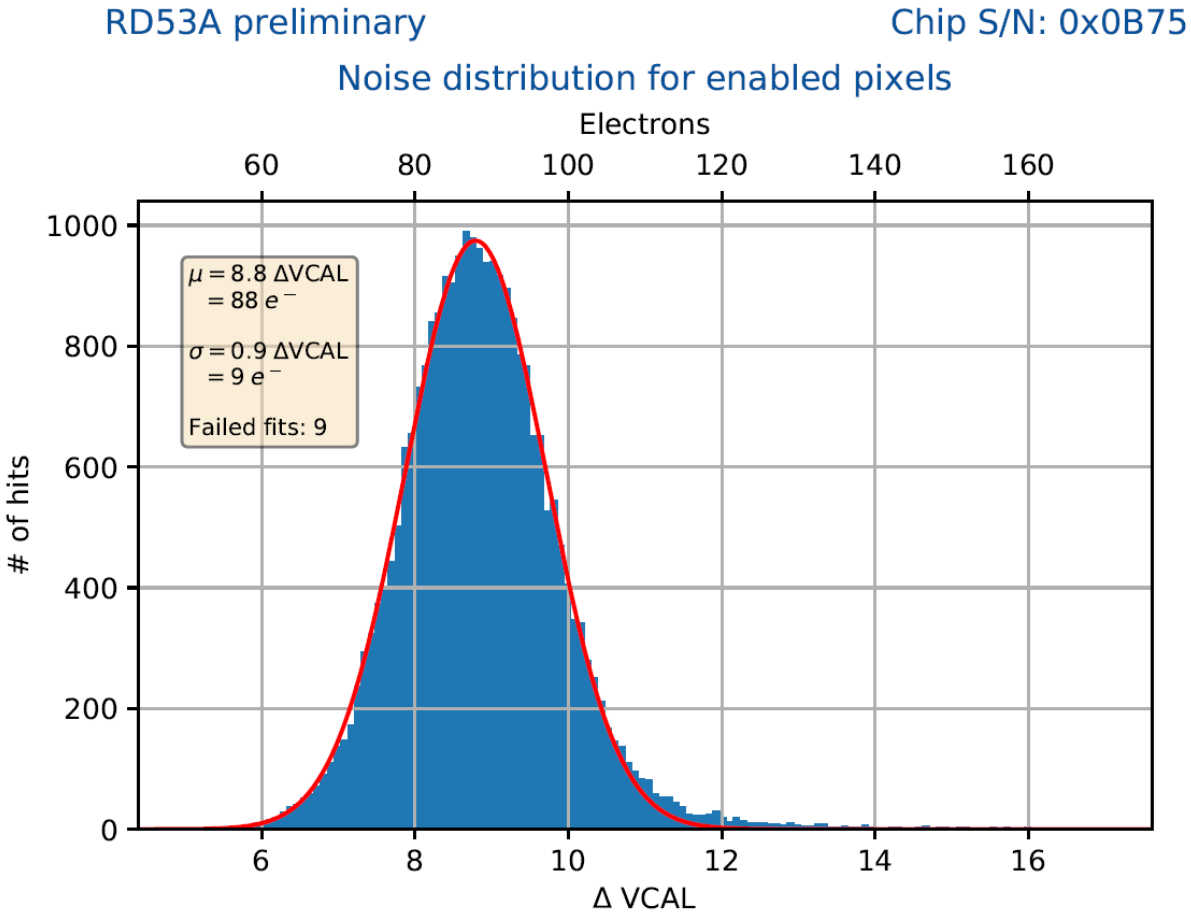
4x4

Backup

- Comparison of FE performance in different setups



16x1

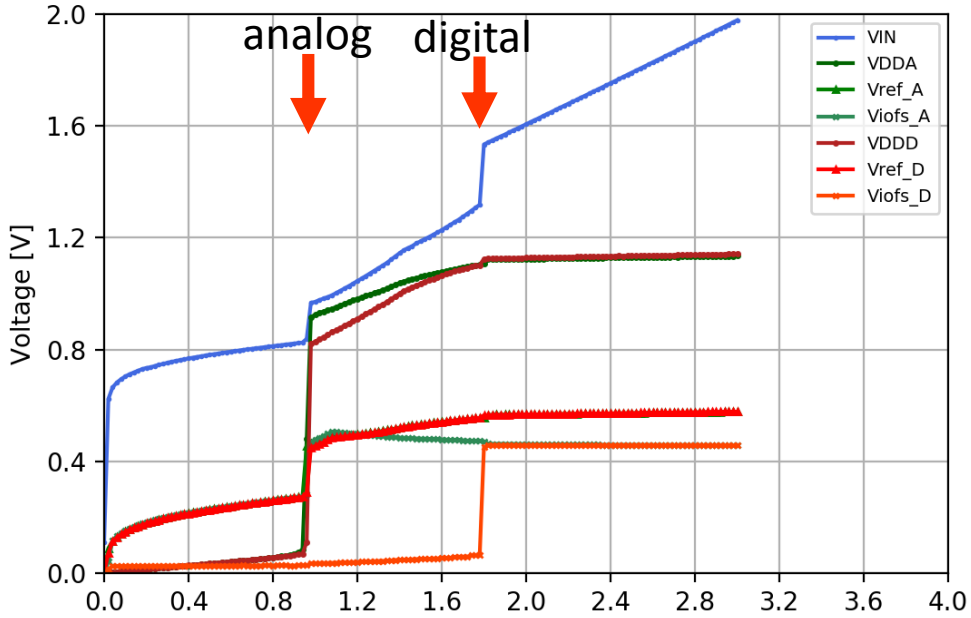


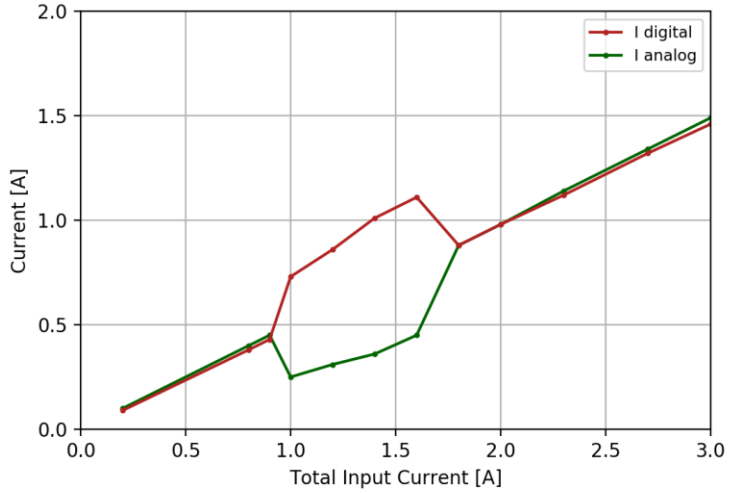
4x4

Line regulation - bandgap startup voltage

- Some bandgaps need higher V(I) to start up
- Seen with **different** bandgap voltages (VrefA, ViofsD, ViofsA)
  => Example of late digital Vofs shown here
- After bandgaps “started” dynamic range is good
- Unequal current sharing “*Eye*” possible:
  - When Vofs starts, SLDO gets into higher ohmic state

  => Jumps in current sharing

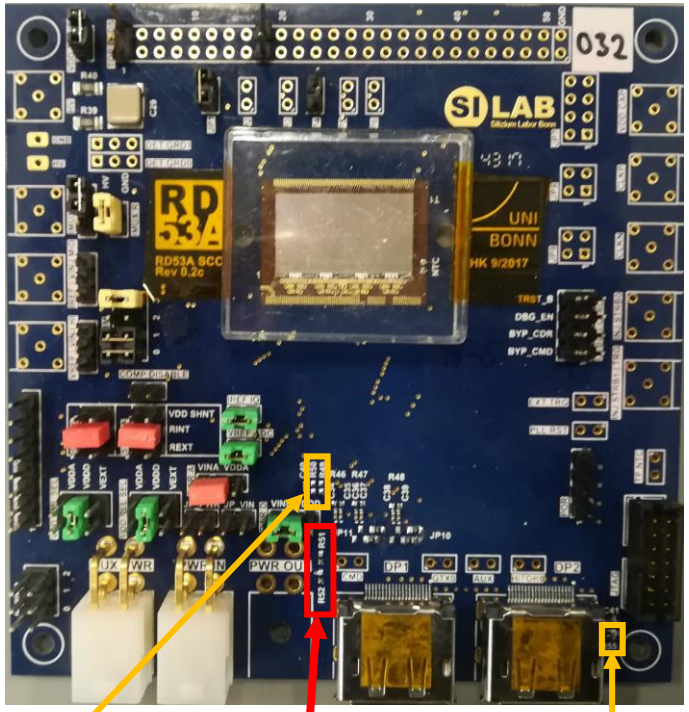




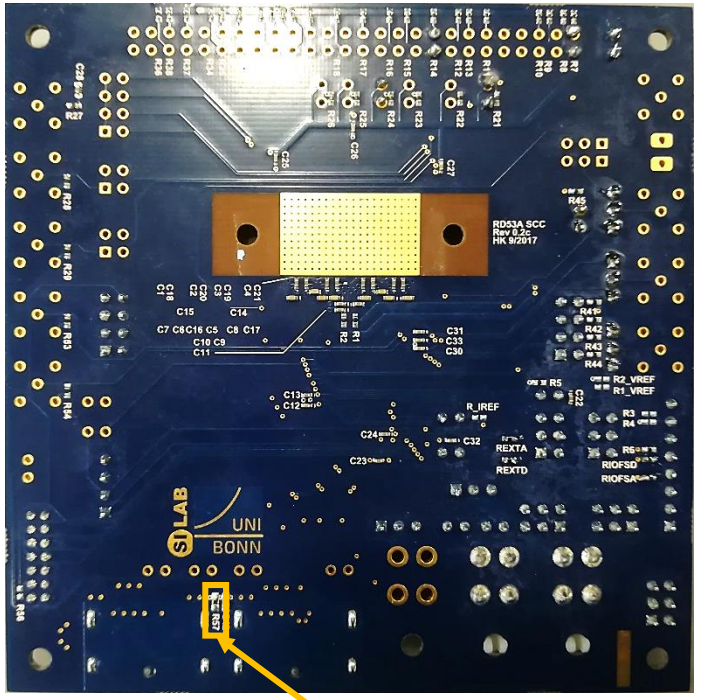
Important configuration for Serial Chains with SCC

For Serial Power Chains: **Remove** (0 Ohm) Resistors R49, R50, R51, R52, R55 and R57
=> otherwise DC-coupling (Grounding problem) through DP

SCC Top Side:



SCC Bottom Side:



R49 & R50
(For external reset signal (POR))

R55
(Connects Display Port Shield to PCB GND)

R57
(Connects Display Port GND to PCB GND)

R51 & R52
(For VDDD and GND Sensing through Display Port)

Is mounted on all SCCs by default

Filter capacitors on SCC

Default configuration:

- Each regulator:
  - Cin=4x10uF, Cout=4x2.2uF
  - Cvofs = 100nF
  - Cvref = 100nF

- Plus C for VDD_PLL (2.2uF) and VDD_CML (4.4uF)
  - VDD_PLL & VDD_CML connected to VDDA

- More than required by design!

=> Change capacitors for SLDO transient studies:

- Shared input Cin_total = 6uF
- Per regulator output Cout = 2.2uF
- Remove 100nF capacitors for Vofs, Vref (each regulator)