
CERN

picoTDC:
Pico-second TDC for HEP

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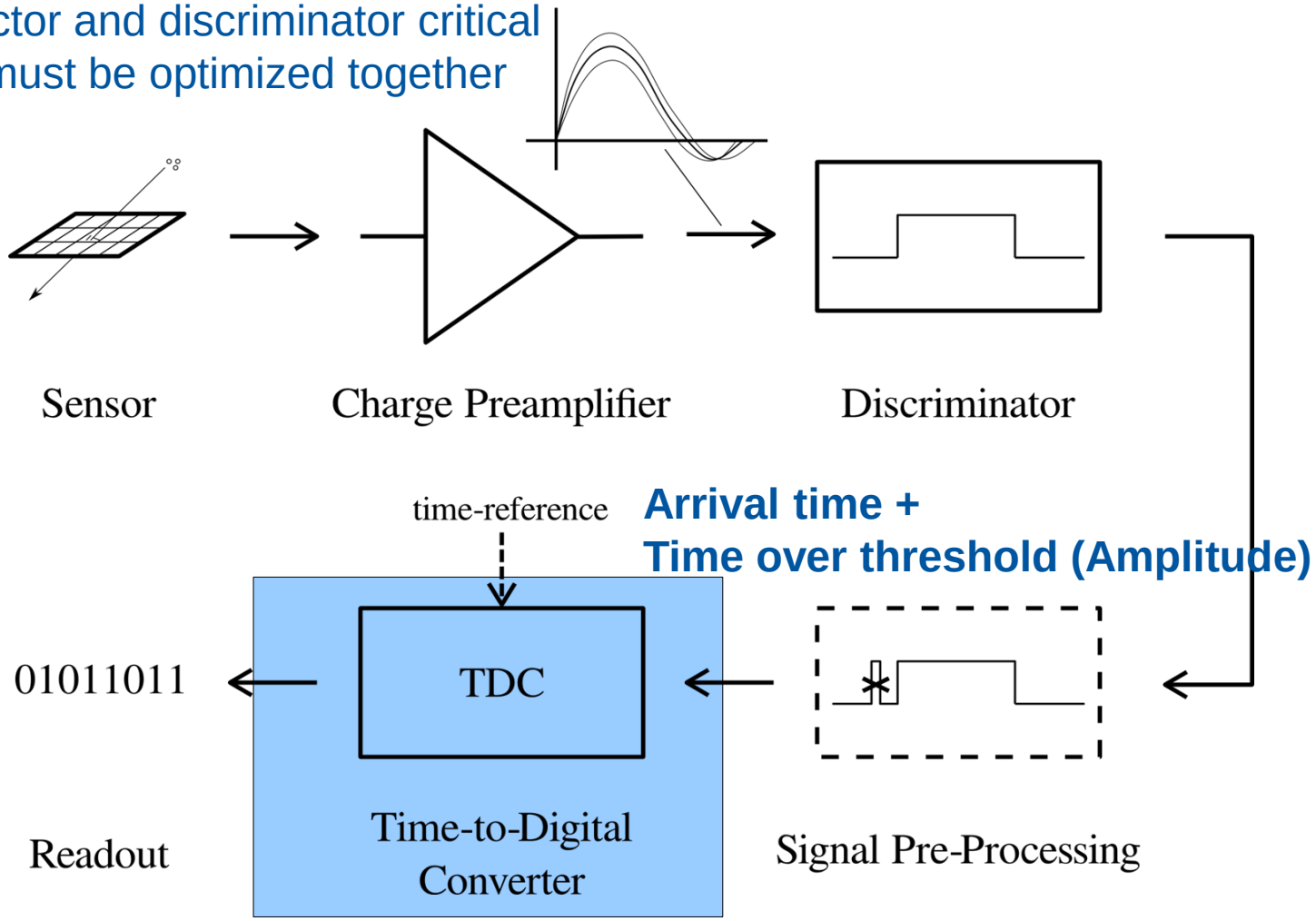
CERN/EP-ESE

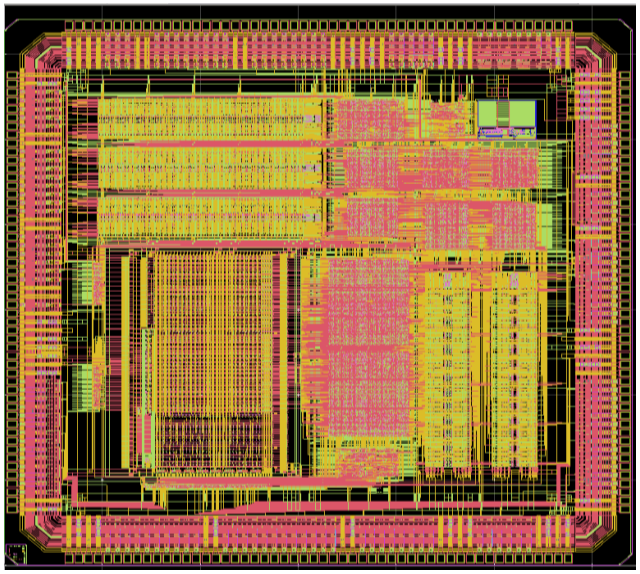
TDC in the Measurement Chain

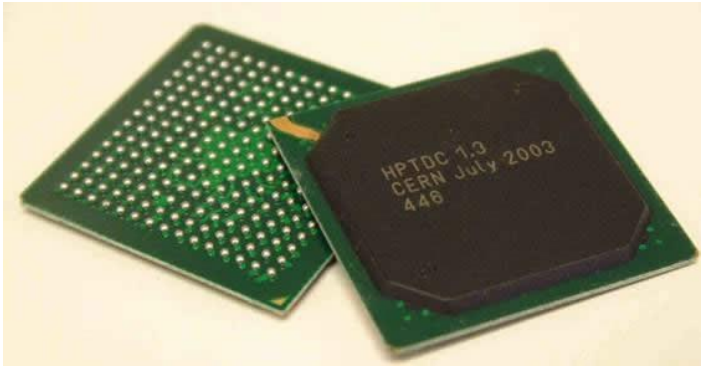
Detector and discriminator critical and must be optimized together



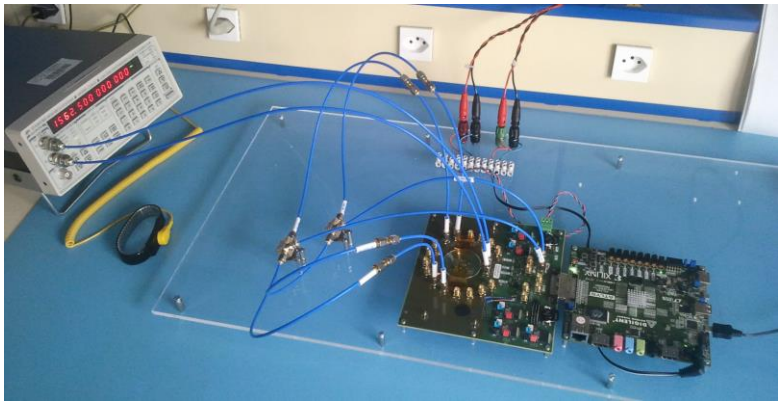
Why a New TDC?

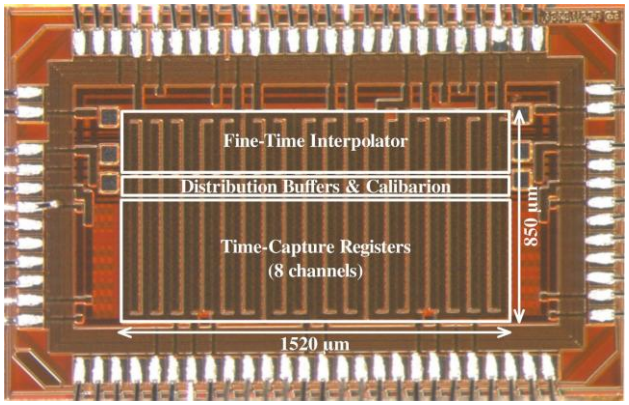
- HPTDC
  - 32 channels (100ps binning), 8 channels (25ps binning)
  - More than 20 HEP and other applications: ALICE TOF, CMS muon, CAEN …
    - We still supply chips from current stock, running out
  - ~50k chips produced, can not be produced anymore
- New applications demand higher resolution and/or integration





TDC Architecture Prototyped in 130nm



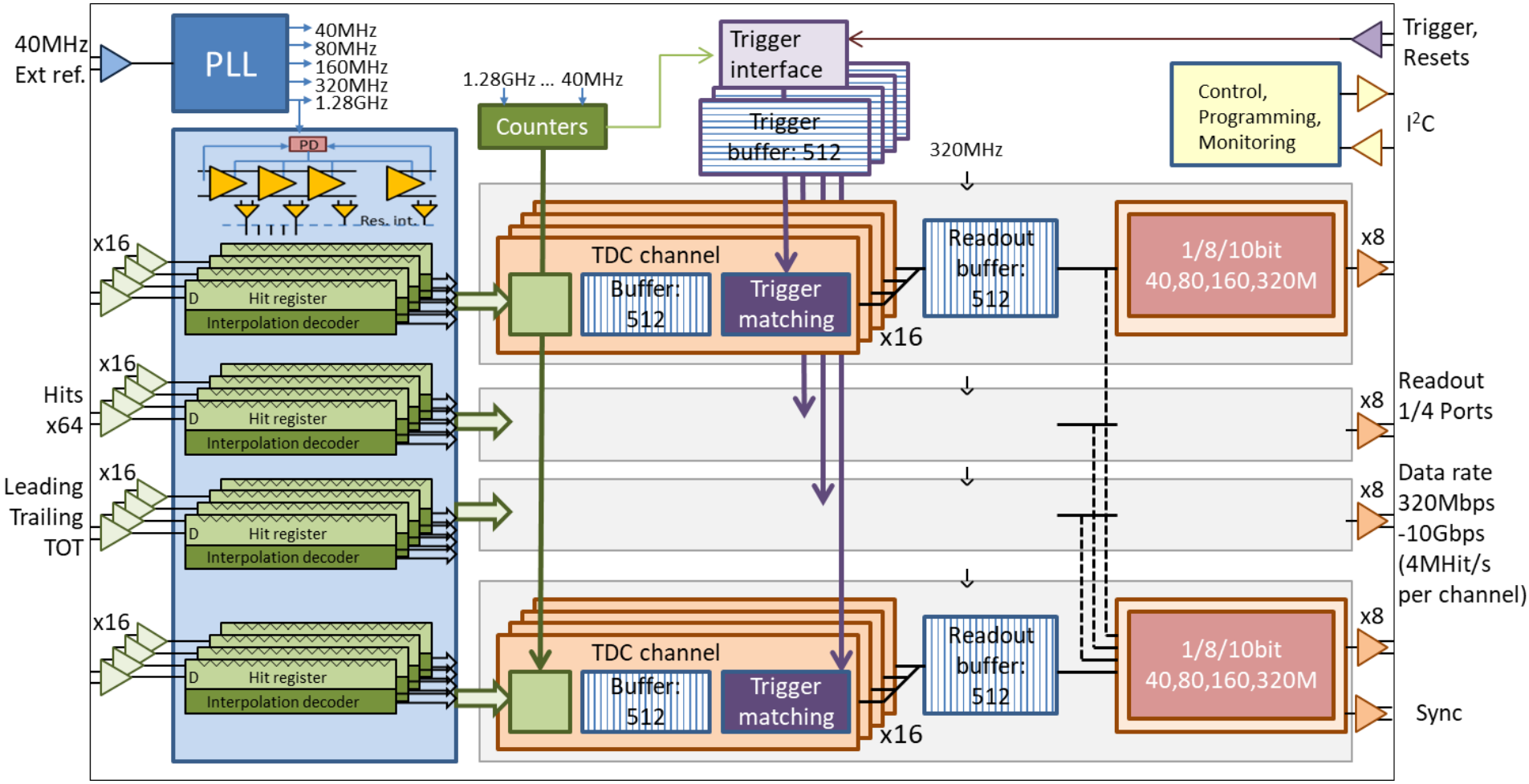


- External time reference (clock)
- Serial readout of capture register
- 3 stage time measurement:
  - Counter: 800ps, Delay locked loop: 25ps, Resistive interpolation: 6.25ps
- Measured performance: ~4ps RMS @ 6.25ps bins
- Design: Lukas Perktold

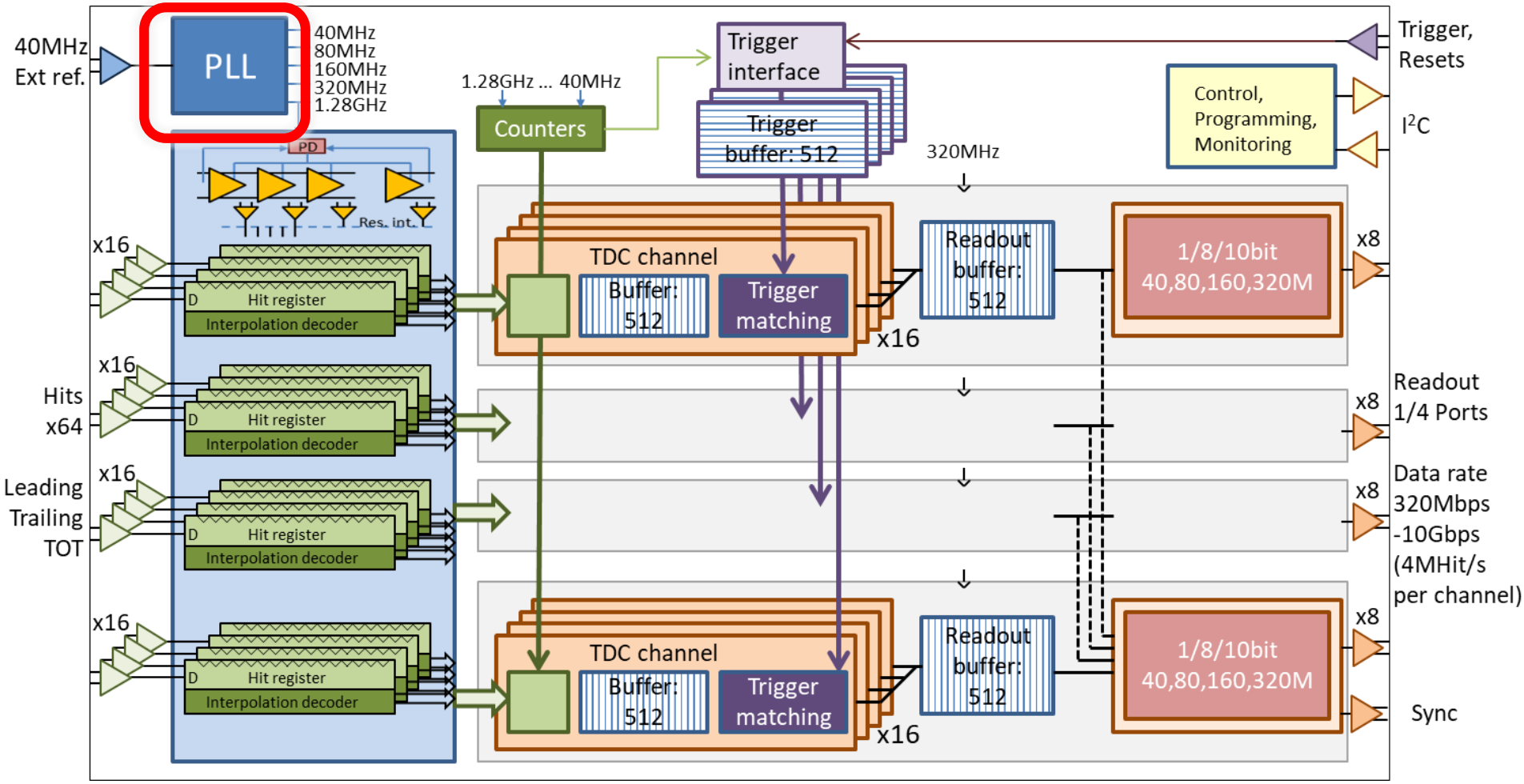
Mapping to 65nm

- Uncertain long term availability of IBM 130nm (now Globalfoundries)
- 2x time performance: -> 3ps binning
- Lower power consumption: < ~½
  - ~1/8 if DLL binning of 12ps enough (RMS ~4ps)
- Larger data buffers
- More channels
- But higher development costs

picoTDC Architecture

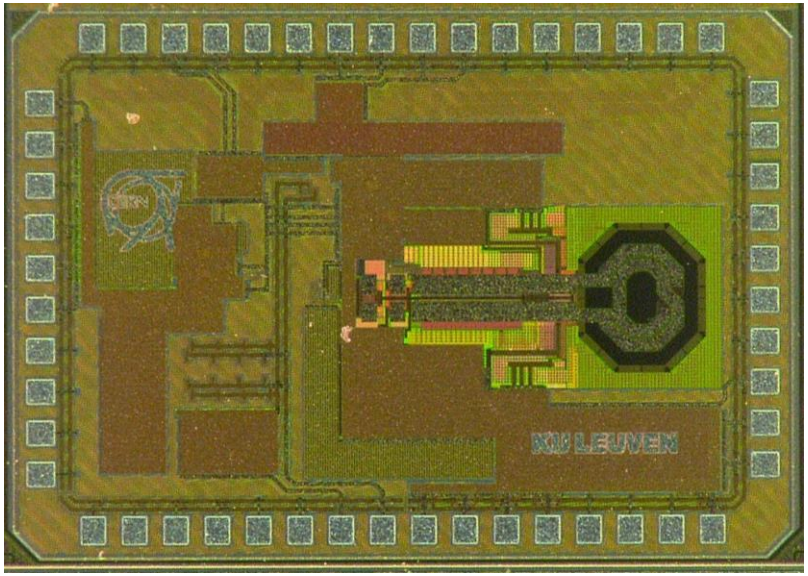


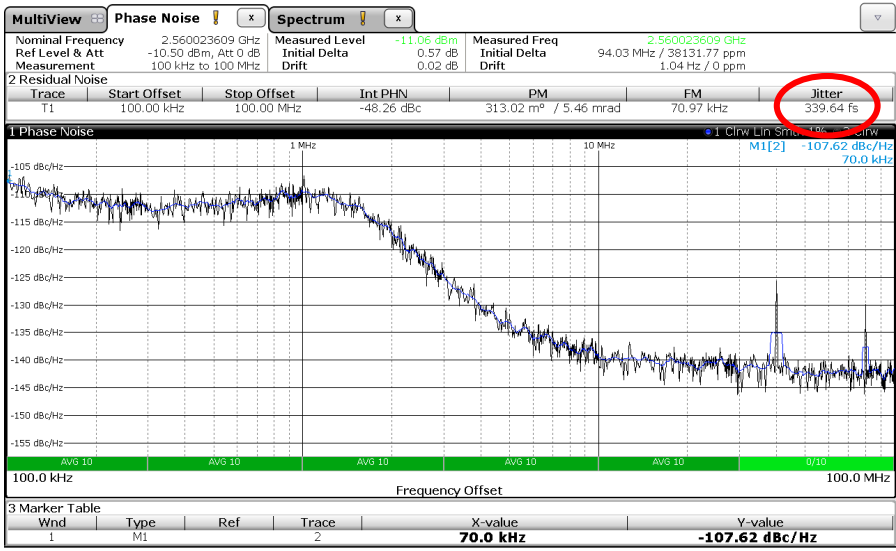
picoTDC Architecture



Low Jitter PLL

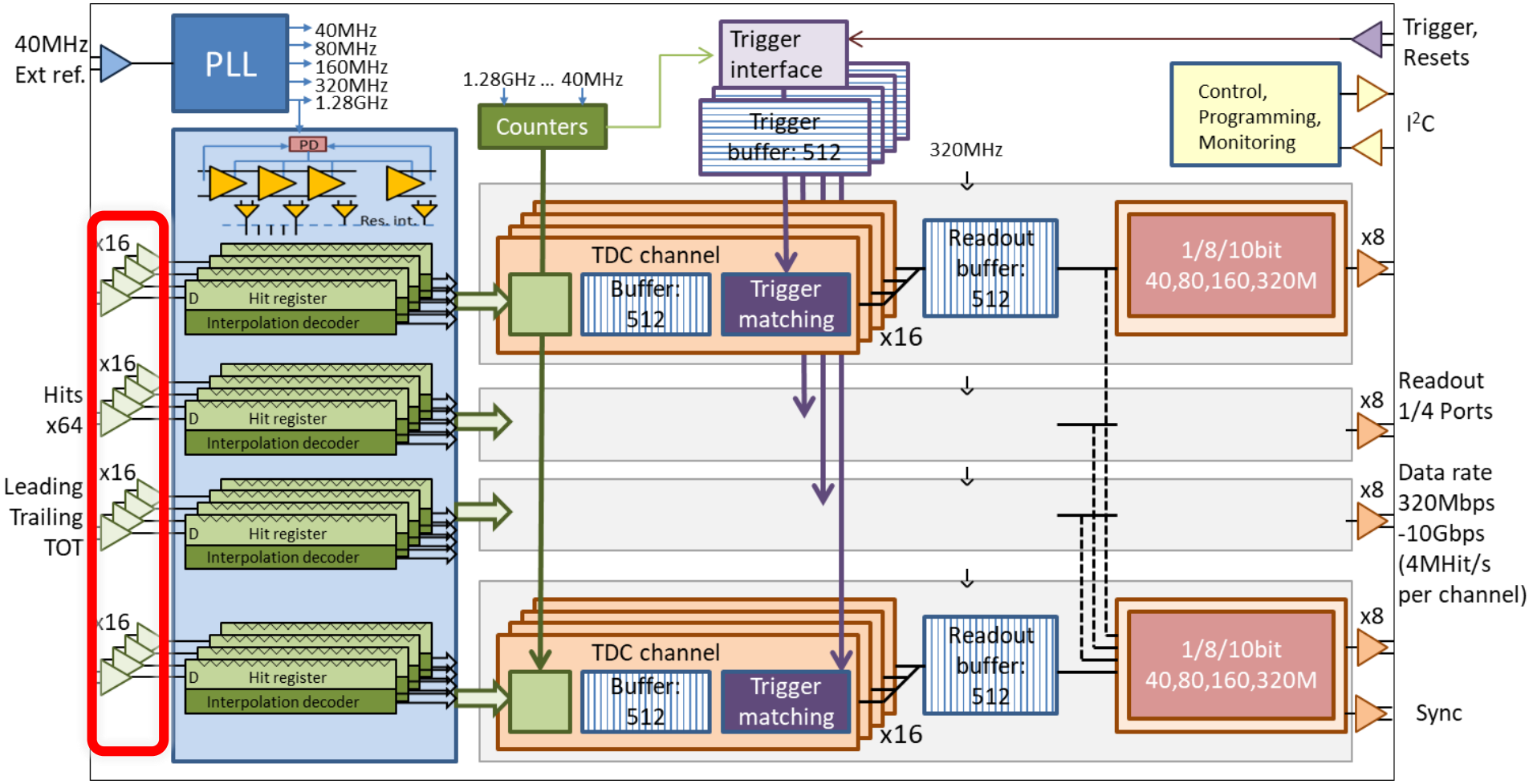
- Clock multiplication from 40MHz to 1.28 (2.56) GHz
  - Low jitter critical
  - Jitter filtering of 40MHz clock to the extent possible
    - 40MHz reference MUST be very clean
  - LC based oscillator
- Design: Jeffrey Prinzie, KU Leuven
- Prototyped & Tested
- Measurements very promising (340fs RMS jitter)





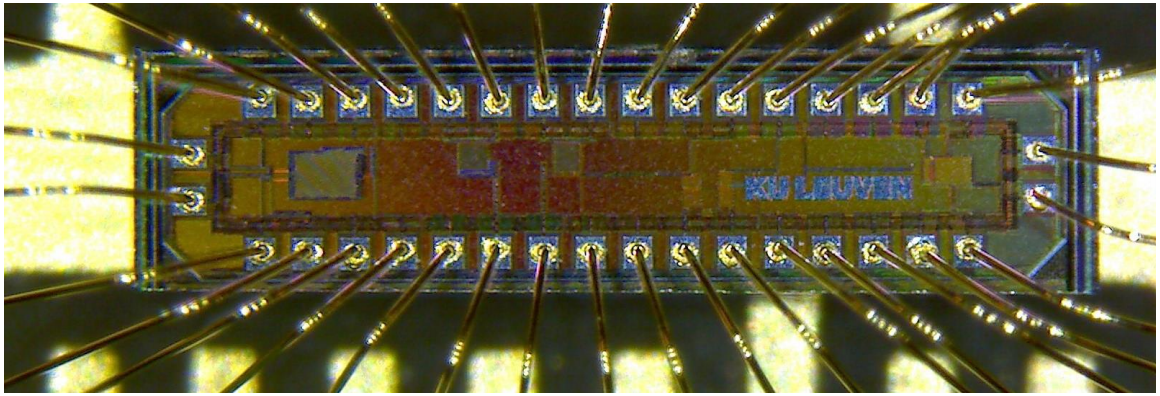
Phase Noise vs. Freq. Offset

picoTDC Architecture

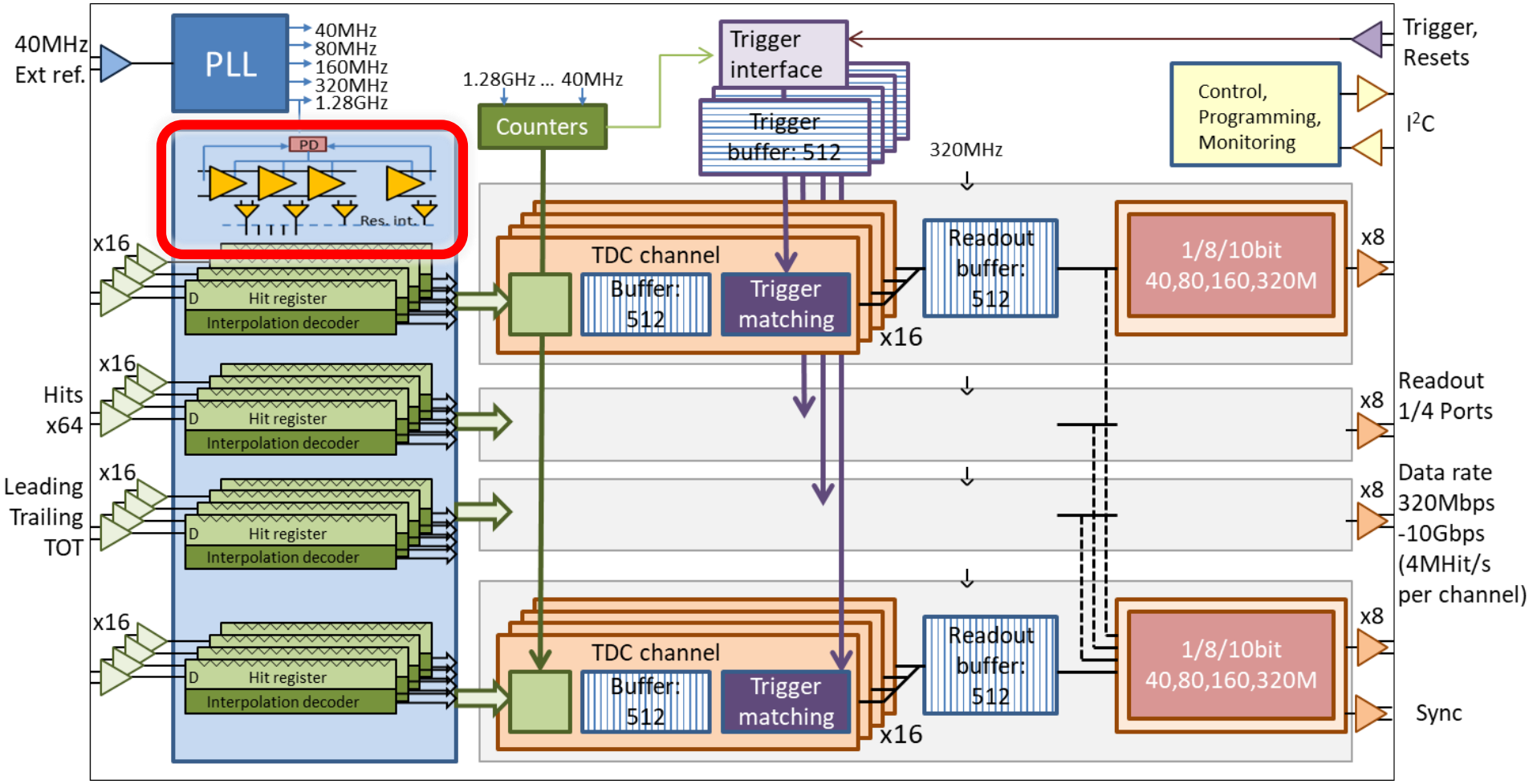


Hit Receivers

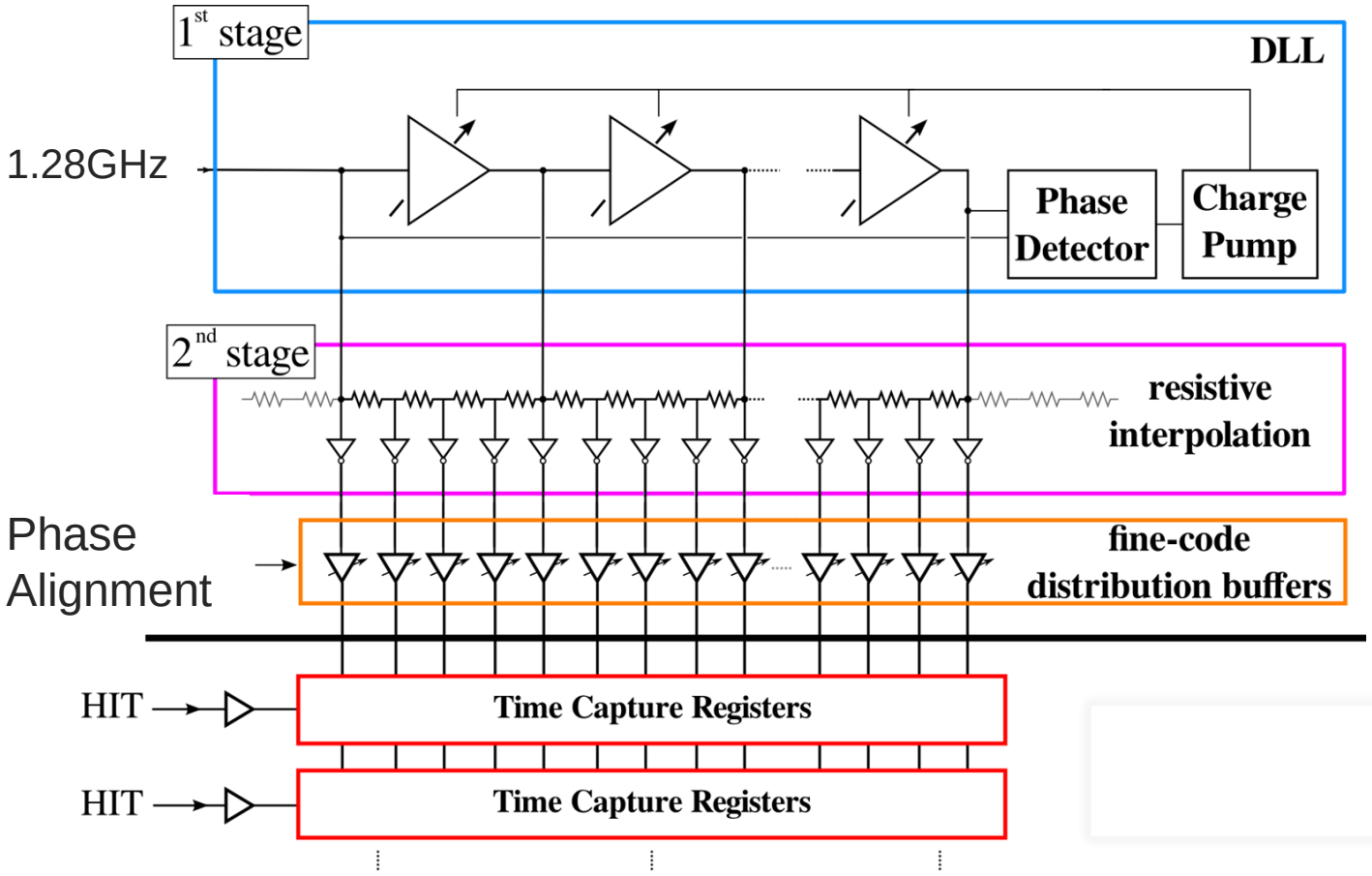
- Differential receivers optimized for ultra-low jitter, low power
- Full Range (common mode 0V .. VDD=1.2V), somewhat LVDS-compatible
- Highest speed @~800mV common mode
- Optimized for 200mV Peak-Peak amplitude
- Design: Bram Faes, KU Leuven
- Prototyped & tested



picoTDC Architecture



Two Stage Time Interpolation



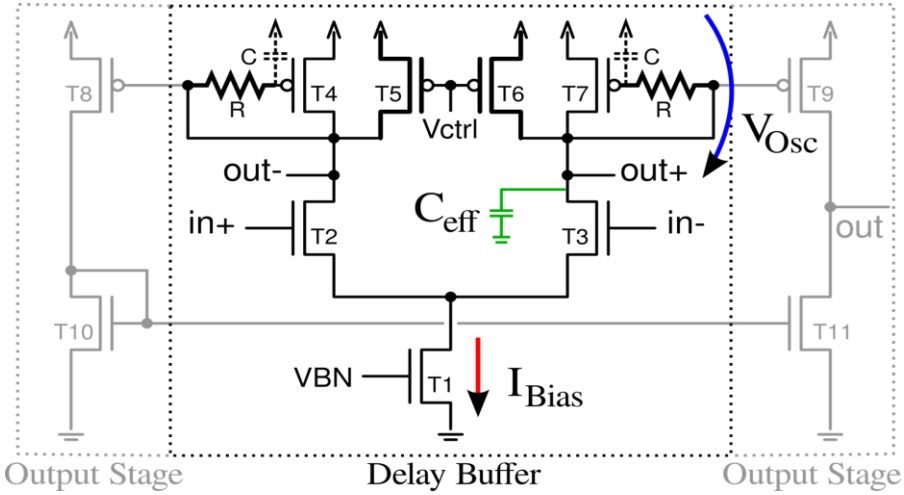
12.2ps delay

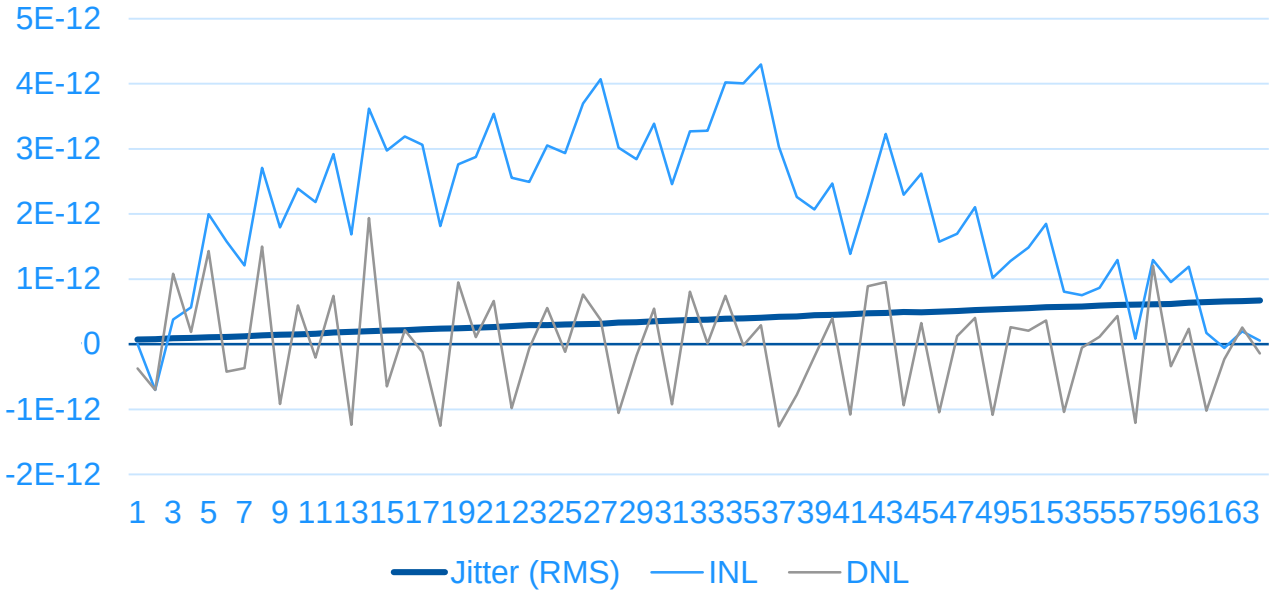
3.05ps delay

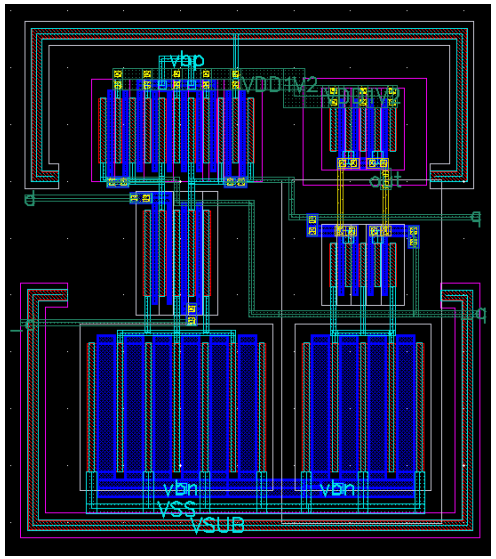
32 steps each with 0.7ps resolution

1st Stage: DLL

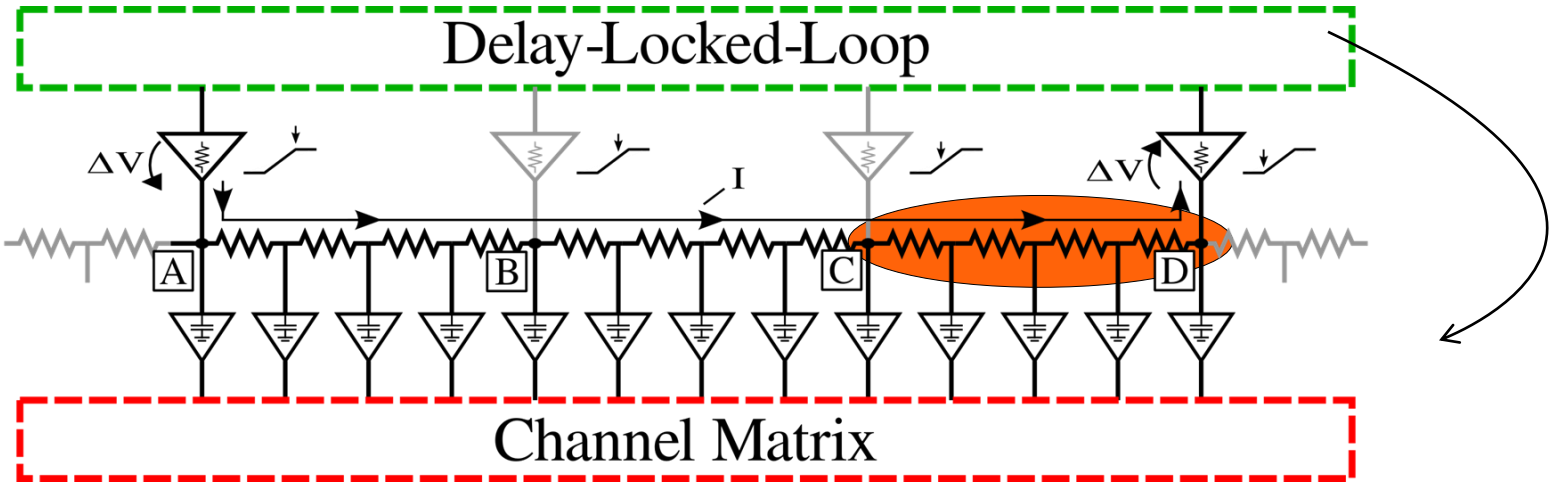
- 64 taps, 12.2ps delay
- Self-Calibrating
- Jitter not as critical, doesn't pile up

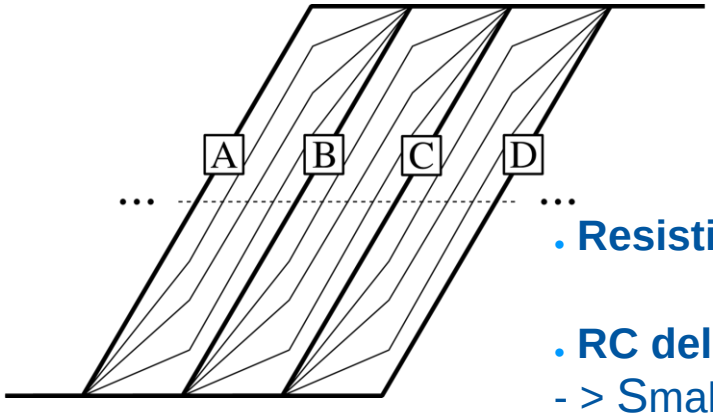


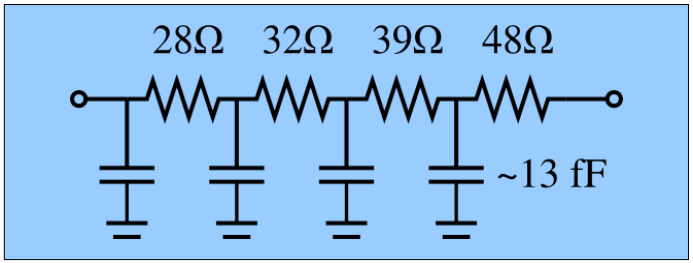




2nd Stage: Resistive Interpolation





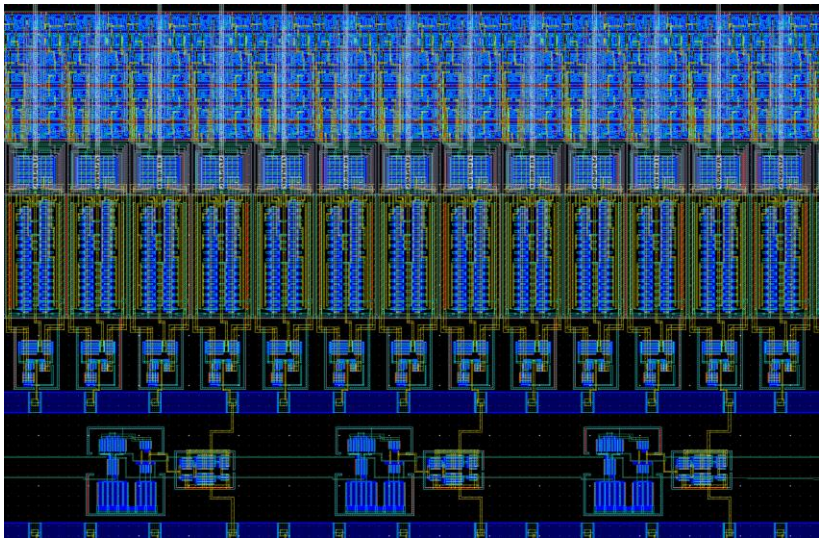


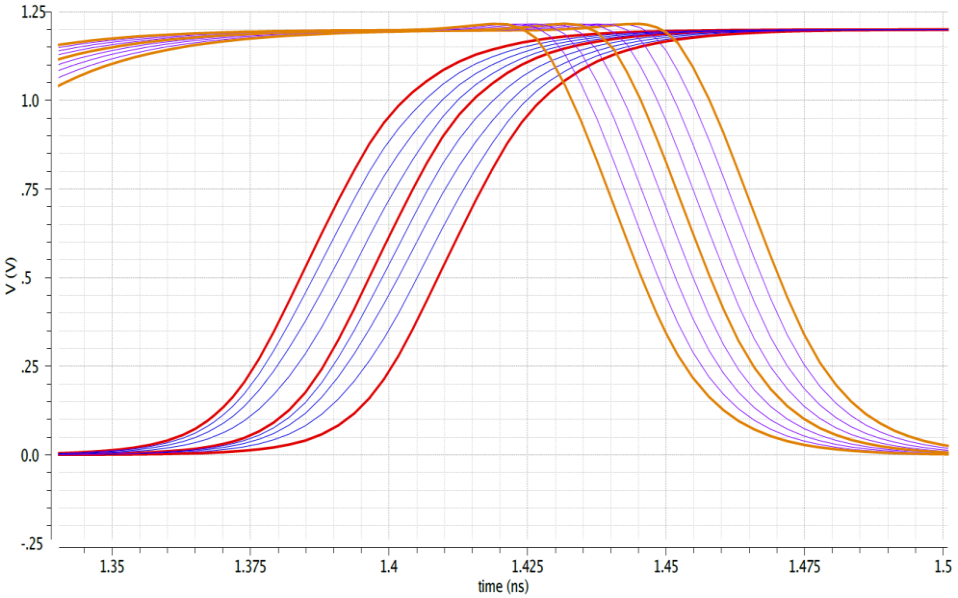
- **Resistive voltage divider**
  -> Signal slopes longer than delay, stabilized by DLL
- **RC delay** (capacitive loading)

- > Small resistances, small loads
- > Simulation based optimization of resistor values

Finecode Drivers and Alignment

- Get down to 3ps bins
- Drivers: tapered buffers, each driving 32 FFs
- Phase alignment separate for each half





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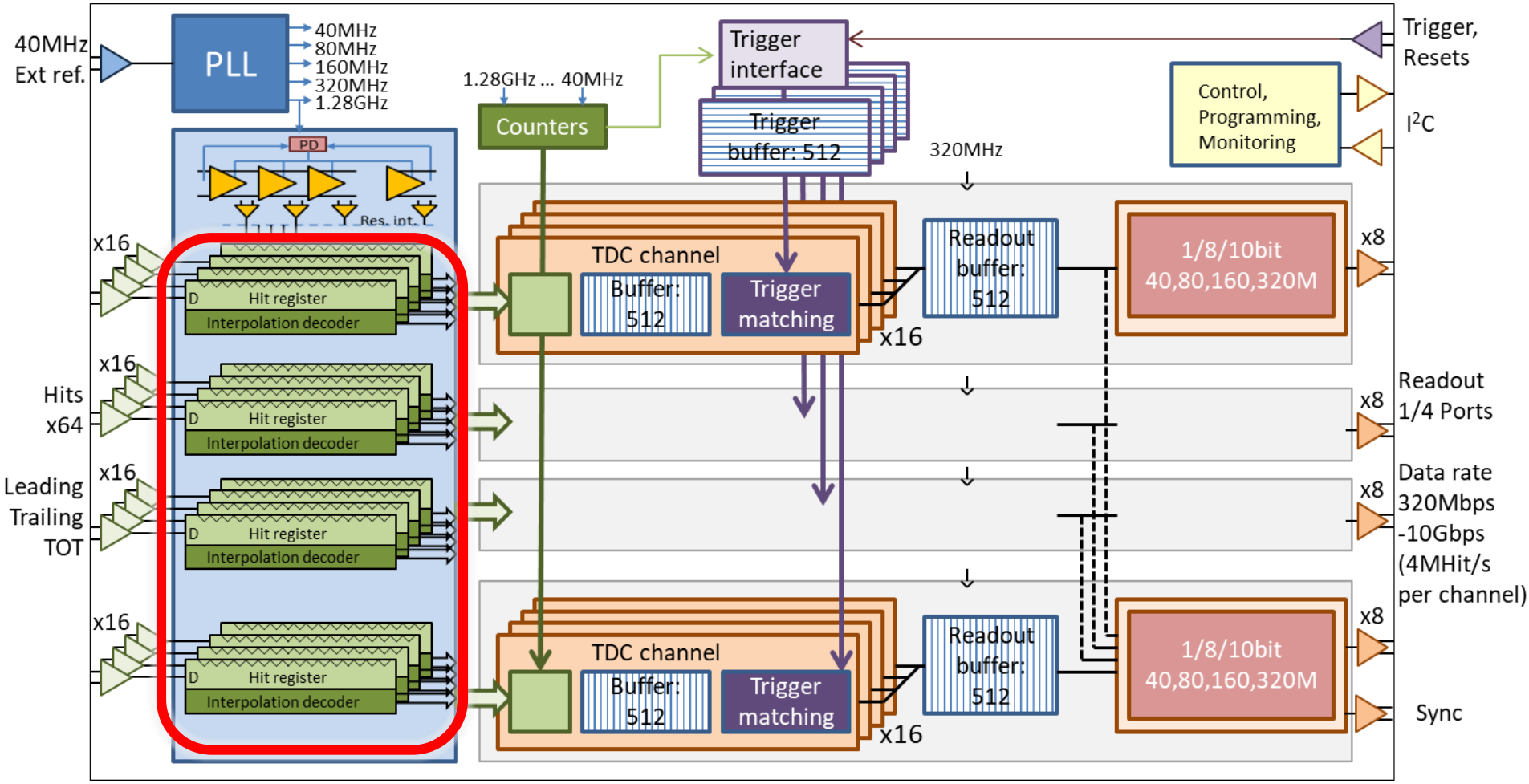
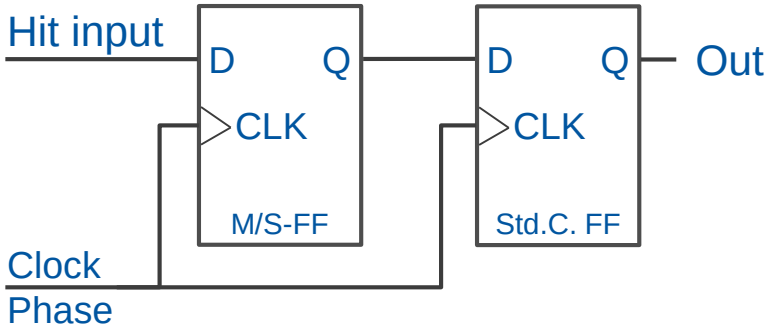
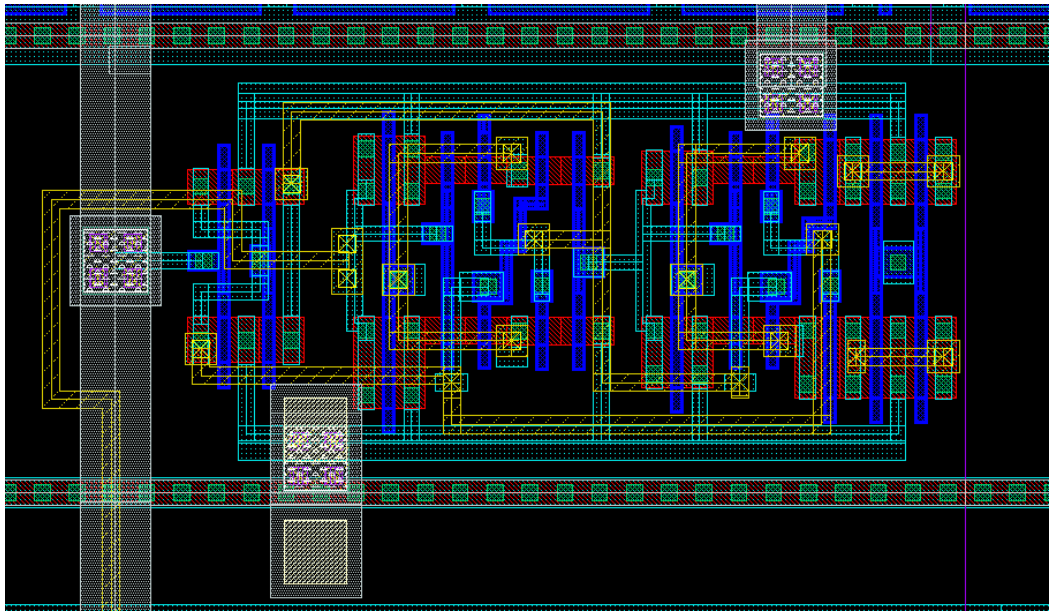


Capture Flip Flops

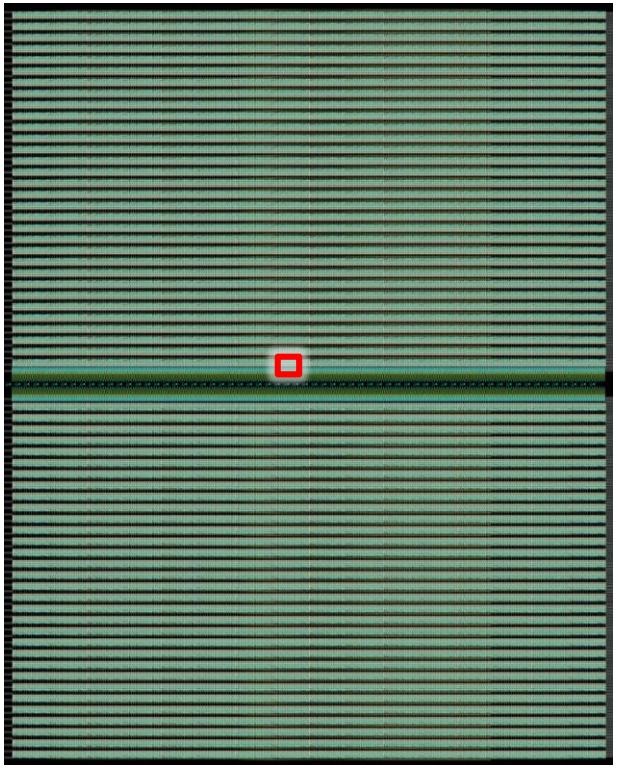
- Revisited design, timing vs. power very critical, 16k capture Flip Flops running @1.28GHz
- Highly optimized M/S Flip Flop followed by standard cell Flip Flop for metastability resolution
- Monte Carlo simulations show a mismatch of 800fs RMS, noise influence of 240fs RMS

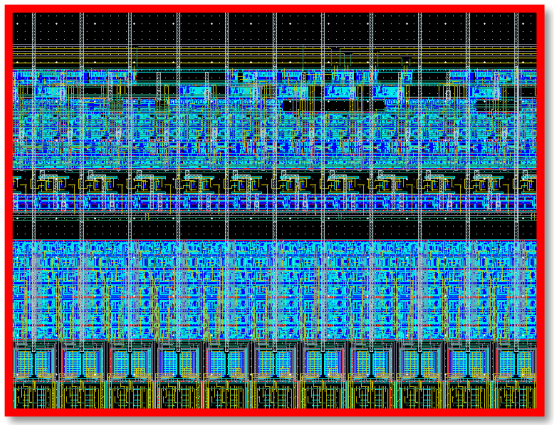




Full Timing Macro

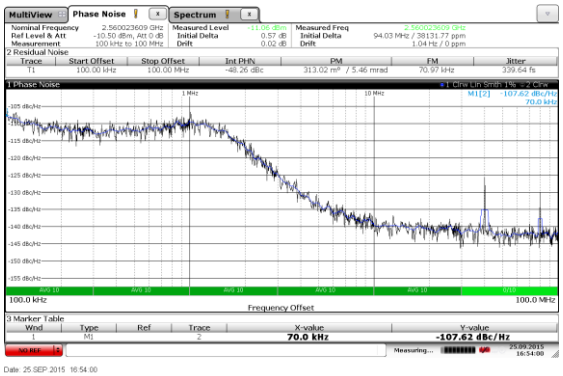
- 64 channels, DLL and resistive interpolator in the center
- Hit signal input on the left, output on the right
- Hit decoding fully synchronous, custom layout with standard cells
  - Decoding of one hit per 0.8ns
- 1.6mm x 2.0mm

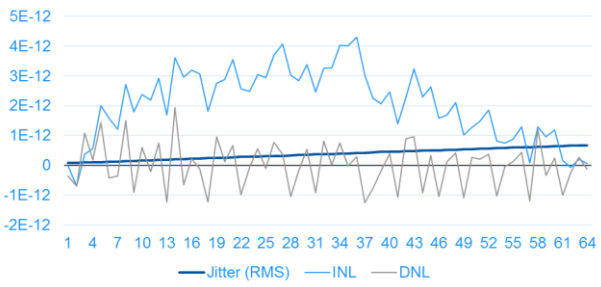


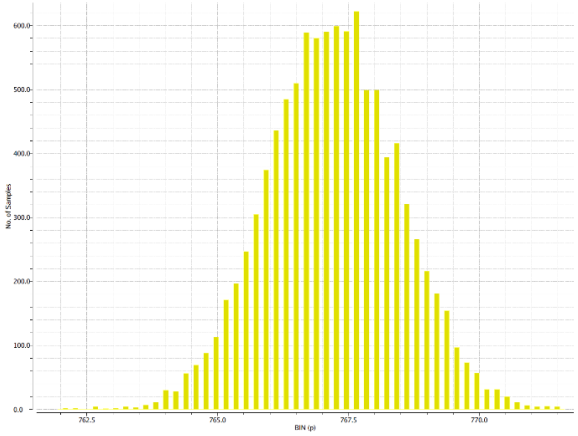


Sources of Measurement Deviation

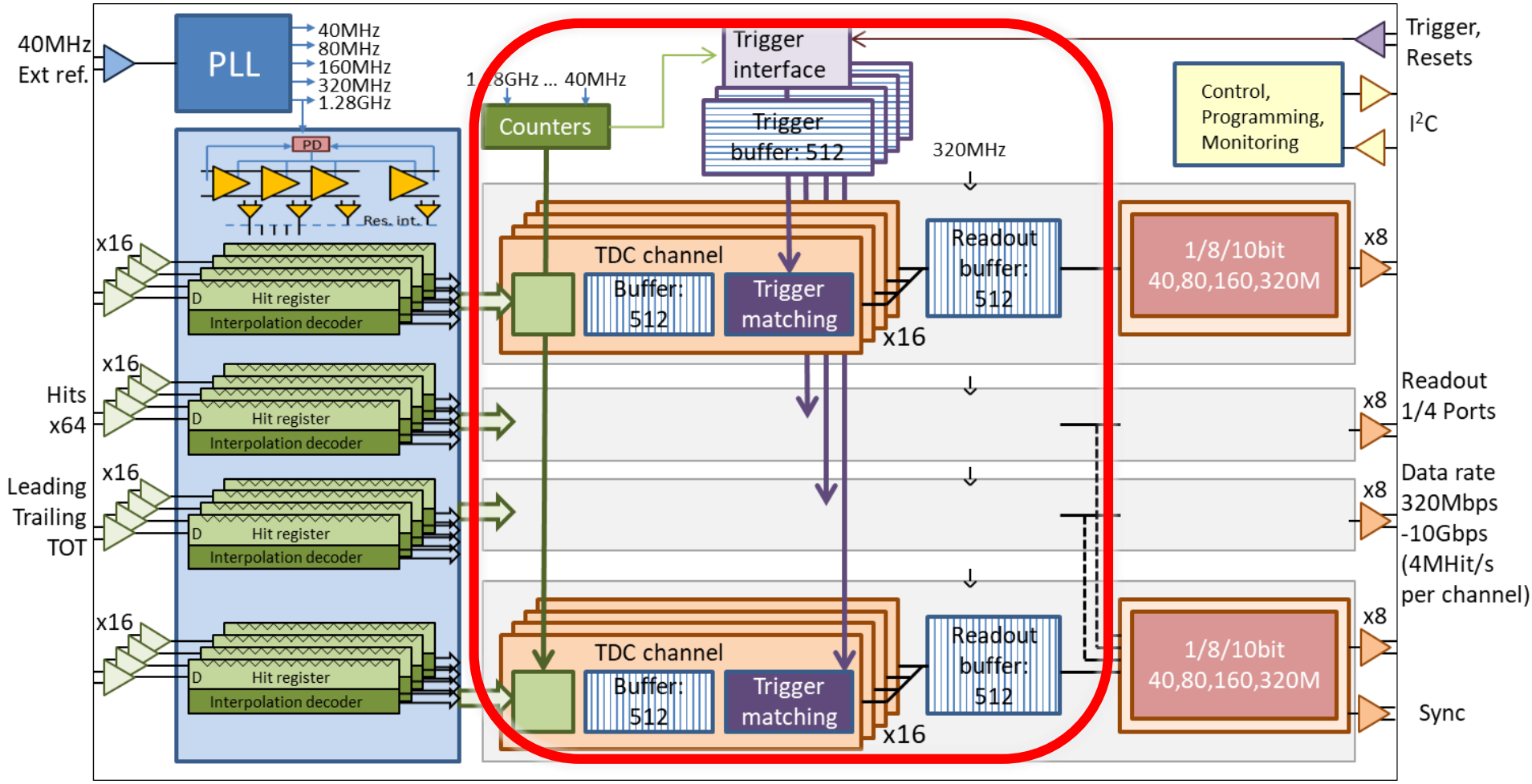
- Bin size 3ps -> 880fs RMS
- PLL: 350fs RMS phase Jitter
- DLL: 400fs RMS phase Jitter, INL/DNL can be adjusted
- Clock Distribution: <500fs jitter
- Capture FFs: <1ps mismatch (DNL)
- Hit receivers: <1ps jitter
- ➢ ~1.75ps RMS total deviation
- External sources: input clock jitter, signal preprocessing







picoTDC Architecture



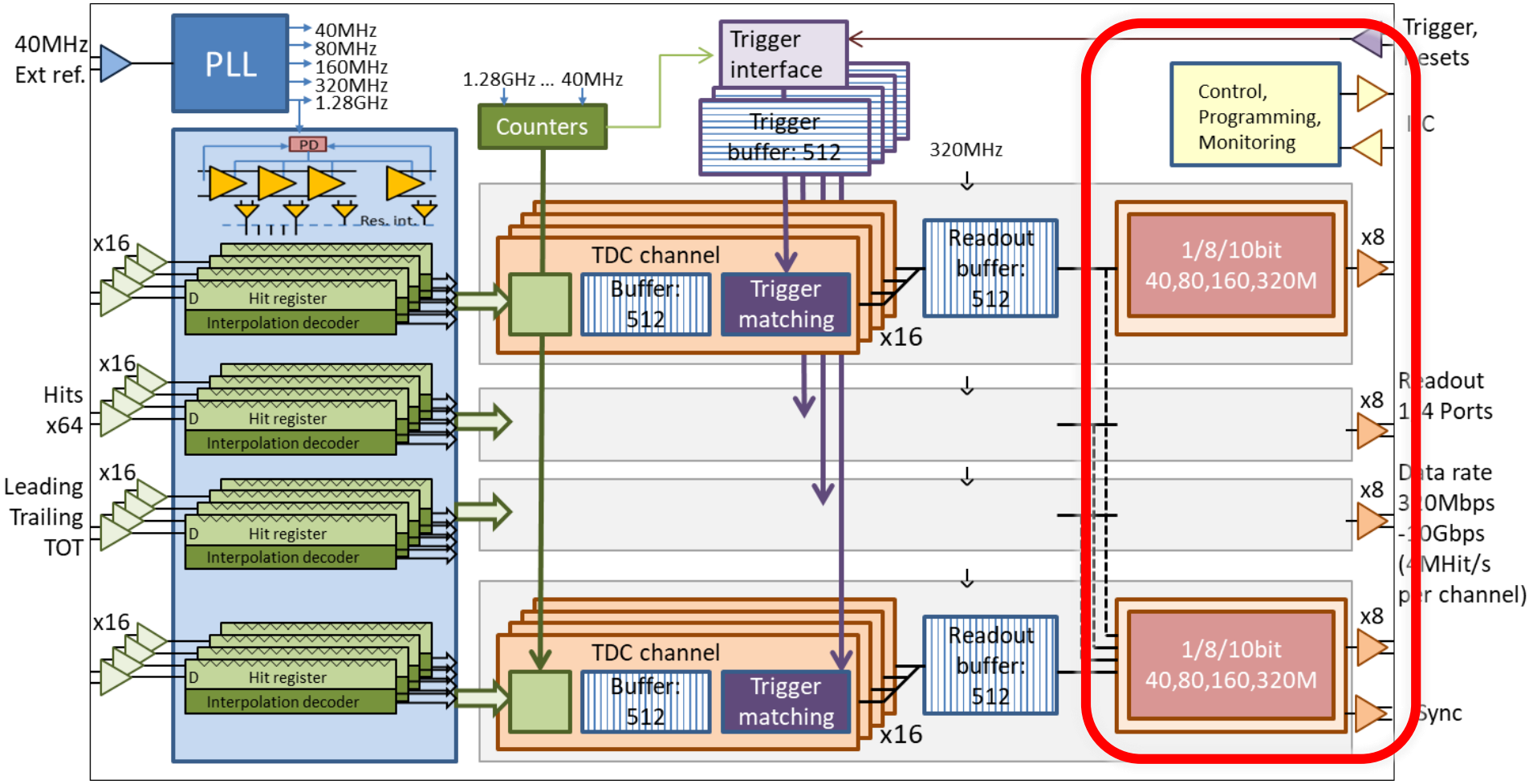
Constraints on Hit Signals

- One edge per 1.28GHz-Cycle (~0.8ns)
- Internal analog glitch filter after hit receiver
  - Filter time can be programmed to ensure 0.8ns
  - Or up to 10ns for filtering e.g. oscillations
- Small derandomizer (4 hits) for each channel running @1.28GHz
- Sustainable rate to channel buffer 320MHz, trigger matching running @320MHz for each channel separate

Logic Features

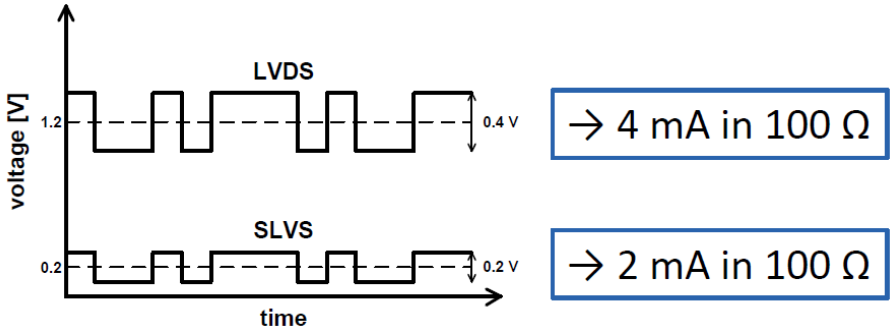
- Triggered with configurable latency and length, overlap possible, or untriggered
- Naturally overflowing counter used for calculating trigger matches, TOT etc.
- Counter with arbitrary overflow and reset for machine cycle, can be inserted in event headers when triggered

picoTDC Architecture



Electrical Interfaces

- Hits: Differential (LVDS “compatible”, common mode from 0.2V to 1.2V)
  - Highest speed (resolution) @ ~800mV common mode
- Time reference: 40MHz differential
  - Low jitter reference critical for high time resolution
- Trigger/Event-Rst/BX-Rst/Reset: Sync Yes/No
- Control/monitoring: I^2C at CMOS 1.2V-levels
- Readout: 4 readout ports of 8 differential signals
  - Common mode 0.6V, programmable current 1-5mA
  - Compatible with LpGBT and FPGAs
- Packaging: 400 BGA (1mm pitch)



Config / Control / Status Interface

- I^2C Interface, up to 1MBit/s
- 1.2V CMOS Levels
- 348 Bytes configuration / control
  - Additional 322 bytes delay adjust
- 300 Bytes status

Readout

- 1 or 4 differential readout ports with 8 bits
  - 40 - 320MHz
  - Bandwidth:
    - Min 320Mbits/s (~0.15 Mhits/s per channel)
    - Max 10Gbits/s (~4 Mhits/s per channel)
- Readout data: 32 bit words
  - TDC data, headers, trailers etc.

32 Bit Frames

TDC measurement

Event headers (up to two)

Possible fields: Event ID, Bx ID, Natural ID

Event trailers

Channel group separator (for single readout port)

Idle frame

Absolute TDC data

FULL TDC data, **DEFAULT FORMAT**

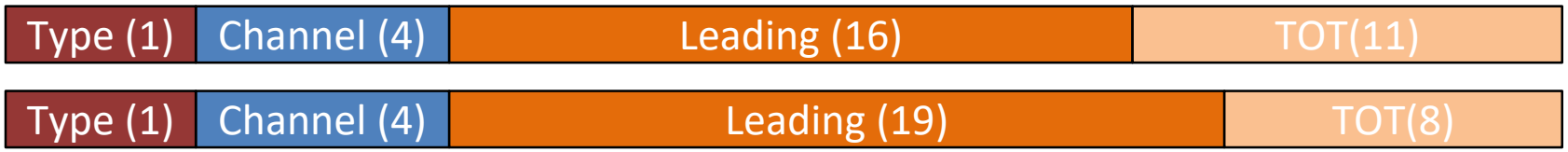
Relative to Trigger

Triggered with relative time: Same as absolute

B: Triggered with relative leading and TOT: Same as absolute Lead. + TOT

Leading + TOT

- Packet Type: 1bit
- Channel ID: 4 bits, for single port readout +2 bit group separator
- Leading: 16/19 bits
  - Large dynamic range
    - 16bit 3ps resolution: 200ns
    - 19bit 3ps resolution: 1600ns
  - **Programmable part of full 25bits leading TDC**
  - (**Relative to trigger to be useable**)
- TOT (Relative to leading): 11/8 bits
  - Short dynamic range:
    - 8bit 3ps resolution: 780ps
    - 11bit 3ps resolution: 6.1ns
  - **Programmable part of full 25bits TOT difference**
    - TOT assumed to be used for offline time-walk correction of leading.
- Alternative: Readout of Individual Leading and Trailing edges with full range/resolution
  - 2x readout bandwidth

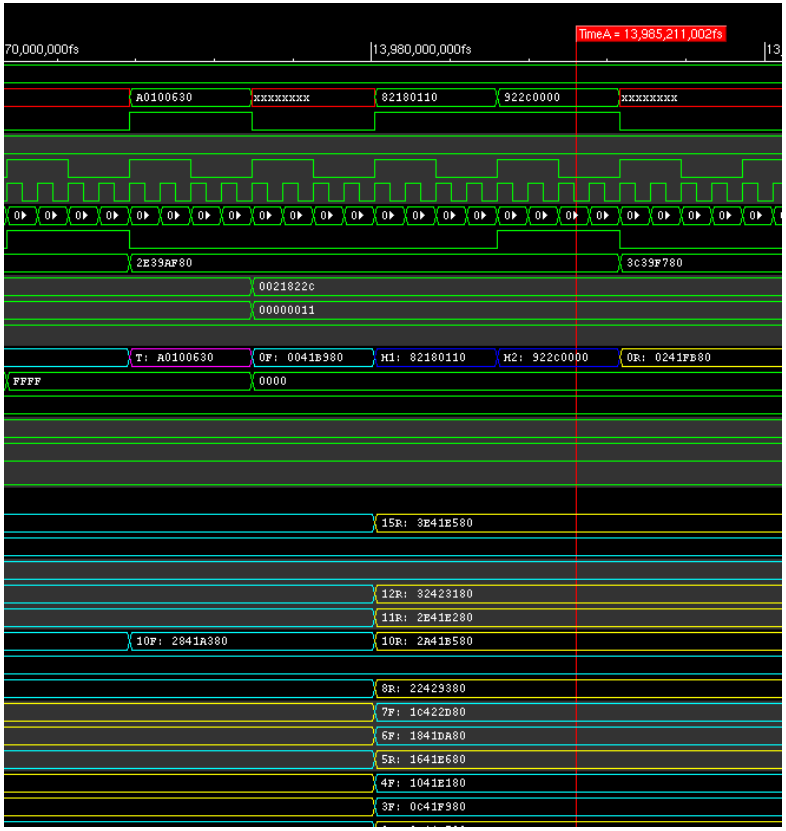


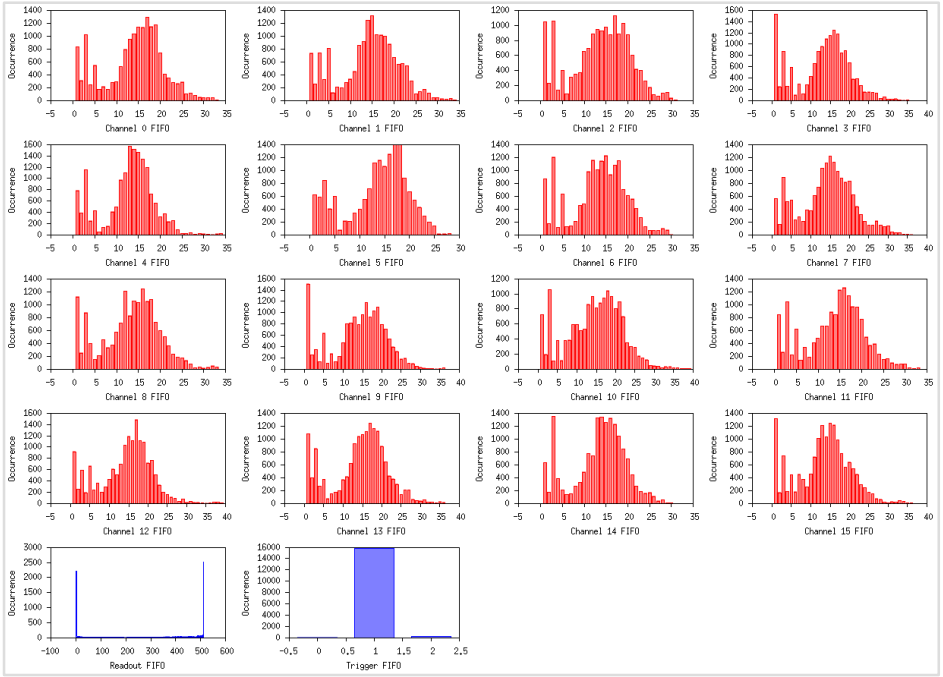
Estimated Power Consumption

Highly dependent on hit rate, values based on 1 MHz per channel

- High resolution, 64 channels: 1300mW
- High resolution, 32 channels: 900mW
- Low Resolution, 64 channels: 850mW
- Low Resolution, 32 channels: 550mW

Verification Environment



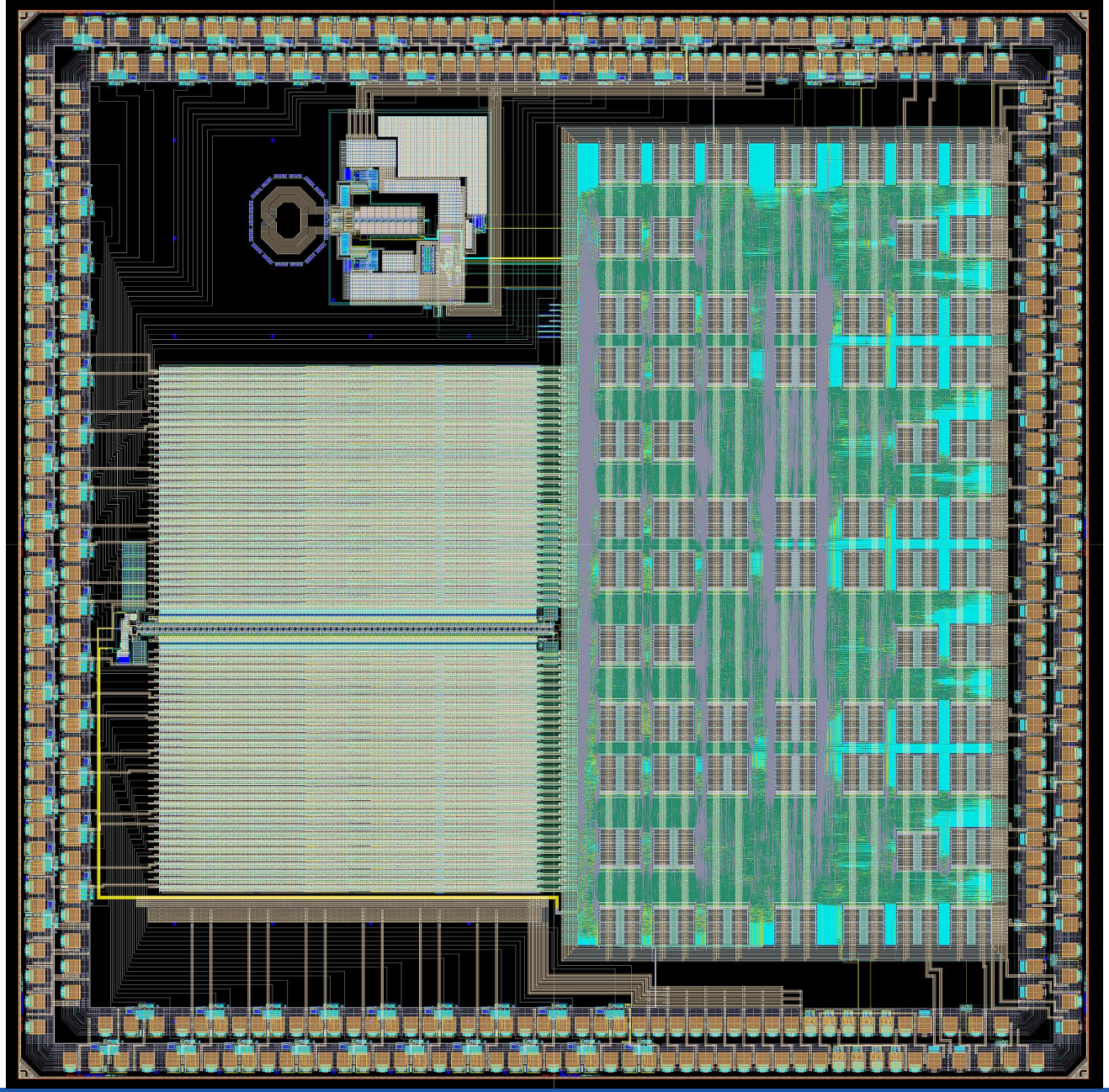



```
Matching trigger header:  911  27
Matching trailer:    27 101 hits
Matching trigger header:  925  28
Matching trailer:    28 107 hits
Matching trigger header:  942  29
!   23573019ps: Missing  Rising  hit at channel          1
!   23591087ps: Missing  Falling hit at channel          5
```

- Verification in SystemVerilog
- Use cases can be defined and automatically tested, visualization of buffer occupancy, lost hits etc.

Verification Features

- Environment supports and verifies all TDC features
  - Triggered / untriggered
  - Rising / rising&falling / TOT
  - Different counter and reset settings
- Extensive test cases
  - High / low / burst hit rate
  - High / low trigger rate, overlapping triggers
- Specific use cases can be defined, verified

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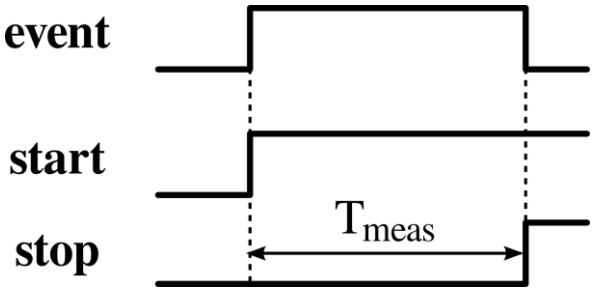
Backup Slides

Measurement Scheme

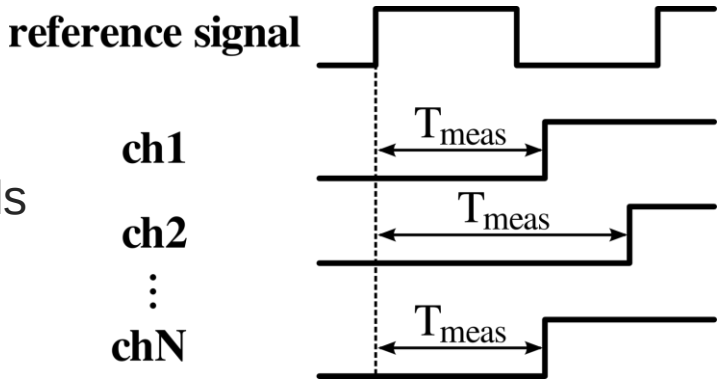
Start - Stop Measurement

- Measure relative time interval between two local events
- Small local systems and low power applications

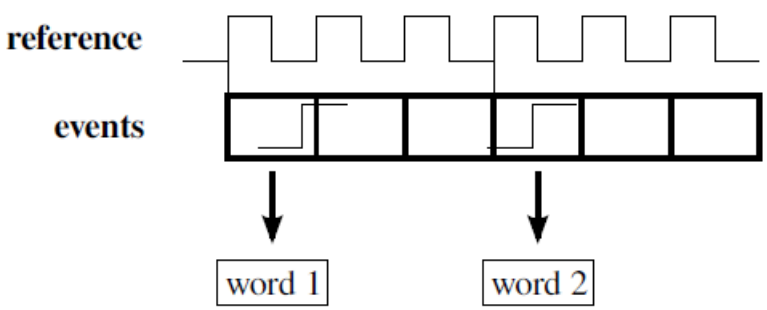


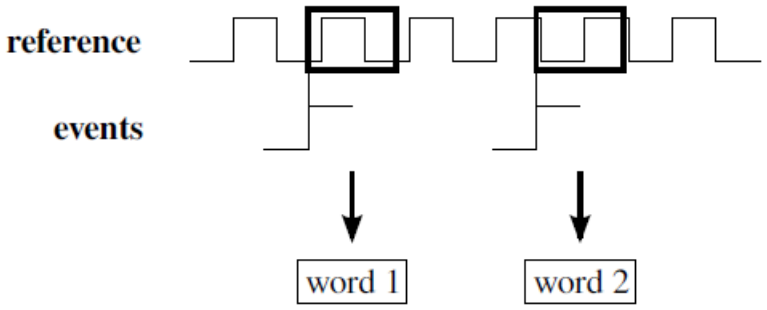
Time Tagging

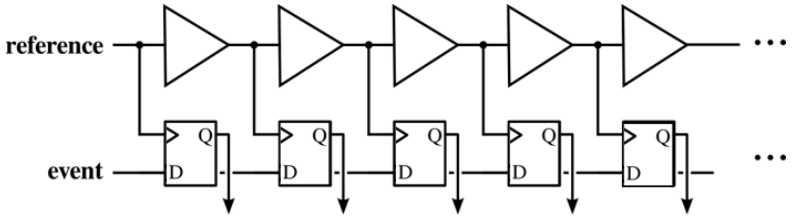
- Measure “absolute” time of an event (Relative to a time reference: clock)
- For large scale systems with many channels all synchronized to the same reference

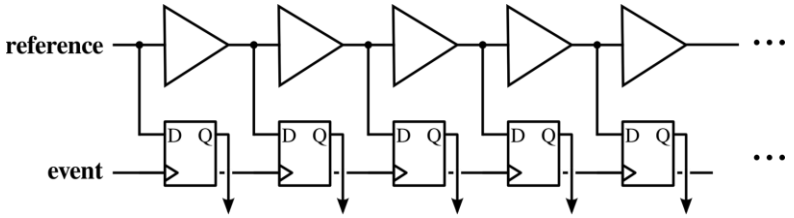


Capture Scheme





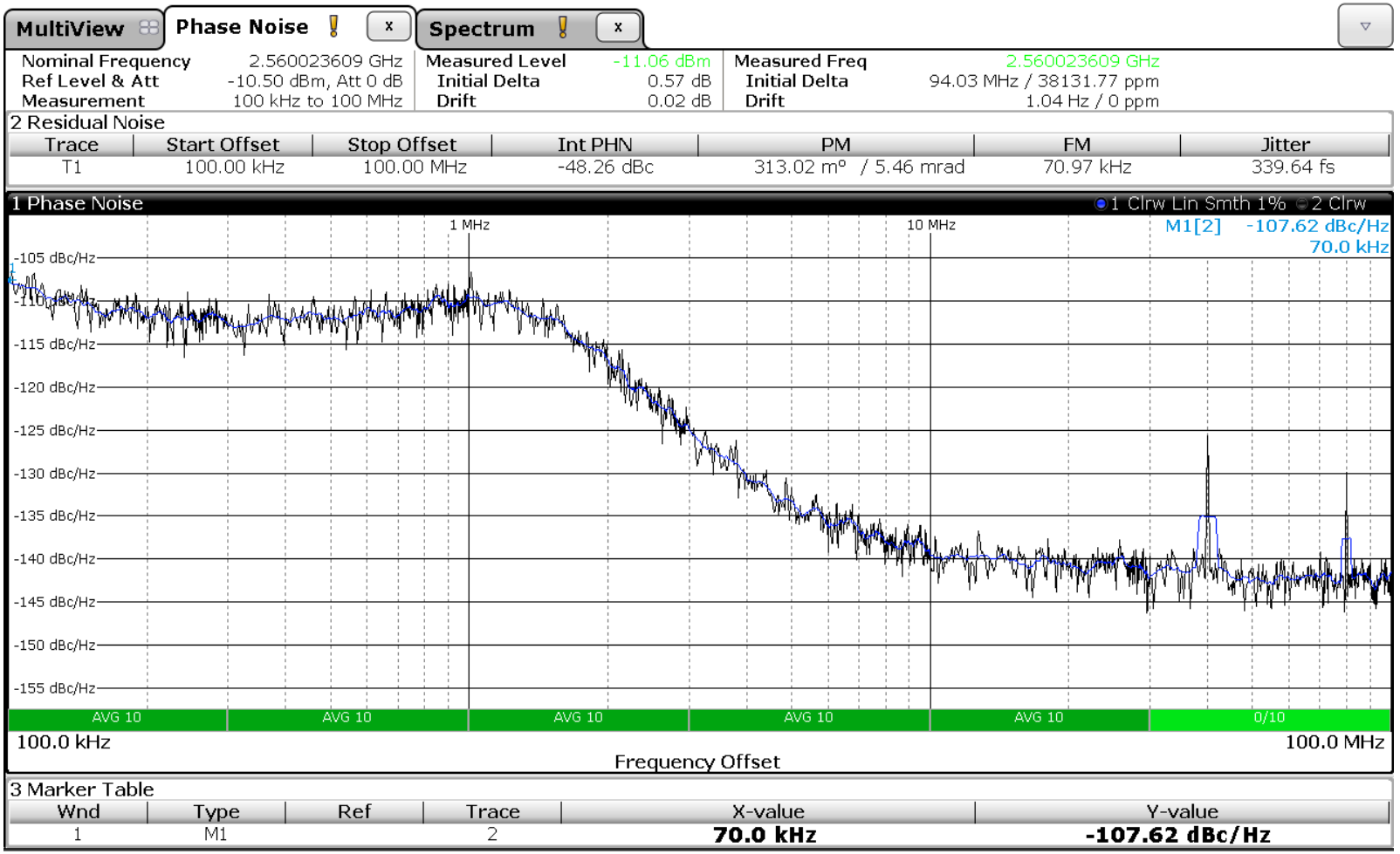




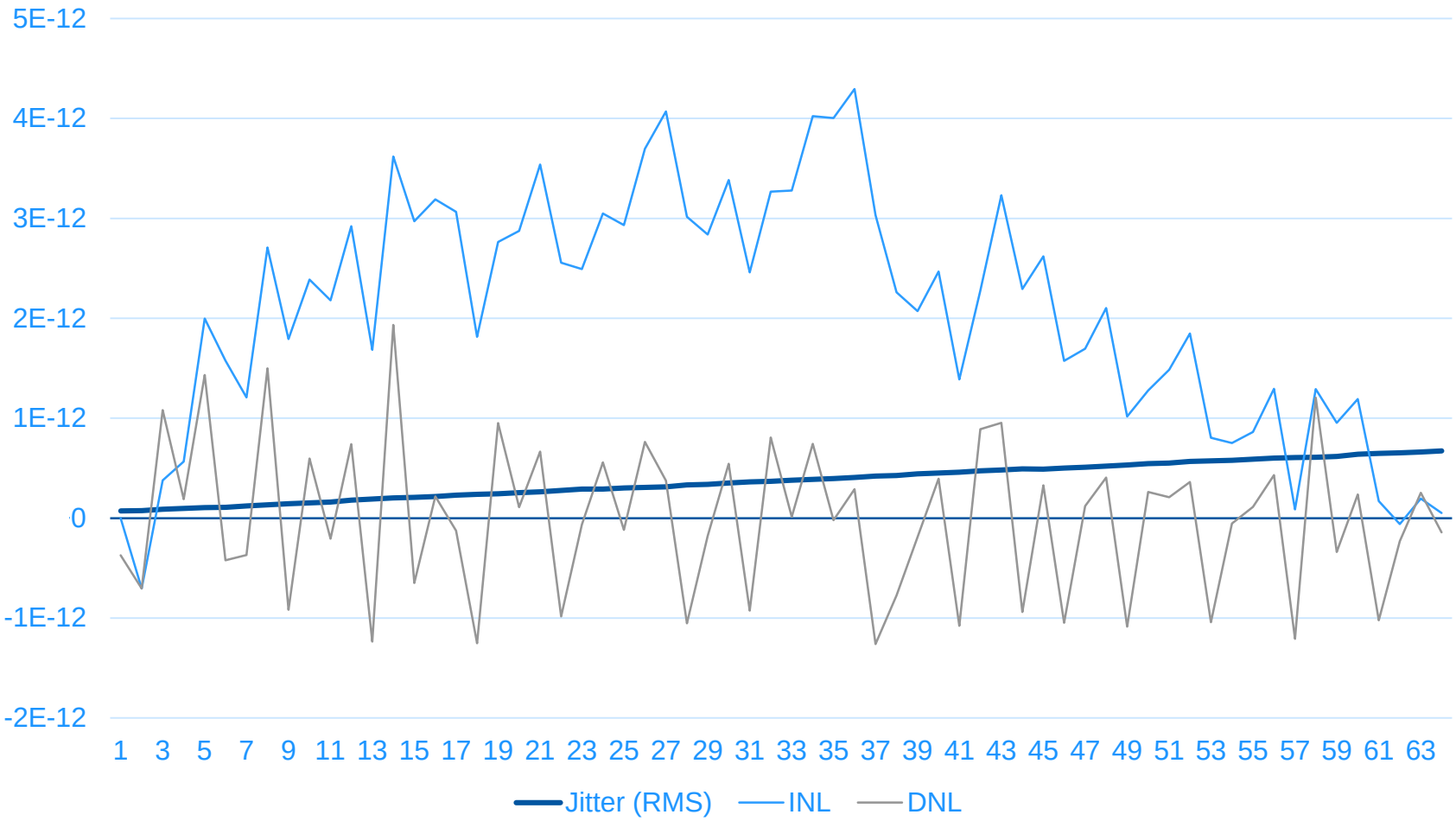
Synchronous

Asynchronous

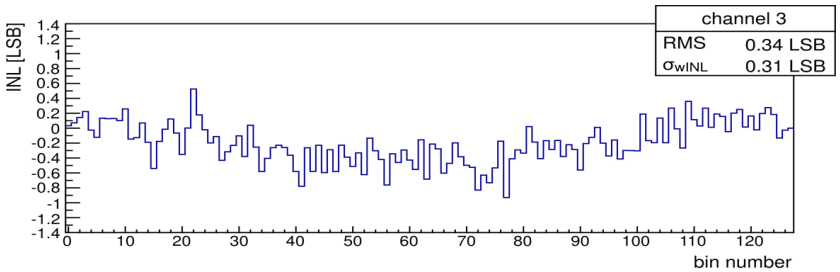
PLL Phase Noise

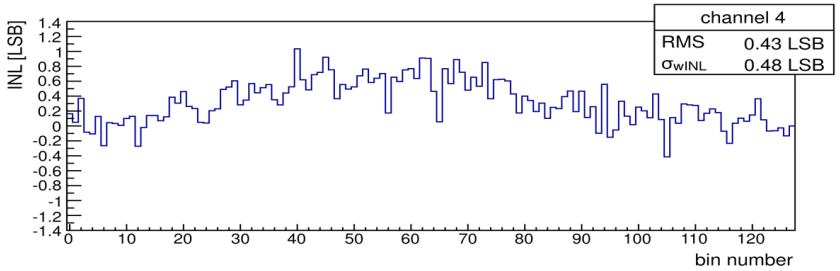


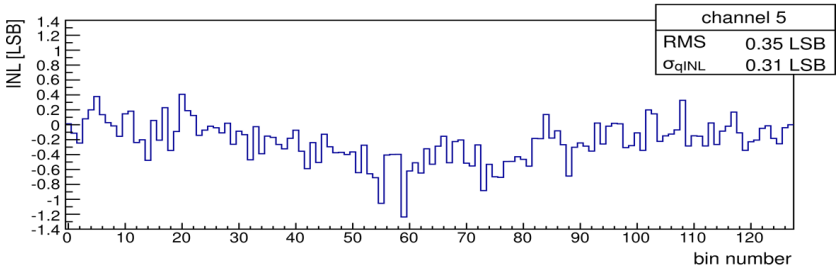
DLL Nonlinearity & Jitter

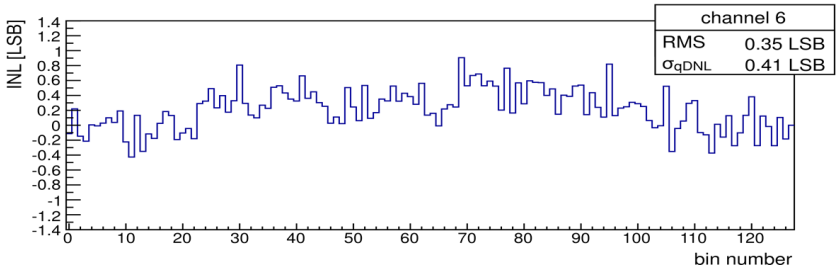


Measured Performance









Code Density Test

INL = ± 1.3 LSB

RMS = < 0.43 LSB (2.2 ps)

Expected RMS resolution from circuit simulations:
including quantization noise, INL & DNL

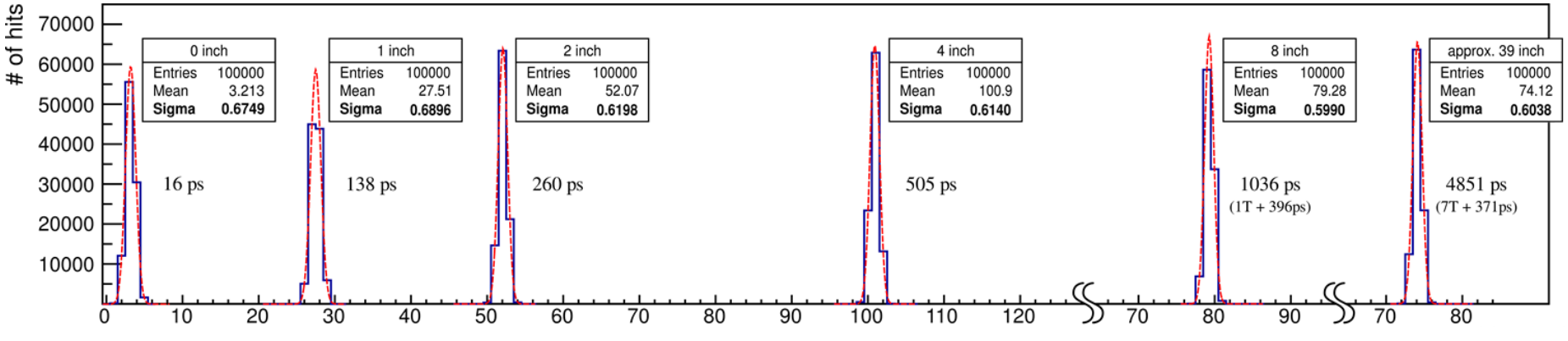
2.3 ps-RMS < $\sigma_{qDNL/wINL}$ < 2.9 ps-RMS

INL can be corrected for in software

DNL, Noise and jitter can not be corrected
(single shot measurements)

Single Shot Precision

- Three measurement series using cable delays
  - Both hits arrive within one reference clock cycle
  - Second hit arrives one clock cycle later
  - Second hit arrives multiple clock cycles later (~5ns)



σ_{TDC} < 2.44 ps-RMS

TWEPP2013 slides and paper: https://indico.cern.ch/event/228972/session/6/contribution/61
ESE seminar: https://indico.cern.ch/event/225547/material/slides/0.pdf