

Ladder assembly

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MFT Ladder Assembly – SEOUL - 2018, November 19th

12th ALICE ITS upgrade, MFT and O2 Asian Workshop



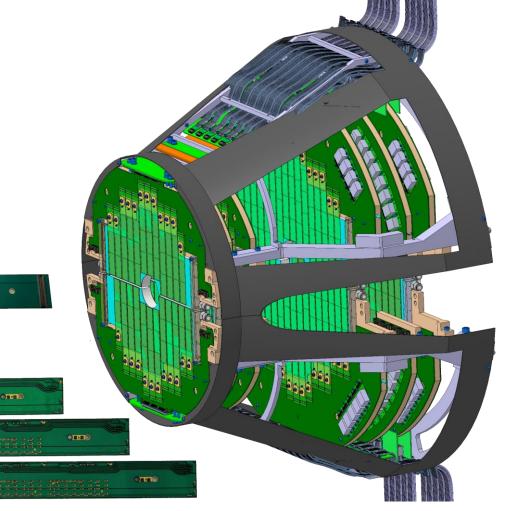
- Goal of MFT project
- Work environment and manpower
- Ladder production
 - Production overview
 - FPCs & Sensors
 - HIC assemblies
 - Bonding and conditioning
 - Ladder testing
- QA
 - Training
 - Procedures
 - Forms
 - Records in DB

Goal of MFT Project

5 disks equipped with ladders on both sides

604 ladders to do (spare included) 2 to 5 silicon pixel sensors glued on an aluminum FPC bonded





REA



MFT Ladder Production

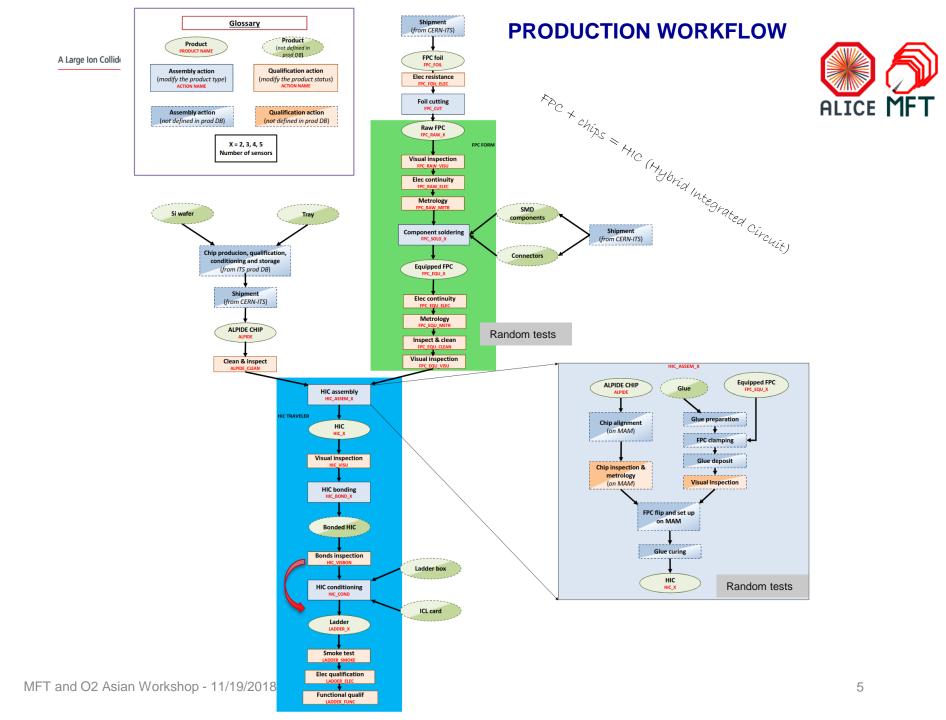
Work environment and manpower

4 teams of 2 people for assemblies @DSF

- CEA Saclay (Antenna)
- LPC Clermont
- IPNLyon
- Subatech Nantes

2 persons (IPNLyon) for FPC inspection @grey room Antenna + Kosei for qualification







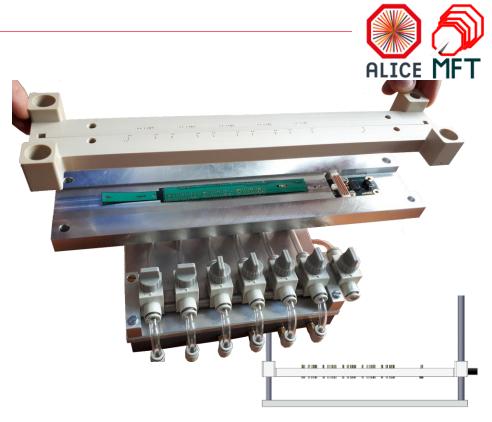
MFT Ladder Production FPCs

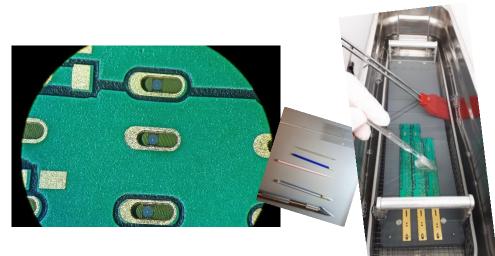




- **FPCs**
- FPCs are produced @CERN : batches of 4 foils of 26 FPCs:
- 2 x type d (5 sensors)
 9 x type c (4 sensors)
 12 x type b (3 sensors)
 3 x type a (2 sensors)
- Raw FPCs are separated by laser cutting in Italy and measured by metrology service @CERN.

- Electrical test bench made by our student Paul TETAZ, to test electrical continuity,
- SMD components soldered by Ouestronics,
- « shaving », cleaning, visual inspection, data and pictures are stored in DB.



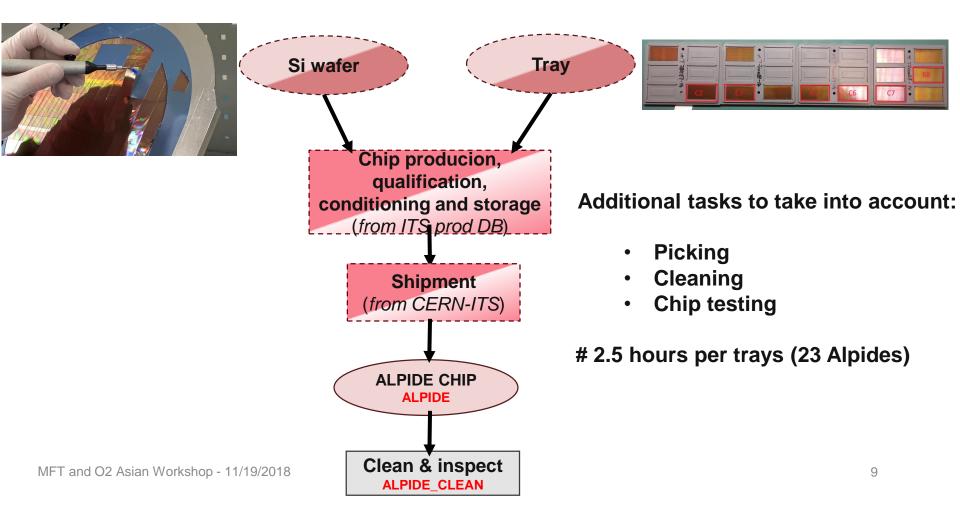


ALICE MFT

MFT Ladder Production

Sensors

Process Flow Diagram (from MFT AIT Diagram)

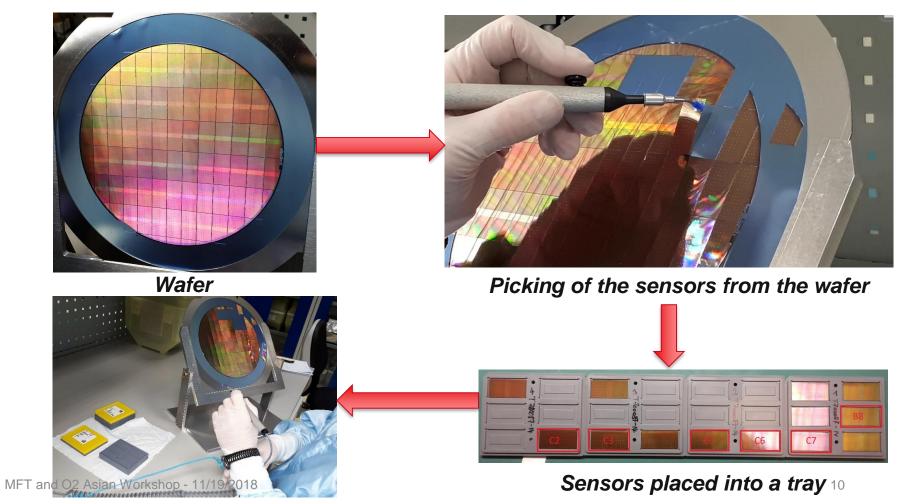


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MFT Ladder Production

Sensors

- Picking of the sensors from the wafers



Visual inspection and cleaning

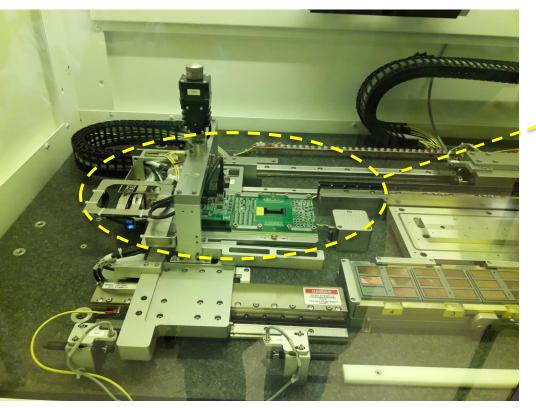
ALICE MFT

MFT Ladder Production

Sensors

- Chip testing

Probe Card Test has been set up into the ALICIA-7





Testing of the sensors:

- Digital and Analogic power
- Functional tests







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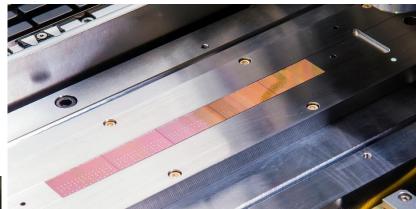
1- Tray of chips in MAM







- 1- Tray of chips in MAM
- 2- Chip positioning by MAM



MAM tests:

Dimensions inspection Edge integrity Pad Cleanliness

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- 1- Tray of chips in MAM
- 2- Chip positioning by MAM
- 3- FPC positioning on JIG



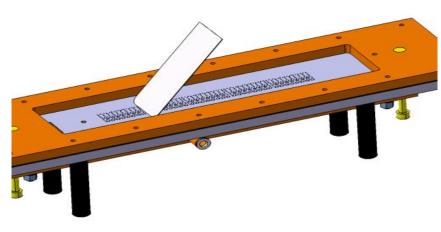




- 1- Tray of chips in MAM
- 2- Chip positioning by MAM
- 3- FPC positioning on JIG
- 4- Stencil above FPC







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- 2- Chip positioning by MAM
- 3- FPC positioning on JIG
- 4- Stencil above FPC
- 5- Glue application (Araldite 2011)
- 6- Stencil removing

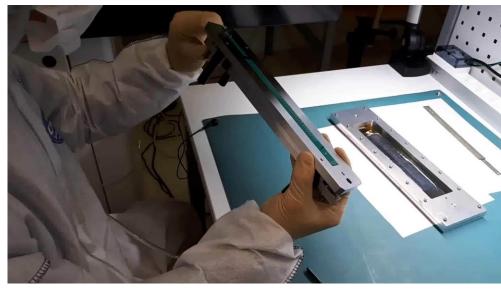






- 1- Tray of chips in MAM
- 2- Chip positioning by MAM
- 3- FPC positioning on JIG
- 4- Stencil above FPC
- 5- Glue application (Araldite 2011)
- 6- Stencil removing
- 7- FPC/Chips assembly

Presso



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Visual Inspection and conditioning

HIC becomes a ladder once bonded

- Careful visual inspection at each step
- Each ladder is stored in a metallic box and equipped with an ICL card
- Each box has 2 labels (IDs, status), QR code to dedicated Cernbox folder (pics, forms, tests)

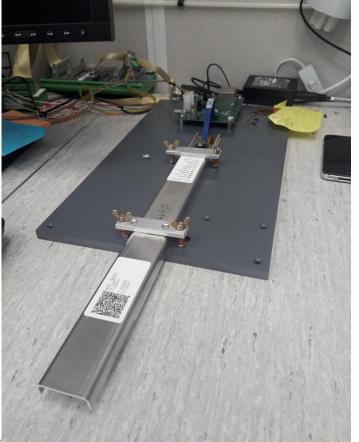






Smoke Test of the Ladder

Test of power supply: AVDD and DVDD



MFT and O2

FPC test bench: Kosei



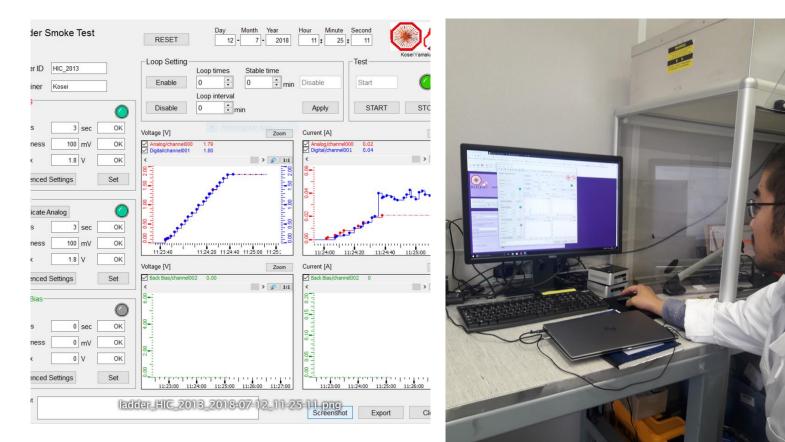
Smoke test now integrate Back Bias tests





Smoke Test of the Ladder

Test of power supply: current I AVDD and current I DVDD



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Smoke test now integrate Back Bias tests

Functional tests of the Ladder

Electrical test

Test A : power only Test B : power + clock Test C : power + clock + activity on chips (simultaneous digital scan on all working chips)

Fifo Scan

Digital Scan

Threshold scan





Storage and shipping tools: Transportation box being sent soon

- For the ladders, case Pelicase 1440 with dedicated foam .
 - 5 cases ordered and equipped @Subatech (Meriadeg) _
 - Datalogger for humidity and temperature
 - Impact indicator

Pelicase 1440







QA: training sessions for operators

- Clean room (PPT + film + practical exercises)
- FPC preparations (@grey room Antenna)
- Assemblies (@DSF)
- Visual inspections (@DSF)
- Functional tests (@grey room Antenna)





QA: procedures

- Cleaning FPC (Shaving, cleaning, visual inspections)
- Picking of the chips
- Testing of the chips
- Tooling preparation
- ALICIA starting
- Chips positioning
- Glue preparation
- FPC_Chip gluing
- HIC Removal
- Bonding Lab
- Visual inspections
- Conditioning
- Smoke test
- Functional tests (recently implemented)





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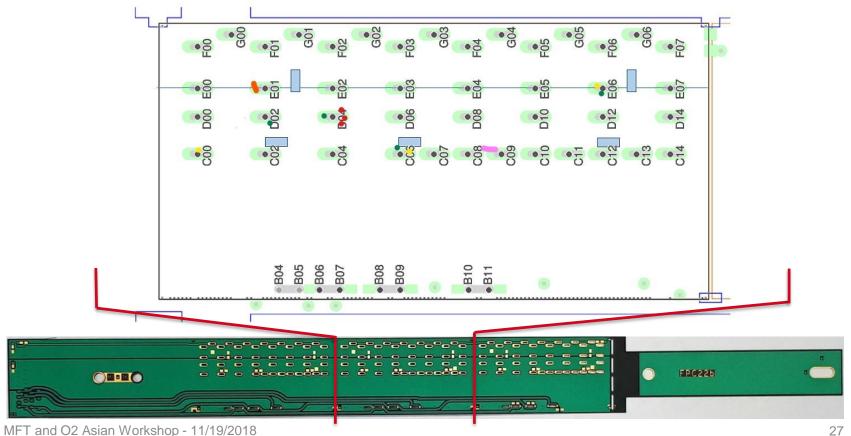
OLUMIN PERSON

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QA: Defect mapping

FPC is prepared («shaving») and cleaned (ultrasonic bath) FPC defects reporting before assembly (with binocular), RECTO and VERSO: Cracks, solder paste, bonds, varnish, foreign substance, folds, SMD, edges cut, ...



QA : forms

- XML forms, shareware librairies
- Fillable in any navigator (IE, firefox,...)
- Fills DB (id_chips, id_fpc, dates, ...)
- Stored in a workspace espace.cern.ch
- Cernbox: all pictures, files, forms, tests, ...

Also in the Cernbox: usual QA records: Equipment certificates,non conformities, revues, user manuals, procedures, ...

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Production status

Production start : 2018.04.01 First months: Training of the team

Today : 38 HICs bonded, between 5 to 8 ladders a week

Objective: production of 2 ladders a day

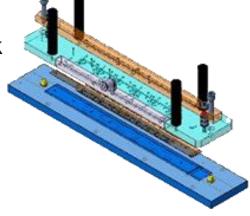
Tooling soon ready:

- electrical test bench,
- new FPC JIG,
- new bonding JIG

Last few problems to solve:

- A better FPC flatness: new FPC JIG Table, new stencil if not sufficient
- Better results for digital scan test with bigger capacitors value $(1\mu F \Rightarrow 22\mu F)$
- 6 new batchs ordered that include improvements (drilling alignement)













A Large Ion Collider Experiment

