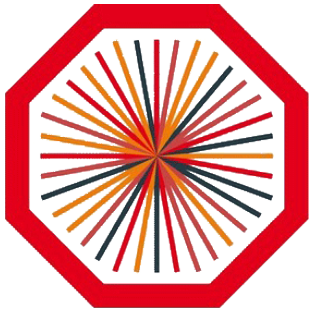
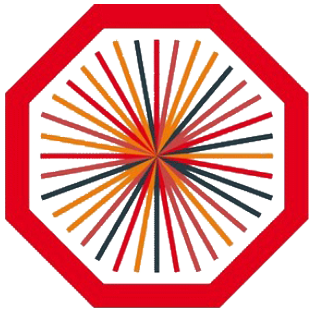
ALICE



Readout Electronics & Power Distribution

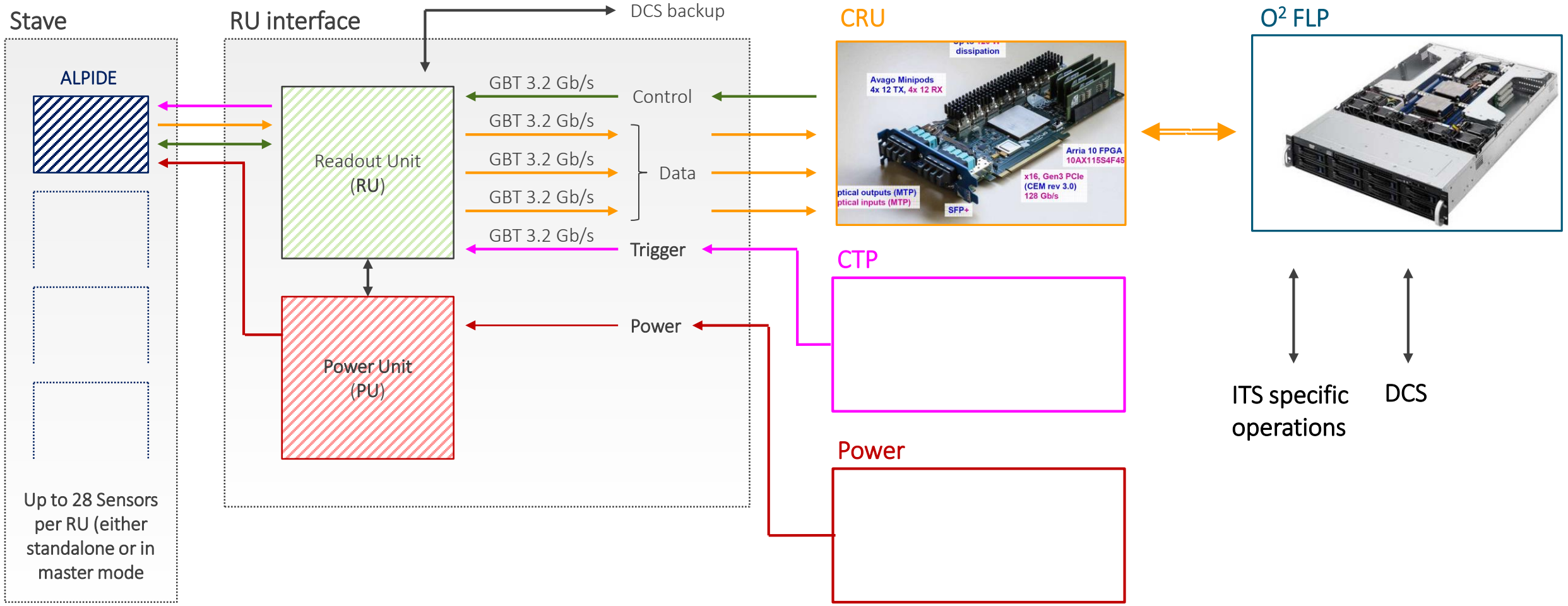
ITS Readout Electronic – **ALICE Asian Workshop** – 20 Nov 2018



Power distribution

Power – Brief recall to ITS Readout Units and Power Board system

- The ITS front-end electronic is divided into modular Readout Units (RU), identical for each layer.
- Each readout unit controls an entire stave, including power to the sensors (through custom-made powe units).
- The CRU interfaces with the Readout Unit only, which in turn manages the trigger and the power for the stave.



From LEO

Power and Bias buses

- Production appears to be proceeding according to schedule. Minor issues have been addressed.

OL-FBs and ML-FBs production status

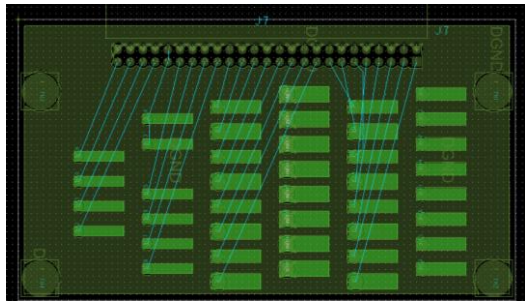
- The full production of FB is now completed and shipped to Torino.

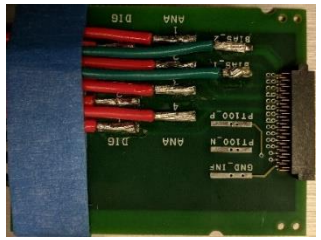
OL-FB-BOBs, ML-FB-BOBs and PB-BOBs production status

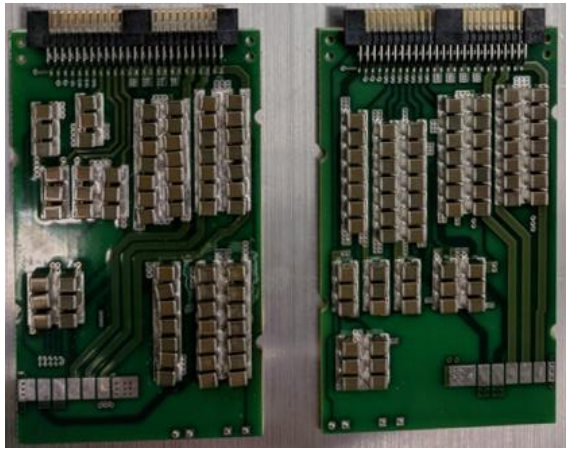
- The full production of BOBs have been delivered to LBNL and shipped to CERN for assembly into cable harnesses. The assembly is in process at Fisher.

PB-BOB brackets

- PB BOB brackets have been ordered and should arrive in the next few weeks.



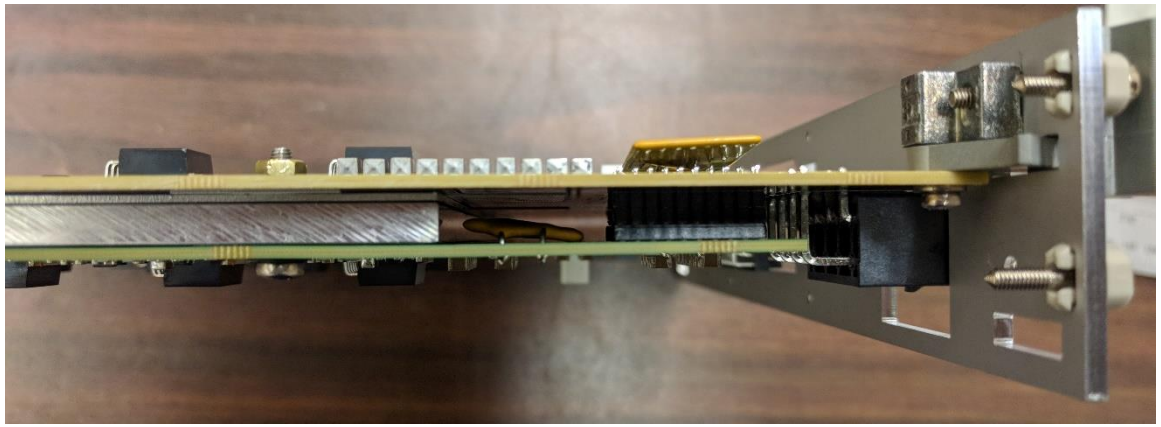


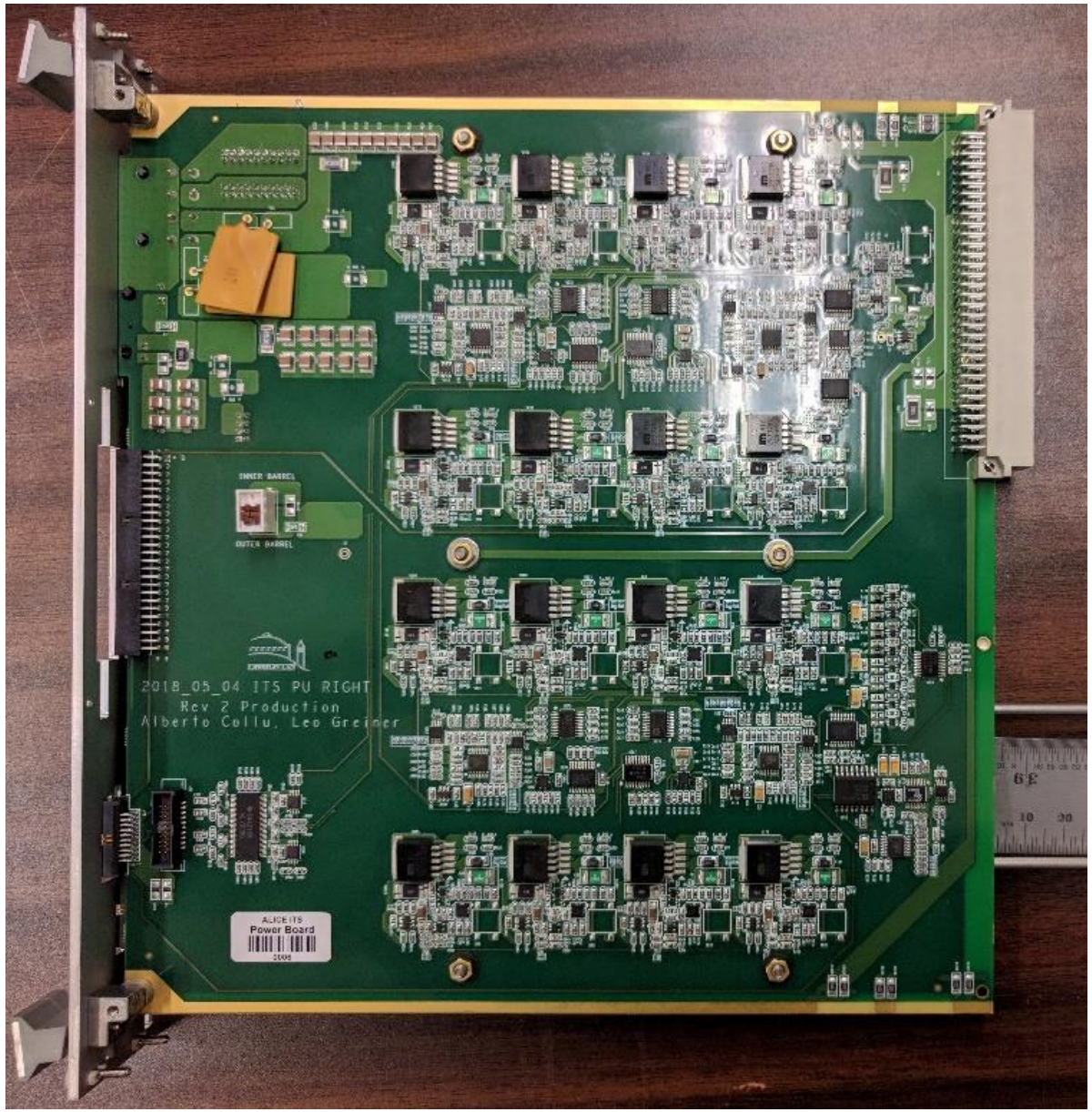


Power – LBNL power board production status

From LEO

- 24 assembled and tested power boards shipped to CERN with CERN produced heat exchangers.
- 5 assembled and tested power boards shipped CERN with heat exchangers from the vendor
- The heat exchangers from the vendor have a smaller ID tubing than was specified. Approximately 1-1.2 mm.
- We will be making tests at LBNL to see the temperature rise as a function of flow pressure (remember we have a negative pressure water system so we do not have a lot of pressure headroom).

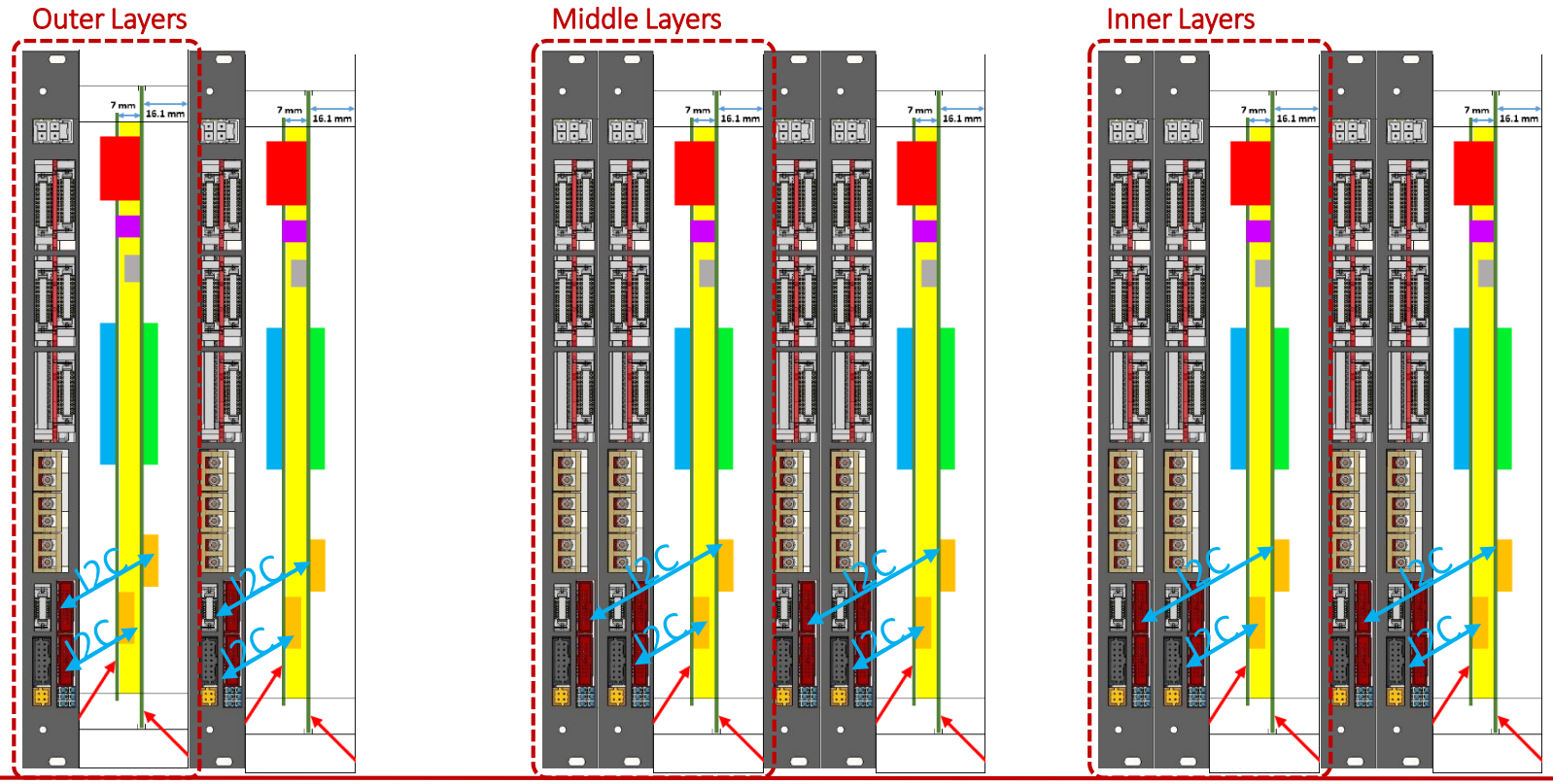




Power – 150 CERN purchased Power Boards production status

From LEO

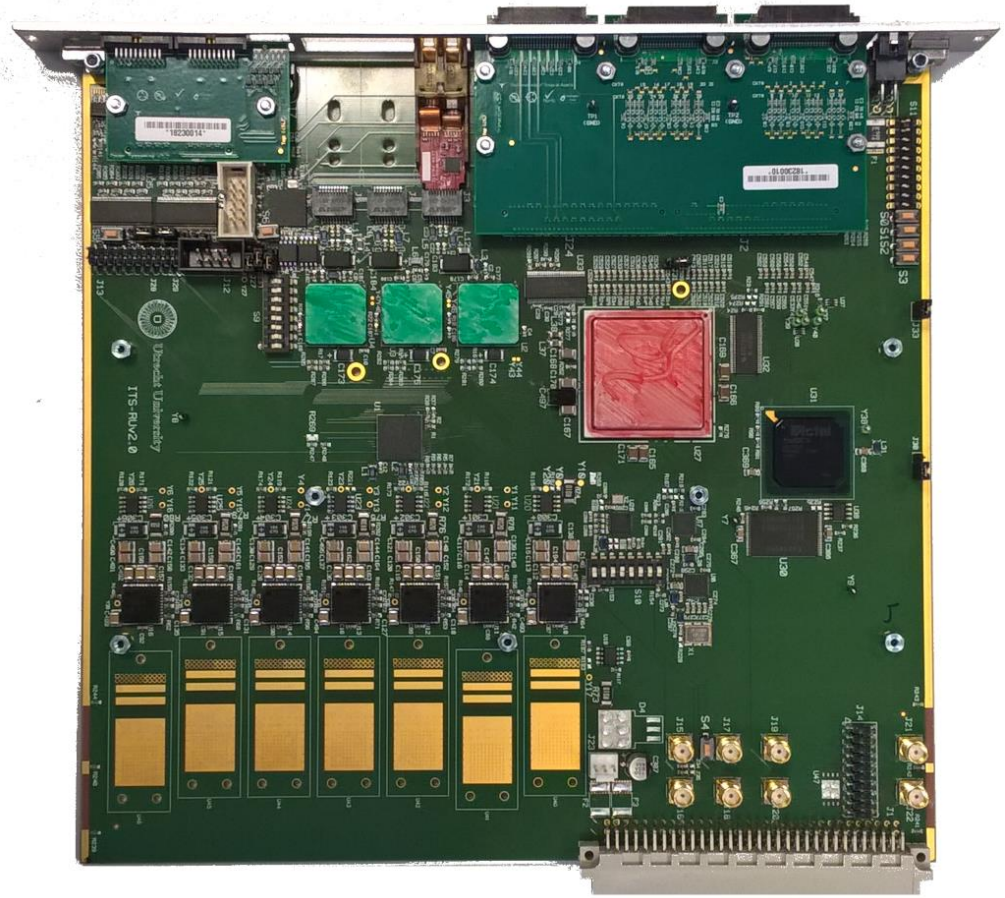
- We have been in contact with the vendor for parts substitution and PCB parameter adjustments. A supplementary cost has been established for these changes and the purchase order has been placed by CERN.
- There will be a delay associated with this set of changes and the 5 pre-series power boards should be delivered in approximately 3 weeks.
- If all goes as planned, the pre-series PBs of this batch will arrive at CERN in early November 2018, the first delivery of 73 will be at CERN in March 2019 and the balance of 72 will be at CERN by June 2019.

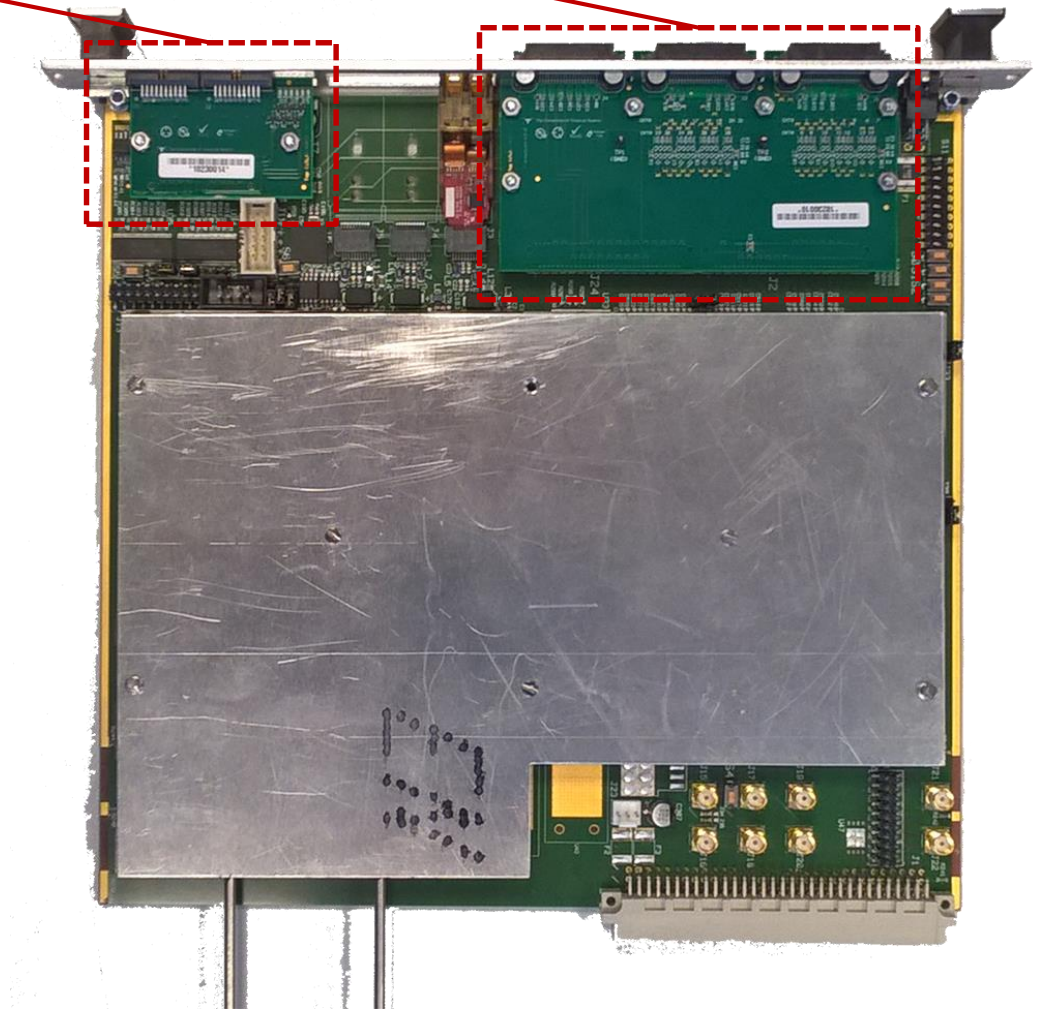


Readout Unit

Readout Unit – Design is **in production** (official version is **RU2v1**)

- RU2v1 is in production as today (could have been completed by the time of this talk).
- 1 bare PCBs arrived at CERN: visual inspection ok, now being cut for inner layers quality verification.
- All daughter boards arrived from Austin: **218 Power Mezzanines** and **218 Transition Boards**





Readout Unit – Production schedule

- First 20 board expected by November 21-24 (**this week!**).

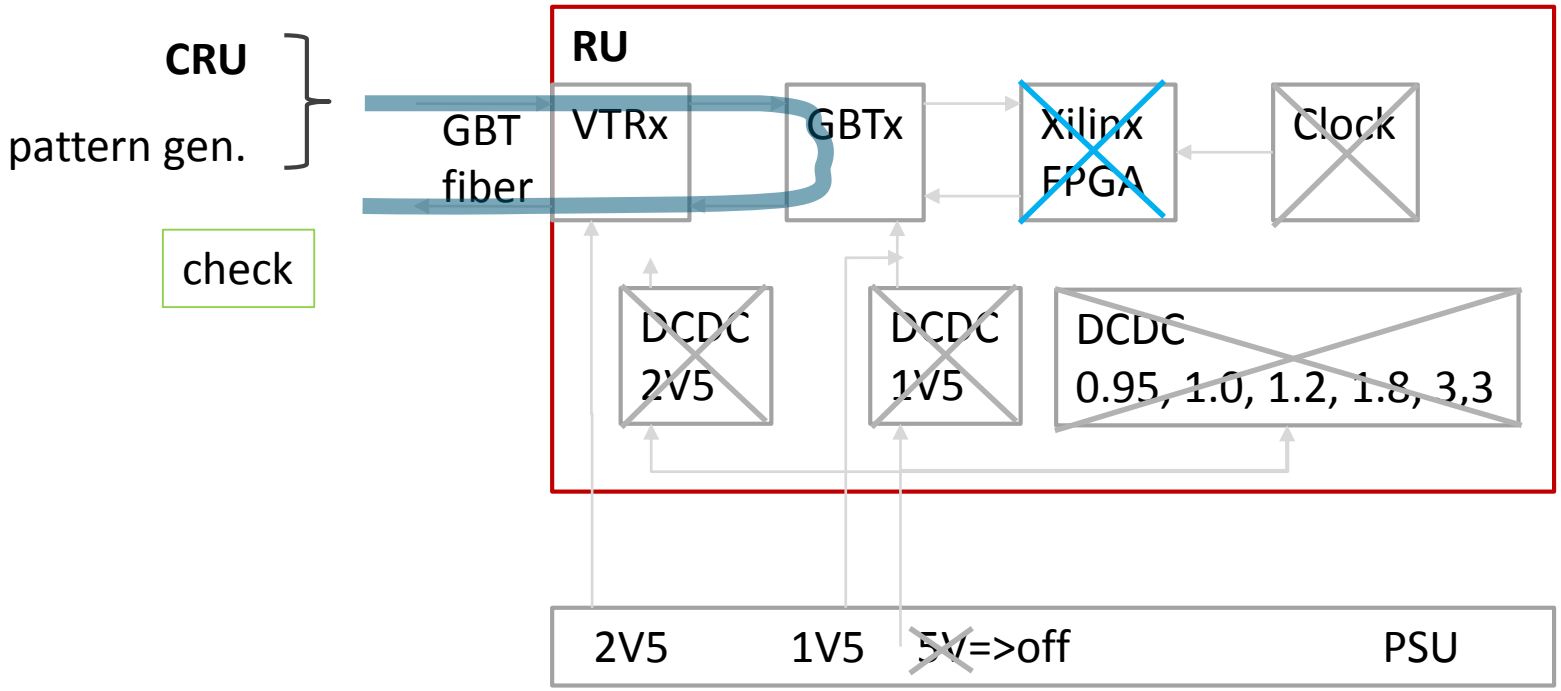
Production schedule (confirmed)

Phase		Qty	Week	Due
Purchase Order	T0			14 Sept 2018
Pre-series delivery	T0 + 10w	20 (4 MFT)	47	21 Nov 2018
Acceptance of pre-series	T0 + 13w	20 (4 MFT)	48, 49, 50	14 Dec 2018
Batch 1 delivery	T0 + 22w	140 (36 MFT)	7	15 Feb 2019
Batch 2 delivery	T0 + 29w	150 (48 MFT)	14	5 apr 2019

Readout Unit – Issue under investigation

From Marcel

- Erratic instability produces GBT link error (few per hours) on some boards, but sometimes it disappear.
- So far defeated any debugging, tests ongoing + GBT team help.

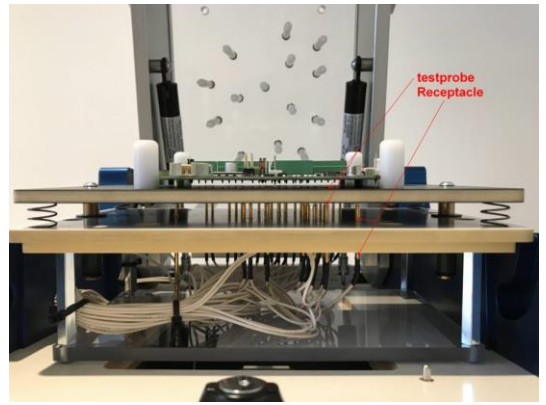


- All DCDC off, external supply on 1V5 rail & 2V5 directly to VTRx, errors remain
- Also fiber and VTRx were replaced=>
- Found using standard CRU (but could be in GBT FPGA).

Readout Unit – Testing system ready

From Marcel

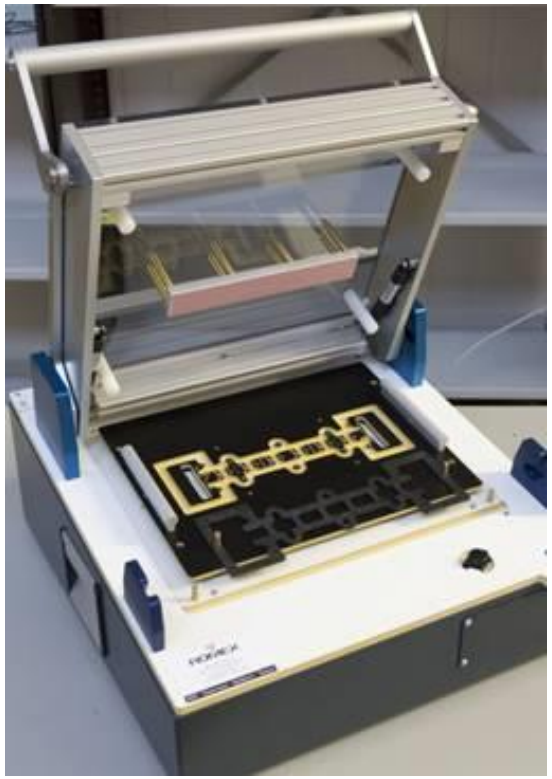
- Full test suite (hardware/firmware/software) ready in Utrecht/Nikhef



Testing / quality control:

- Producer: PCB electrical test, characteristic impedance, mechanical cross sections
- Detailed visual inspection on a sub-sample of boards (CERN)
- Boards sent to Utrecht/Nikef for acceptance.

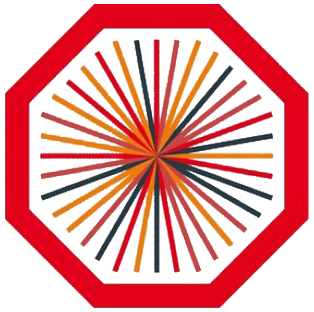
Standard acceptance testing (on all boards) – very short summary here.



- Scan barcode (bought/tested scanner)
- Power-on test (Impedance check for shorts, power rail voltages and currents).
- Program USB3 I2C PROMs, GBTx, check if all 3 GBTx are visible
- Loopback tests (Transceivers, GBT)
- All firmware(s) upload and testing (XCKU060, PA3, Xilinx DNA)
- Read and store Flash bad blocks

Extensive testing (on sub-set):

- Multiple power on power off sequences (HAMEG HMP4040 PC controlled PSU)
- Test in climate chamber NIKHEF climate chamber (reserved fOR wk48-53)
  - Passive: multiple cycles 0°C (noncondensing) to 80°C

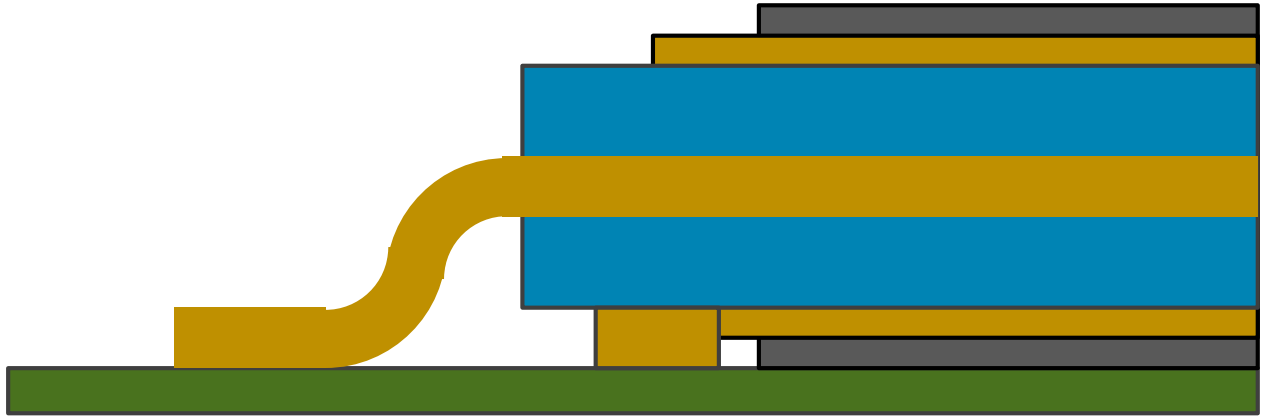


Data cables

Data cables – Issue overview

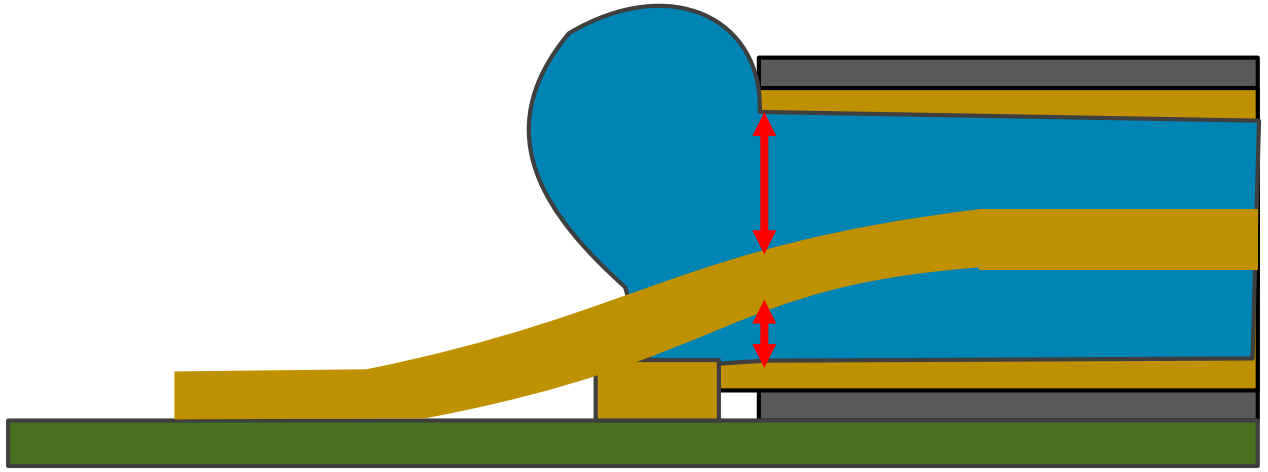
Overview

- Samtec committed 2 engineers (US based) full time on our cables, with the further support of a production expert and a project manager (Jason). Total team size is 5, with 2 full-time members.
- Material taken to the meeting was very good, clearly illustrating the status of the process development and the problems encountered so far: it seems they put resources on the task.

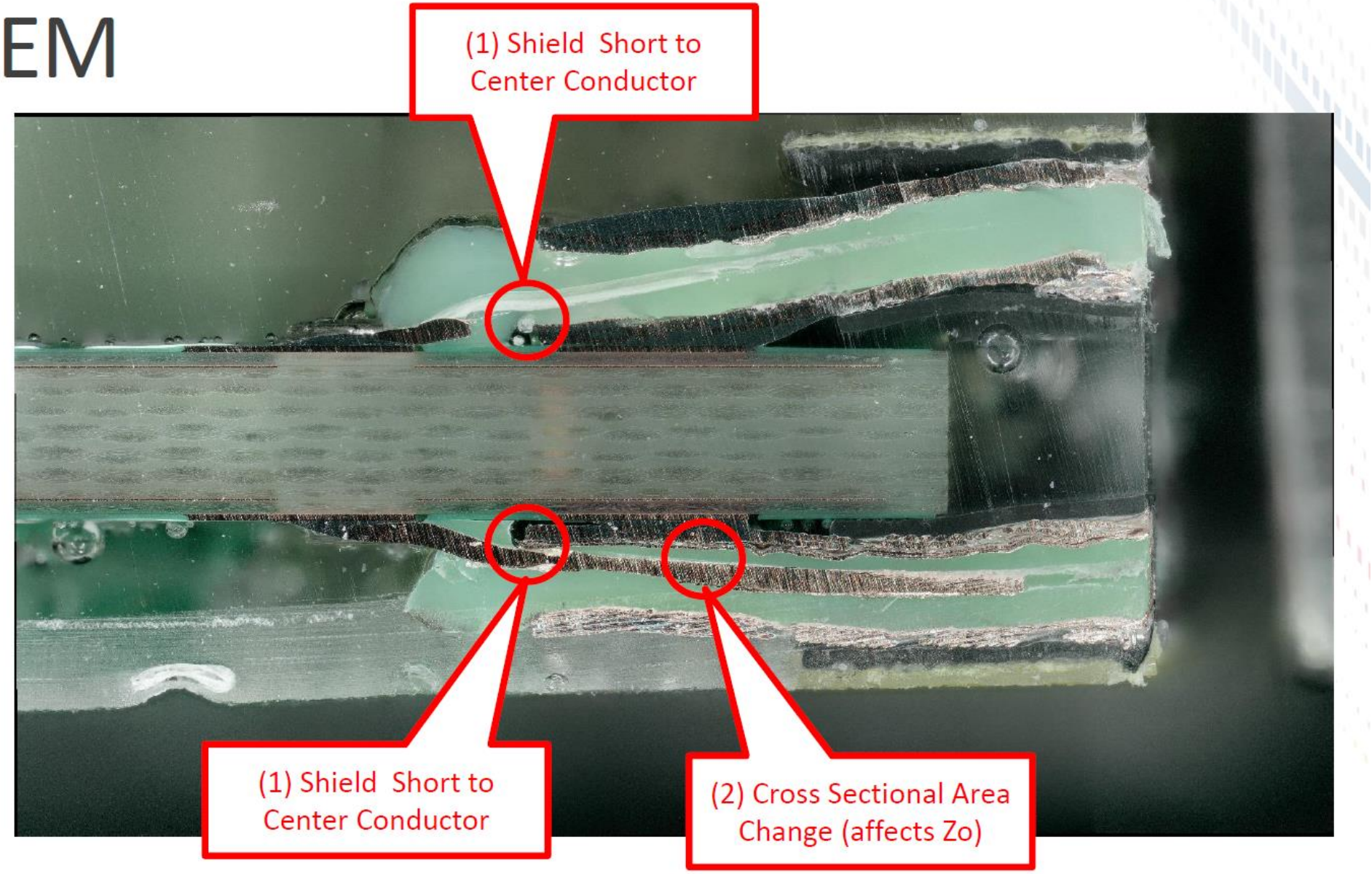


The issue in prototypes production

- Melting of the custom made dielectric while soldering the cable to the PCB, as it has lower melting point respect the standard one, which:
  1) may short the central conductor with the shielding,
  2) even if no short happens, the change in geometry (extreme in the first prototypes) affects the z0 of the cable

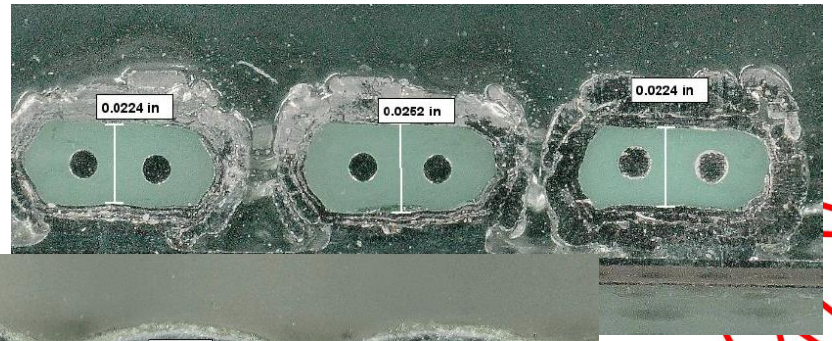


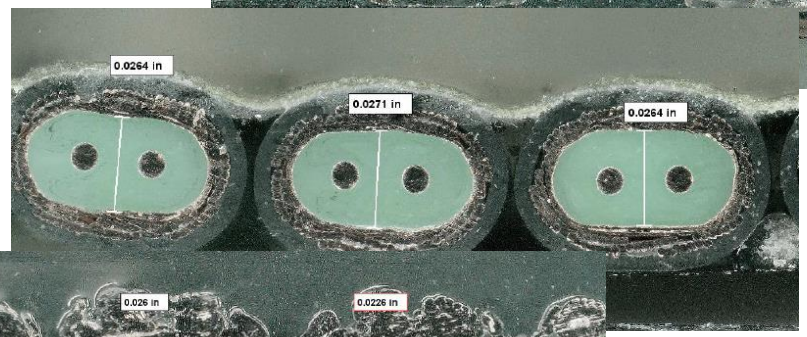
PROBLEM

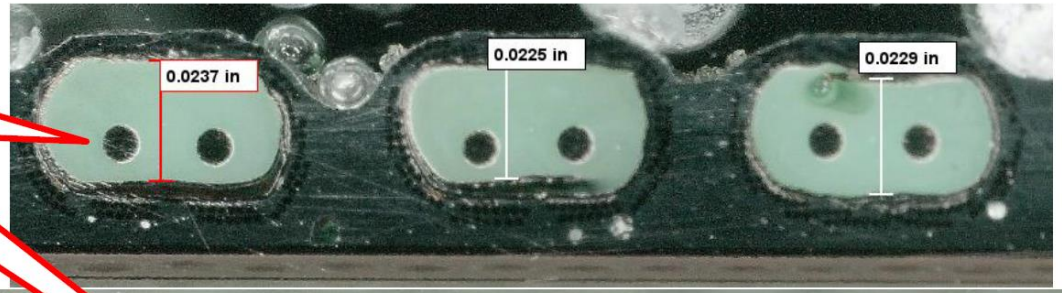

(1) Shield Short to Center Conductor
(1) Shield Short to Center Conductor
(2) Cross Sectional Area Change (affects Zo)

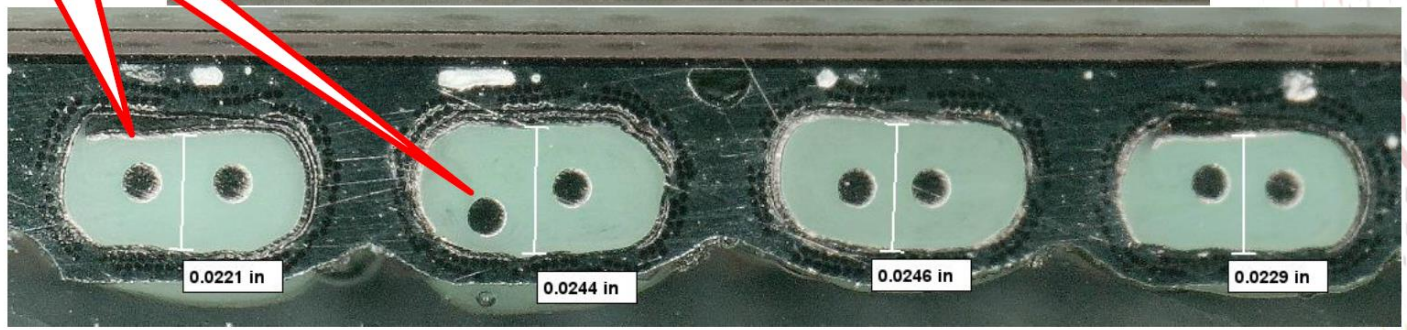
Data cables – A lot of work by the manufacturer to address the issue (courtesy by **Samtec**)

- Use of Bismuth soldering (lower temperature, and compliant with CERN safety rules).
- Pre-forming the cable end before soldering to counter-act the plastic deformation.
- Use of newly-developed low-pressure fixtures to partially relief the mechanical strain on the dielectric during the soldering process.
- **All validated for production**



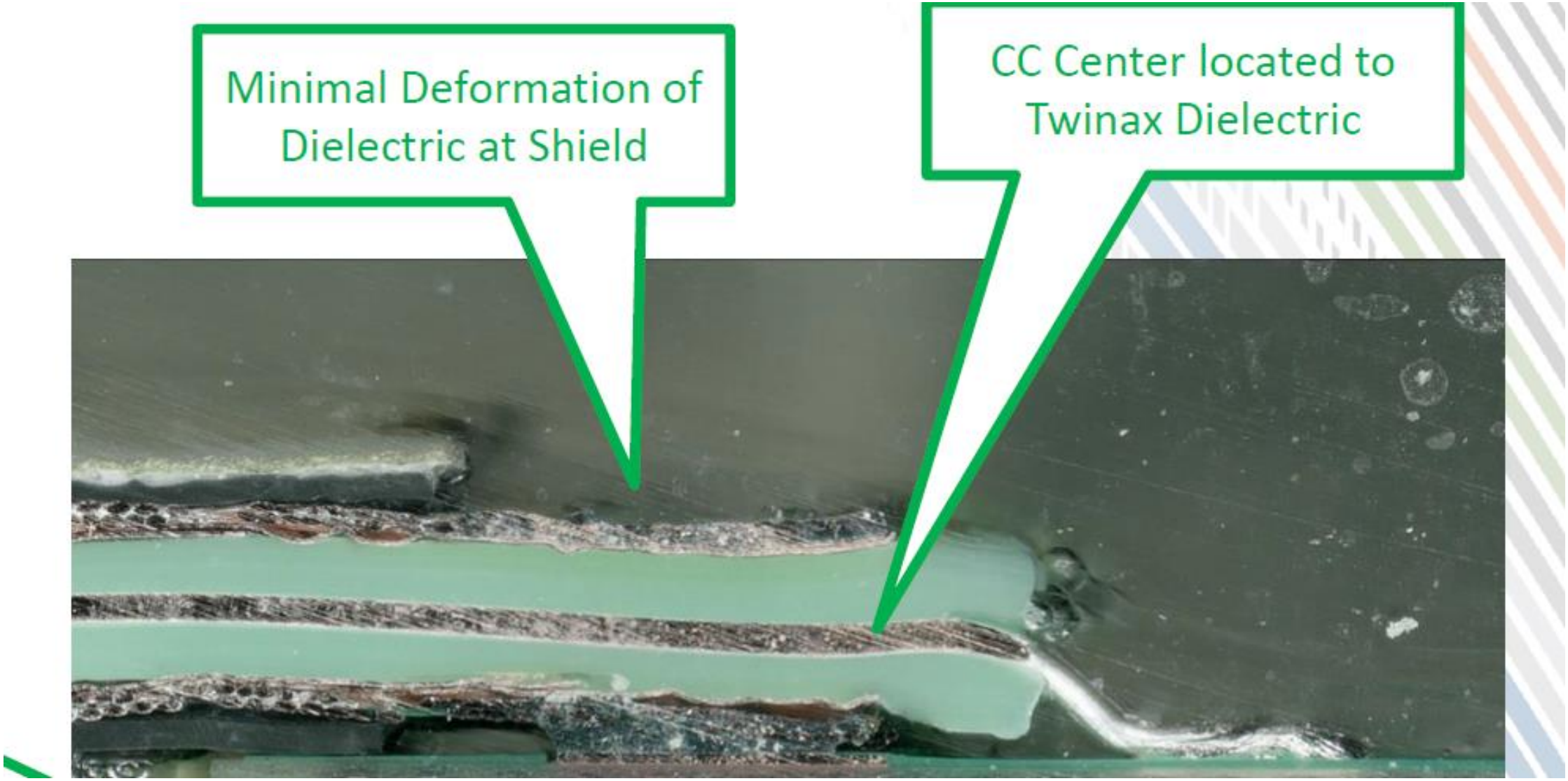






Data cables – Issue solved, ready for production (courtesy by **Samtec**)

Image here showing a pre-production cable obtained with the full production toolset (no prototype!)

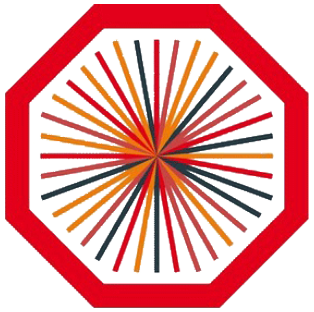


Data Cables – Production schedule

- Company confirmed production scheduled.
- Still on track to get 24 assemblies (48 cables) before Christmas break.

Production schedule (confirmed)

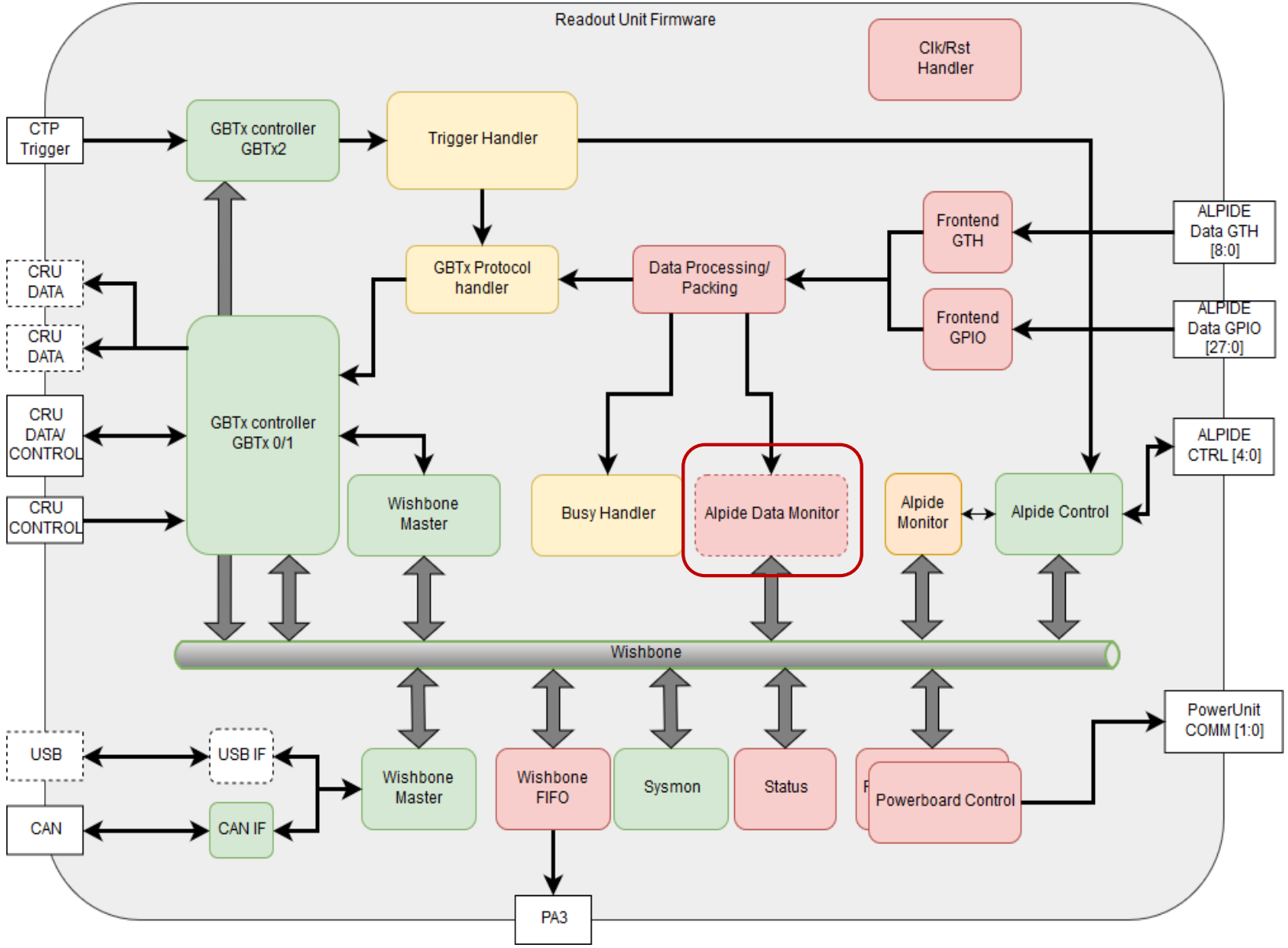
Phase		Qty	Week	Due
Purchase Order	T0		39	26 Sep 2018
Batch 1a production	T0 + 8w	24 A + B	47	15 Dec 2018
Batch 1b production	T0 + 12w	46 A + B	5	1 Feb 2019
Batch 2 production	T1 + 20w	90 A + B	10	8 Mar 2019
Batch 3 production	T1 + 26w	90 A + B	15	12 Apr 2019
Batch 1 production	T1 + 32w	90 A + B	19	08 May 2019



Firmware, software & CRU/O2 interaction

Firmware – Status overview

From Johan



- Several minor changes have been done to the firmware in the last month.
- These are mainly tweaks and adjustments and not complete redesigns
- The most significant update is the addition of an Alpide monitor module.
  - Still being specified – design expected to start by end of November
  - A similar module for monitoring of the power board is being considered
  - Not focused on push architecture (but might be considered for later).

Firmware – ALPIDE Monitor quick overview

From Johan

- Task: Read I, V, T ++ from ALPIDEs during operation
- Challenge: Using ALPIDE control bus - shared with trigger distribution
- Specs (short form):
  - Support 3 modes of operation:
    - Idle mode
    - Continous mode
    - Triggered mode (most challenging)
  - Deterministic timing for ALPIDE control bus access
  - Flexible solution with user specified ALPIDE registers to monitor
  - Monitored values available via Wishbone bus for *pulled* DCS access
    - Should also be easibly adaptable for push mechanisms
- Solution: using the abort gap to readout ALPIDE parameters
  - In the worst case 2625 ns needed, 2975 ns is the abort gap duration.
  - Flexible solution with user specified ALPIDE registers to monitor
  - CTP issues a specific flag to signal the abort gap start (or we count by ourselves)

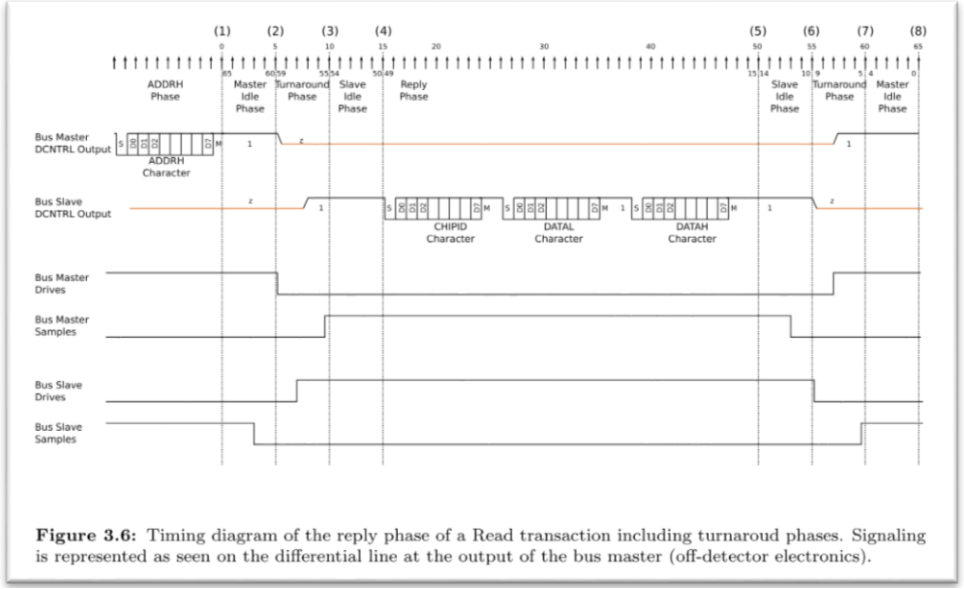


Figure 3.6: Timing diagram of the reply phase of a Read transaction including turnaroud phases. Signaling is represented as seen on the differential line at the output of the bus master (off-detector electronics).

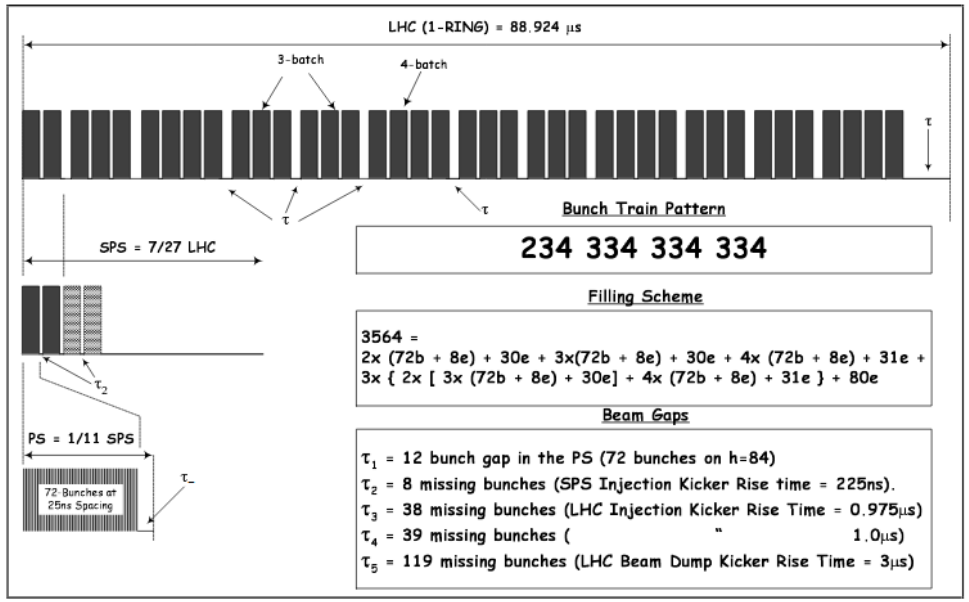


Figure 1: Schematic of the Bunch Disposition around an LHC Ring for the 25ns Filling Scheme

Firmware – Ongoing firmware/software activities

From Johan

Programming of Xilinx

- Magnus is working on software control of the fifo interface in the XCKU as well as JTAG programming of the PA3
- Updating the scripts to support the PA3 v0206 firmware is on hold for now

Documentation

- An effort to improve (actually build!) the documentation on the XCKU project has been started.

Firmware updates:

- All 28 lanes enabled in the firmware
- The lane numbering has been remapped so it would be sequential on the new transition board for the RUV2

Software:

- SWT and SCA communication works
- However, only able to talk to one RU at the time due to limitations in CRU (see next slides)
- Data taking is working using the SW readout modules from O2

CRU/O2 – Interaction

- **No major issues** so far.
- Excellent support from the CRU/O2 team.
- SWT protocol works as expected.

(Very) **minor issues**

- Python versions differ (some missed pre-agreement, little can be done now)
- …

ITS specific requests (already in discussion)

- Some extra counters to better check the data flow (mostly to monitor SEE corruptions).
- **Multiple input FIFOs** (one per RU connected) to allow RU pushing SWT to the CRU.

CRU/O2 – ITS SWT on multiple channels (in **discussion** with O2/CRU)

SWT as present

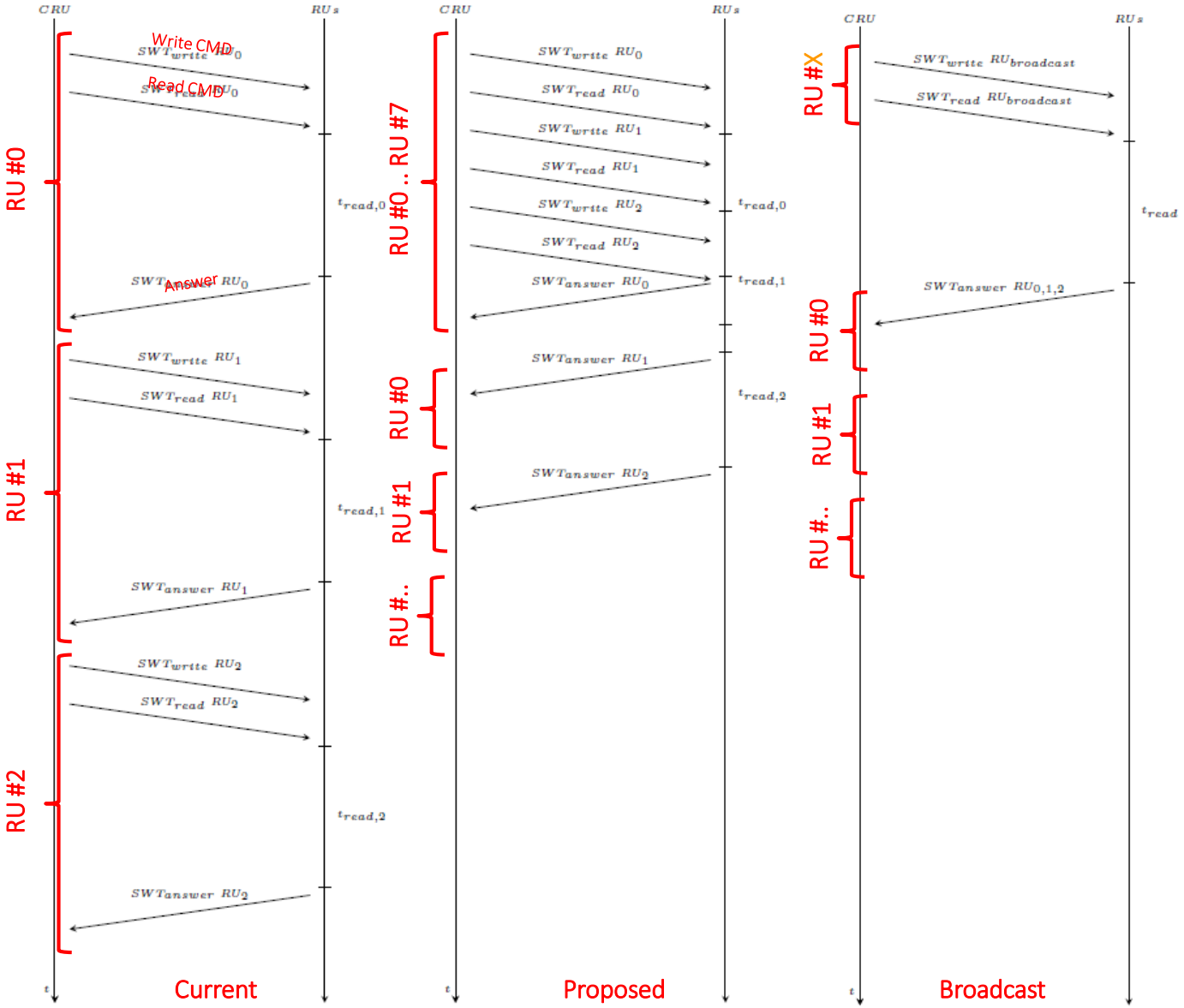
- Each Common Readout Unit (CRU) is connected to 8 Readout Units (RUs). Current CRU implementation has a multiplexer connecting to a single RU. **If a RU answers on a different channel than the one selected, the data are lost.**
- The answers for the SWT on a single RU can take "long time" for some operations, prompting for a "push" mechanism.

Uplink FIFOs on CRU

- What ITS proposes is a per-channel FIFO to store the results of the SWTs. This would greatly reduce the time to query information from multiple RUs.
- Each channel FIFO should have a depth of 1024 words.

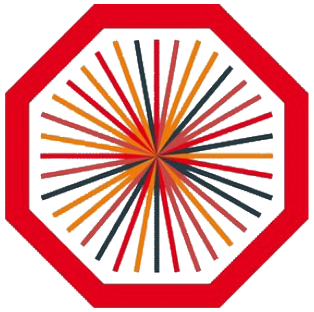
CRU SWT broadcast

- If a per-channel FIFO is possible, it might be beneficial to broadcast the SWTs to different RUs.
- This would also greatly reduce the time required to execute periodic reads of the same values in different boards.
- This might also be done with a mask: instead of broadcasting to all the boards only a subset could be set with a 1-hot encoding.



(a) Current implementation.

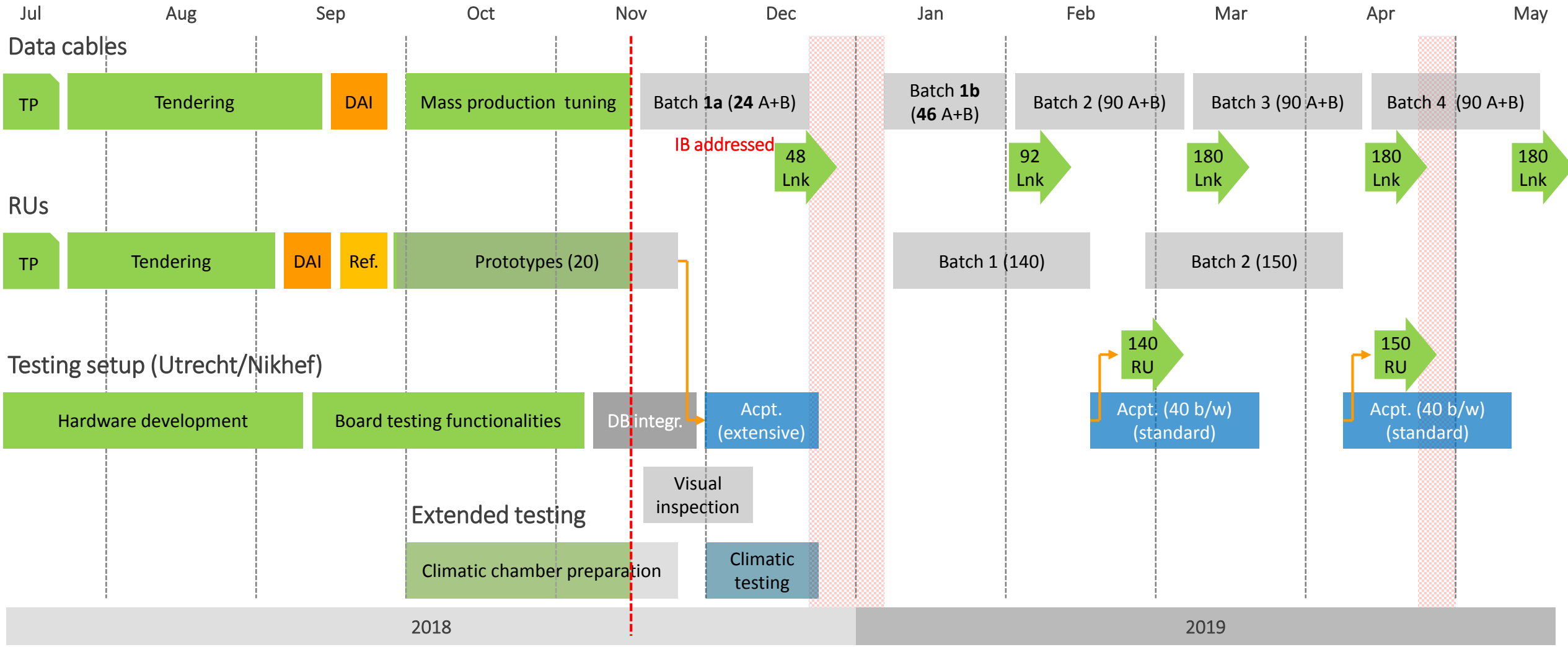
(b) 1 FIFO per channel.



Timeline

Production – Overall timeline

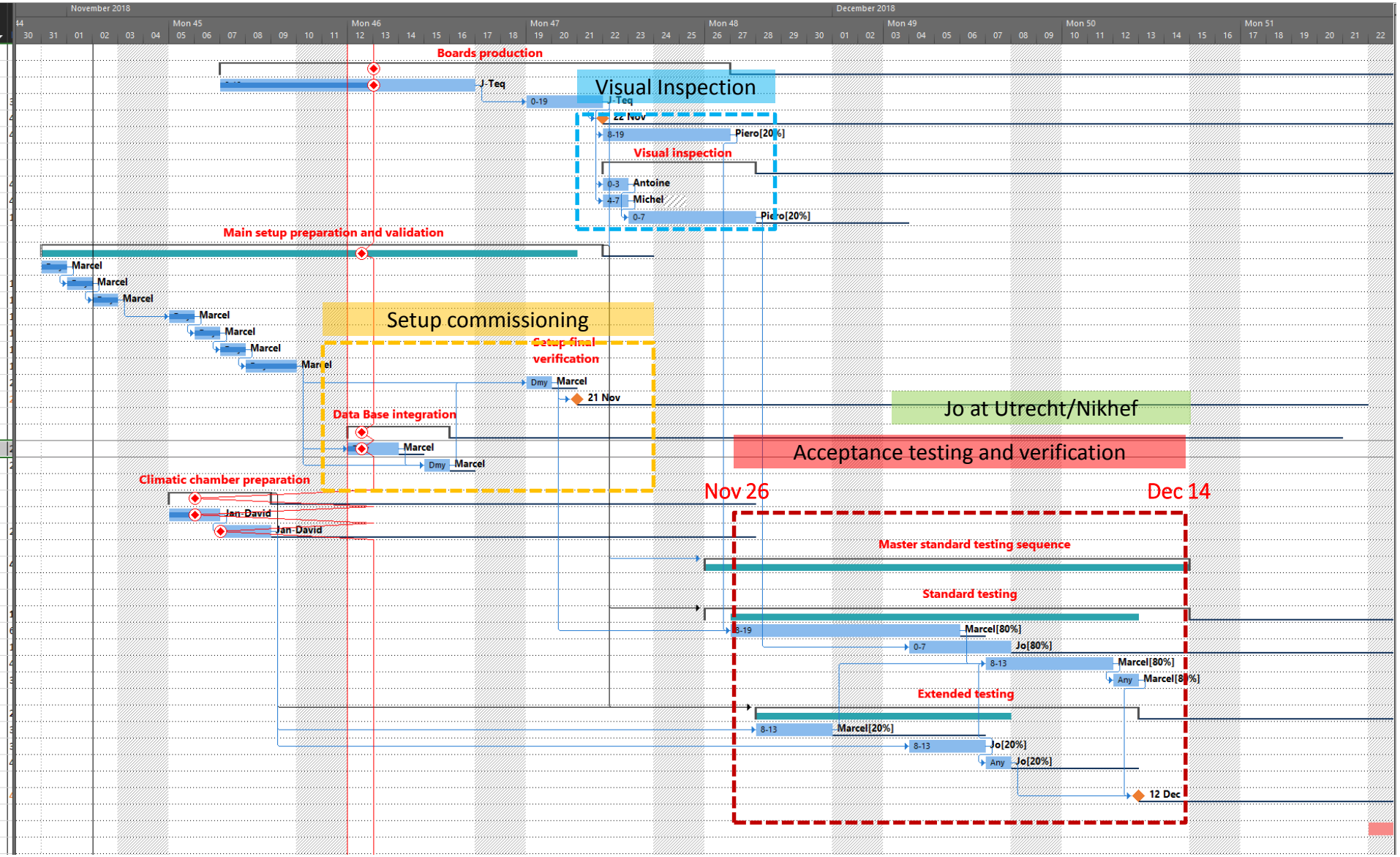
Both RUs and Data Cables are at the DAI. Goal is having 20 RUs before Christmas Break, as well as enough data cables to connect the whole IB (24 assemblies, equal to 40 data cables).

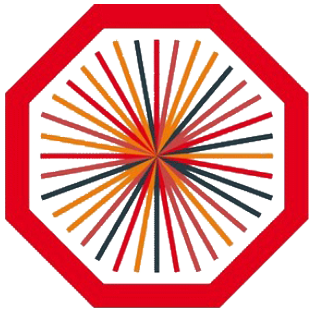


Production – RU2v1 pre-production testing detailed timeline

Setup and peole almost ready in Utrecht/Nikhef to receive the 20 RU2v1 pre-production boards

Task Mode	Task Name	Duration	Start	Finish
	Pre-series Production [0 - 19]	**14 days**	**Wed 07/11/18**	**Mon 26/11/18**
	Boards production	8 days	Wed 07/11/18	Fri 16/11/18
	Shipment to CERN	3 days	Mon 19/11/18	Wed 21/11/18
	Boards @ CERN	0 days	Thu 22/11/18	Thu 22/11/18
	Shipment to Nikhef [8 - 19]	3 days	Thu 22/11/18	Mon 26/11/18
	Acceptance at CERN	**4 days**	**Thu 22/11/18**	**Tue 27/11/18**
	Visual Inspection [0 - 3]	1 day	Thu 22/11/18	Thu 22/11/18
	Visual Inspection [4 -7]	1 day	Thu 22/11/18	Thu 22/11/18
	Shipment to Nikhef [0 - 7]	3 days	Fri 23/11/18	Tue 27/11/18
	Testing setup preparation	**16 days**	**Wed 31/10/18**	**Wed 21/11/18**
	Current/Voltage measurement	1 day	Wed 31/10/18	Wed 31/10/18
	FLASH & XCKU data extraction	1 day	Thu 01/11/18	Thu 01/11/18
	Loopback test	1 day	Fri 02/11/18	Fri 02/11/18
	GPIO test	1 day	Mon 05/11/18	Mon 05/11/18
	GBTx fusing	1 day	Tue 06/11/18	Tue 06/11/18
	Other testing	1 day	Wed 07/11/18	Wed 07/11/18
	Setup verification	2 days	Thu 08/11/18	Fri 09/11/18
	Verification with RU2v0	1 day	Mon 19/11/18	Mon 19/11/18
	Setup validated	0 days	Wed 21/11/18	Wed 21/11/18
	Data Base synchronization	**4 days**	**Mon 12/11/18**	**Thu 15/11/18**
	Prepare DB connection	2 days	Mon 12/11/18	Tue 13/11/18
	Test writing test result to DB	1 day	Thu 15/11/18	Thu 15/11/18
	Extended testing setup	**4 days**	**Mon 05/11/18**	**Thu 08/11/18**
	Verify climatic chamber	2 days	Mon 05/11/18	Tue 06/11/18
	Connections and control test	2 days	Wed 07/11/18	Thu 08/11/18
	Testing [0 - 19]	**15 days**	**Mon 26/11/18**	**Fri 14/12/18**
	Standard testing	**15 days**	**Mon 26/11/18**	**Fri 14/12/18**
	Testing boards [8 - 19]	7 days	Tue 27/11/18	Wed 05/12/18
	Testing boards [0 - 7]	4 days	Tue 04/12/18	Fri 07/12/18
	Re-Testing boards [8 - 13]	3 days	Fri 07/12/18	Tue 11/12/18
	Backup Testing	1 day	Wed 12/12/18	Wed 12/12/18
	Extended tetsing	**11 days**	**Wed 28/11/18**	**Wed 12/12/18**
	Extended testing [8 - 13]	3 days	Wed 28/11/18	Fri 30/11/18
	Extended testing [8 - 13]	3 days	Tue 04/12/18	Thu 06/12/18
	Backup testing	1 day	Fri 07/12/18	Fri 07/12/18
	Testing Completed	0 days	Wed 12/12/18	Wed 12/12/18
	Christmas Break	12 days	Sat 22/12/18	Mon 07/01/19



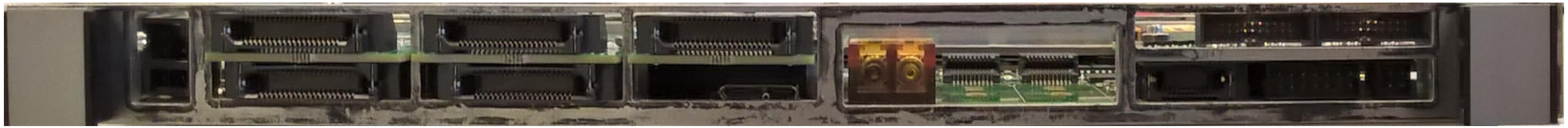


Backup

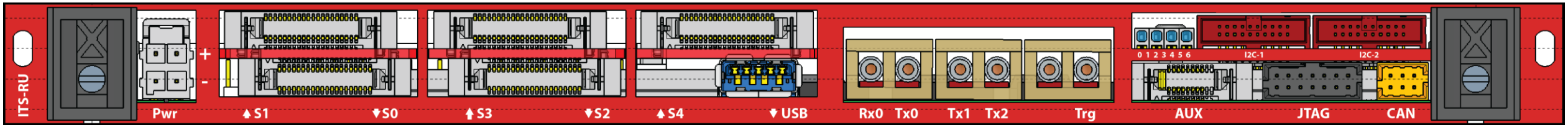
Readout Unit – Final front panel will be supplied together with the RUs

- Ancillary components and mounting hardware defined, ready to be ordered.

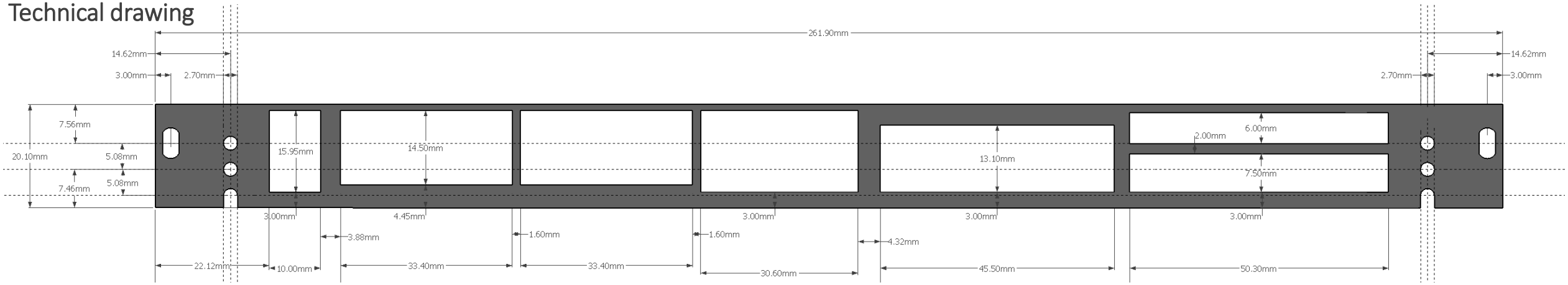
Prototype front panel



Serigraphy



Technical drawing



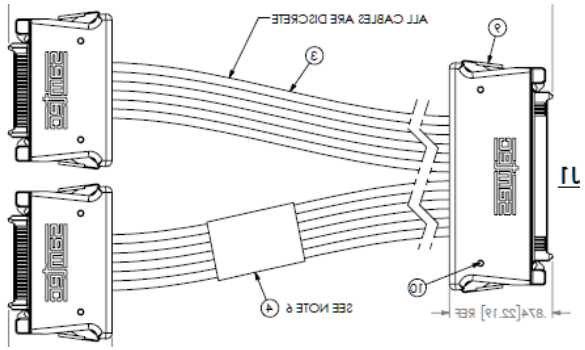
Data Cables – Production summary

PP1

PP2

PP3

HDR-203194 (Type B)

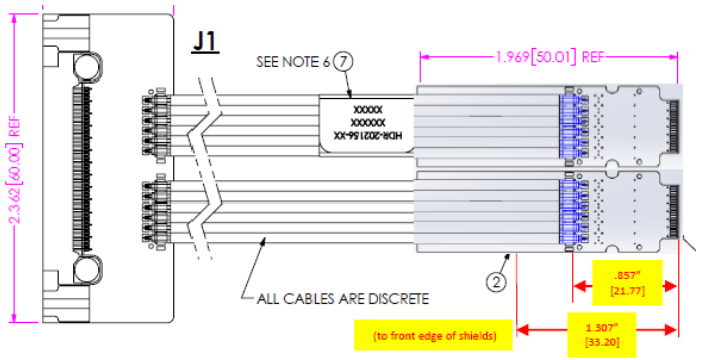


Production quantities

Layer	Qty	Length
3,4,5	60 + 8	4300 mm
0,1,2,3,4,5,6	156 + 8	4800 mm
0,1,2,6	72 + 8	5300 mm
	312 + 28	

340 Type B

HDR-206142 (Type A)



Production quantities

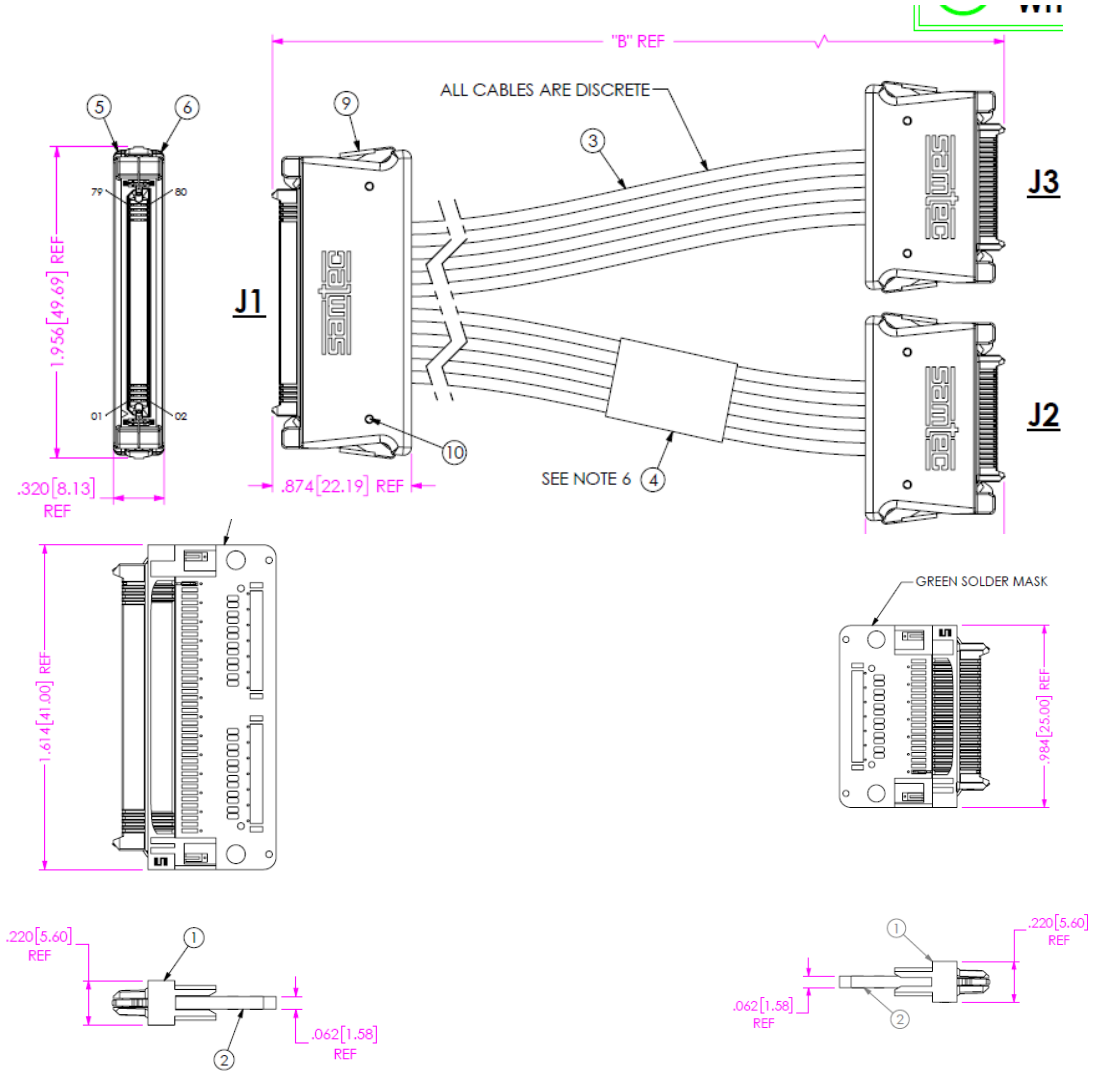
Layer	Qty	Length
5,6	180 + 8	2150 mm
3,4	108 + 8	2450 mm
0,1,2	24 + 8	2650 mm
	312 + 28	

340 Type A

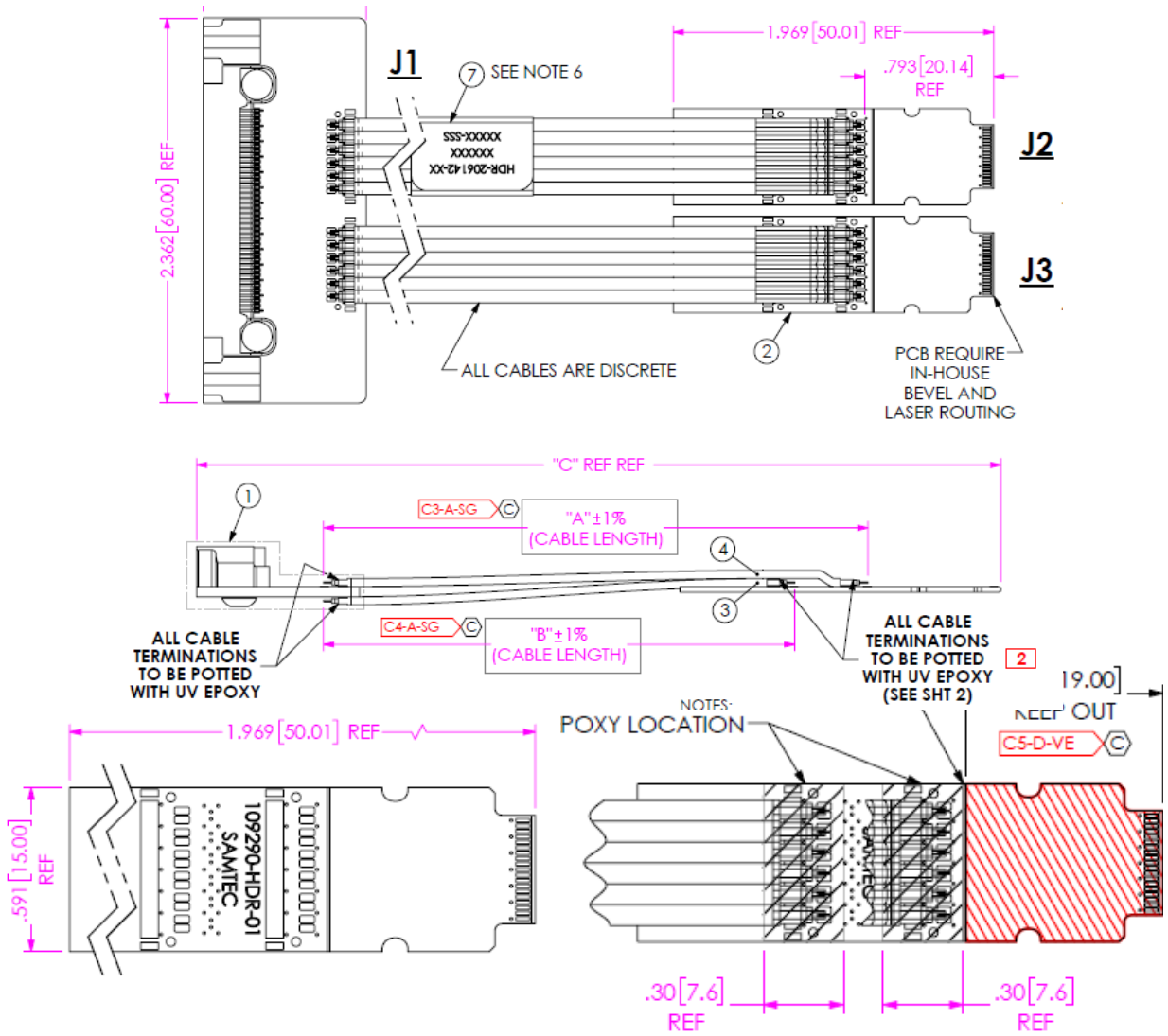
Data Cables – Design considered production ready

Considered the extensive testing so far, we will go for pre-production with latest version of drawings (**12 Sep 2018**)

HDR-203194 (Type B)



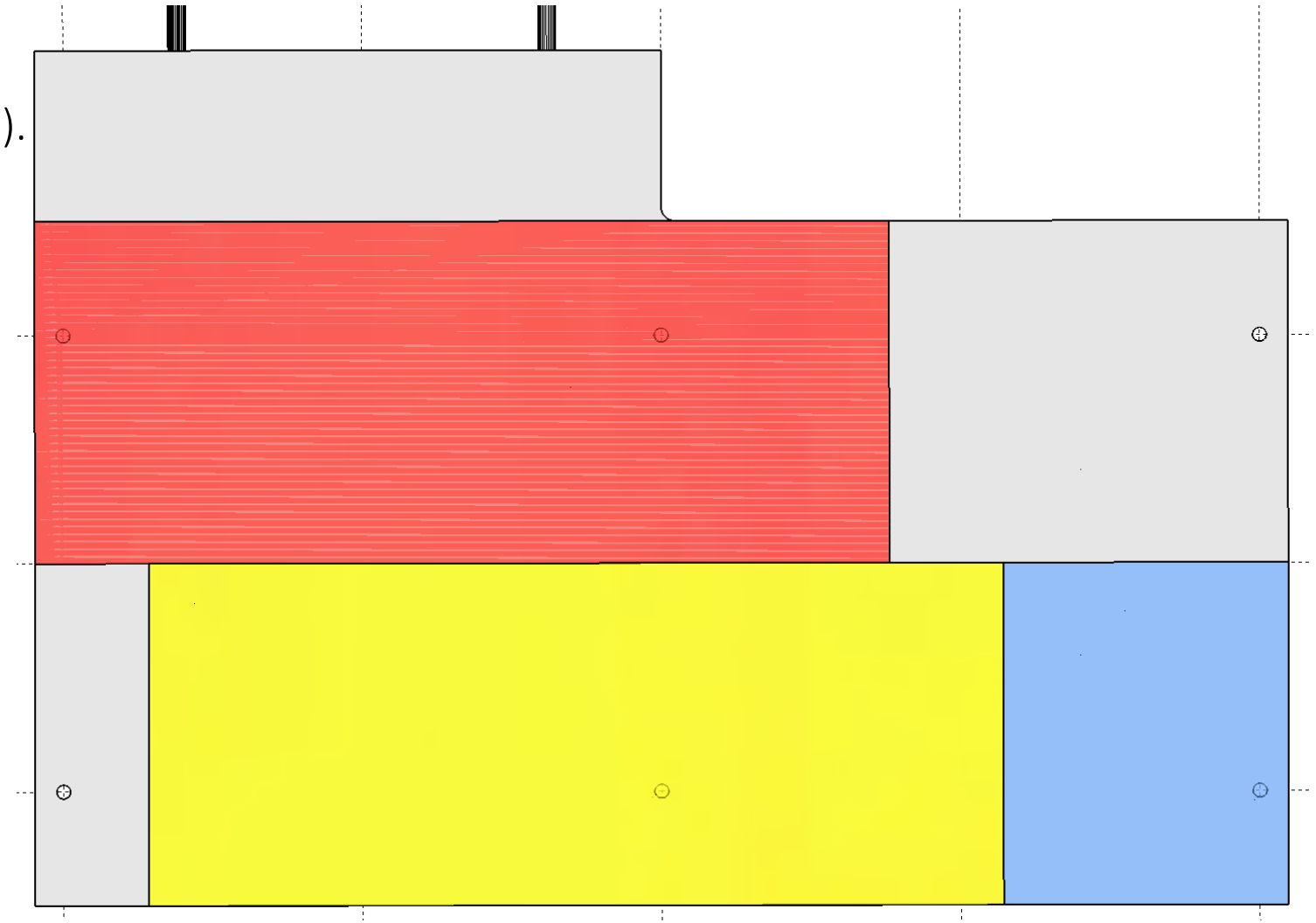
HDR-206142 (Type A)



Cold plate – Thermal padding

Three different thicknesses of thermal pad are necessary. For each thickness, cut a rectangular pad of the indicated dimensions. From a 150 × 150 mm^2 mat, it is possible to make two 1mm thick pads, two 2mm thick pads and six 3mm thick pads.

- 1 mm thick: 150 × 60 mm^2 (red in figure).
- 2 mm thick: 150 × 60 mm^2 (yellow in figure).
- 3 mm thick: 50 × 60 mm^2 (blue in figure).



Readout Unit & Power – Cold plate has been standardized with the RU one

- Procurement status:

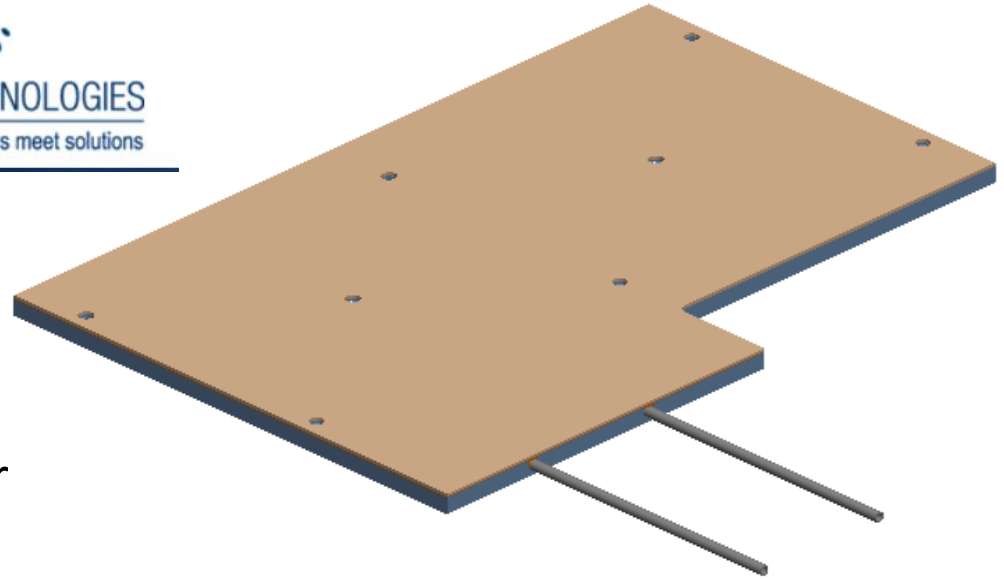
  - Quantity need (included spares) is 490:
    - ITS RU: 220
    - ITS PU: 180
    - MFT : 90

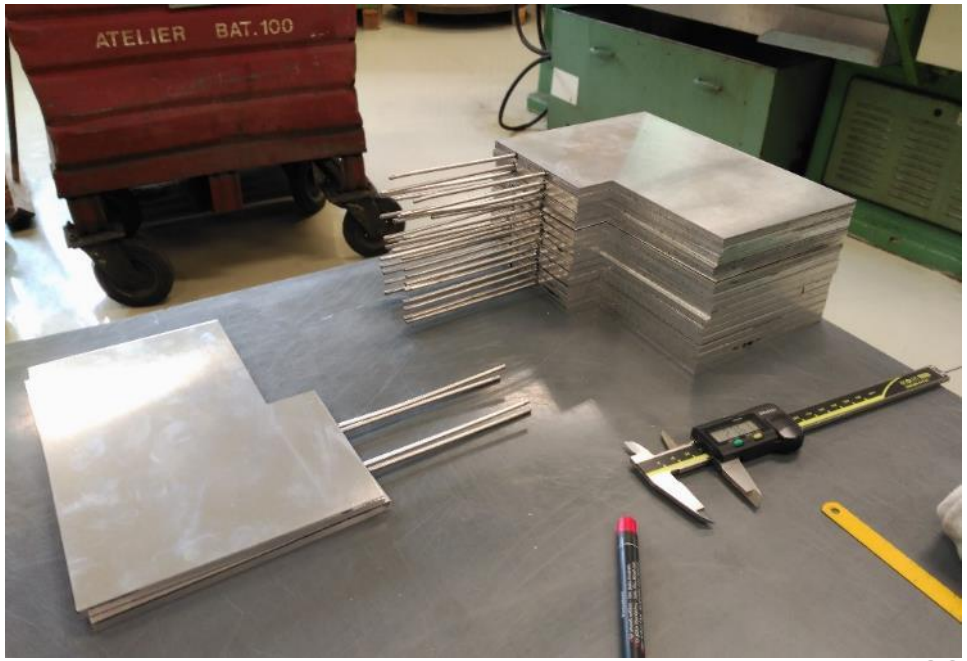
  - Price Enquiry DO-31553/EP/ALICE in july with Purchase order sent out to AMS technologies

https://edh.cern.ch/Document/SupplyChain/DAI/7316926

  - Delivery schedule:
- First lot of 40 units to be delivered directly to US **week 40**
- Remaining components (450) delivery: **week 44**

  - N.24 units produced at CERN, can be delivered to US by the end of **week 35** (all plates produced, piping being cut to lenght and cleaned)



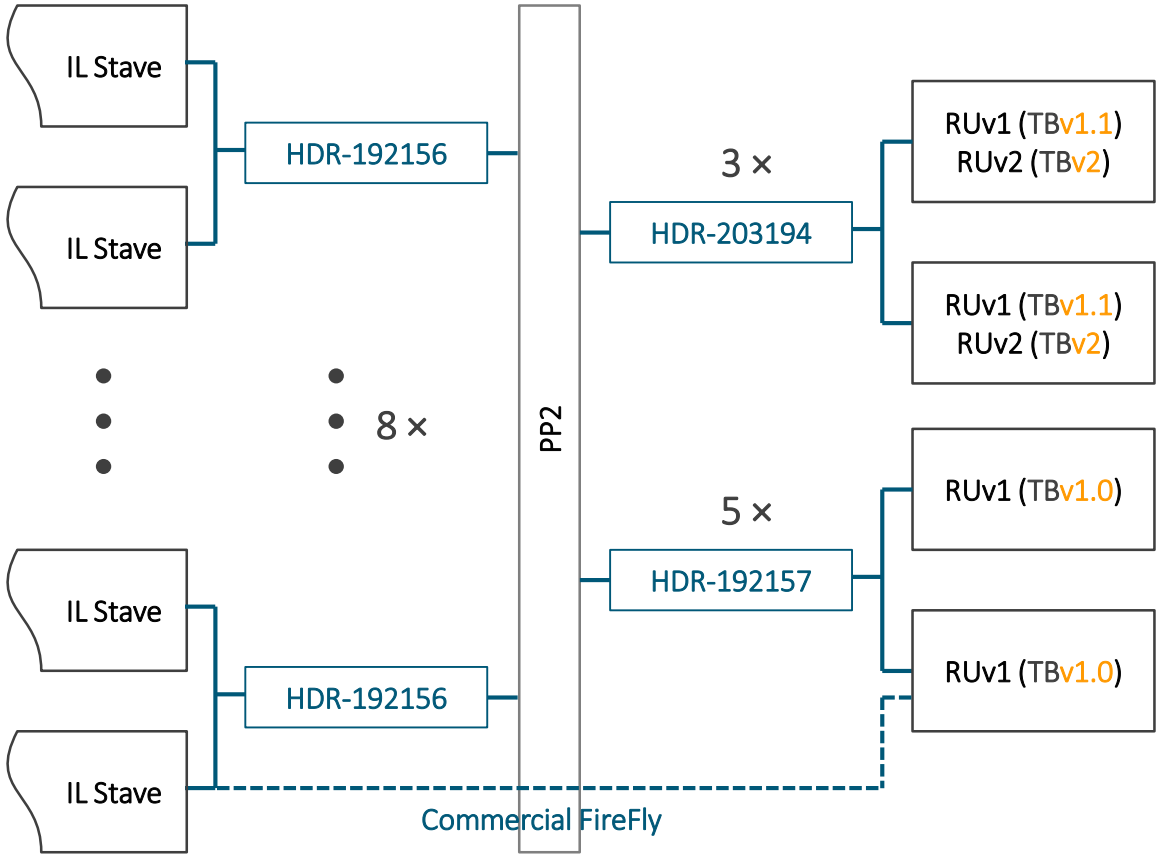


System – many transition boards flavors produced and in production

Austin

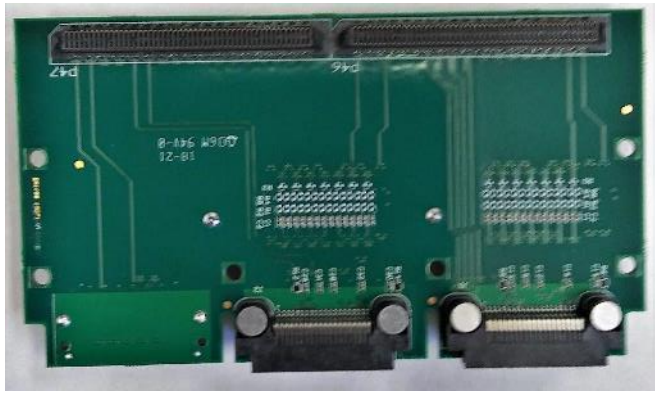
At the moment we have 8 PP2 to PP3 assemblies (HDR-192156), capable to connect 16 IB staves. From PP2 to PP3, we have prototype cables to connect:

- Up to 16 RUv1 (likely 6-7 of them available for commissioning).
- Up to 6 RUv2, as they use the updated PP2 to PP1 data cable (HDR-203194)
- **All PCBs necessary for "cavern" installation already produced, ready in Austin.**



Transition Board v1.0 – compatible with RUv1.x and HDR-192157 cables (**and commercial cables**)

Transition Board v1.1 – compatible with RUv1.x and HDR-203194 cables



Transition Board v2 – compatible only with RUv2 and HDR-203194 cables