MFT Readout Electronics and Power Distribution

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ITS–MFT–O^2 Asian meeting
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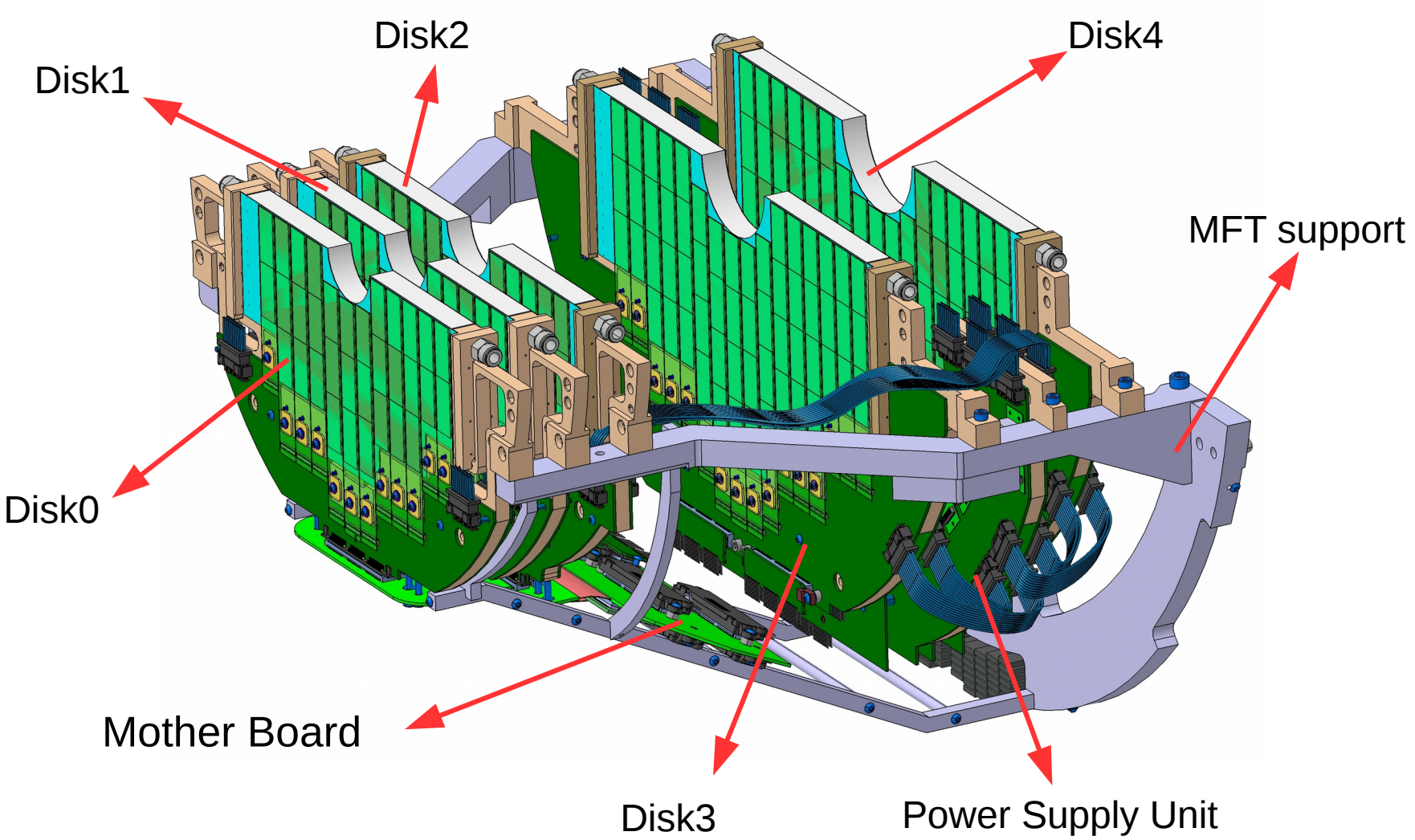
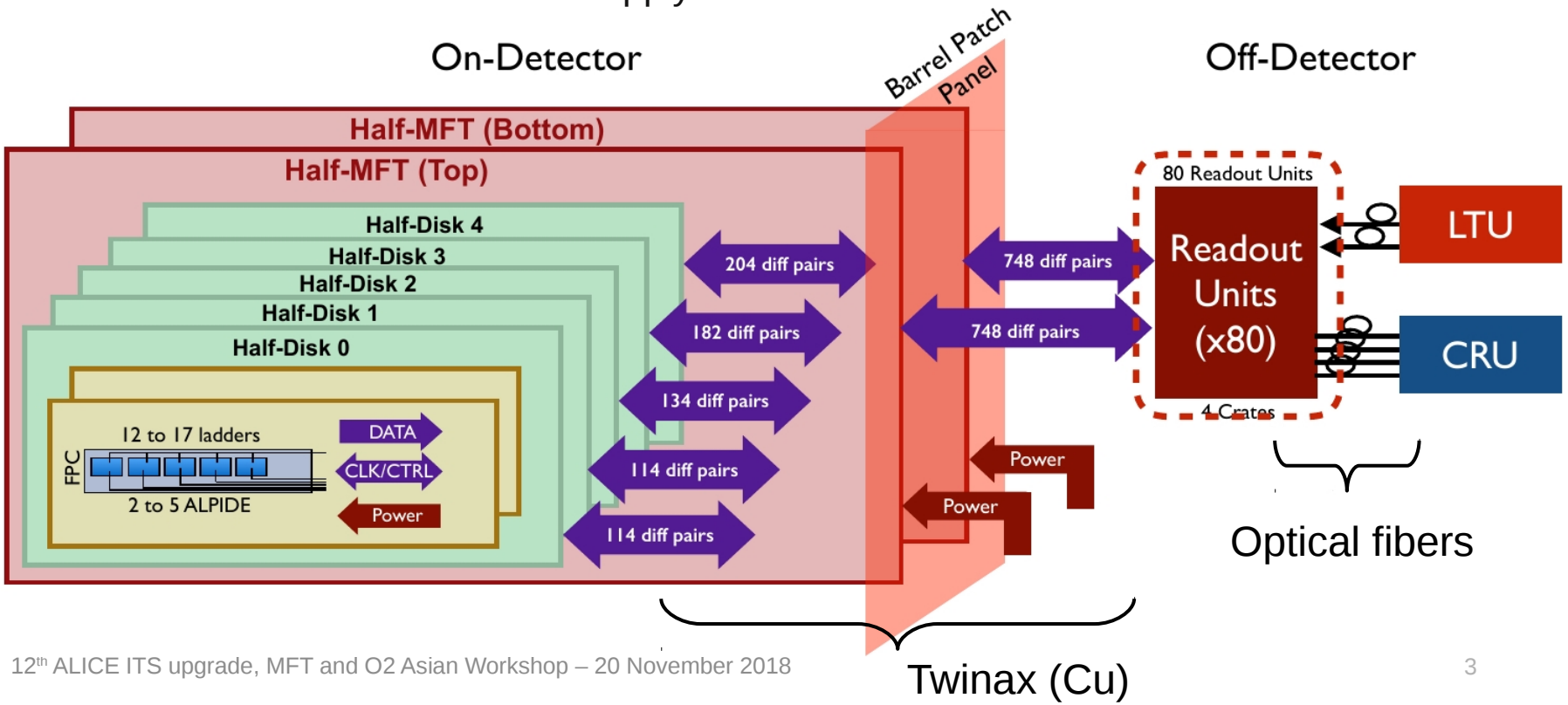
Overview of half MFT



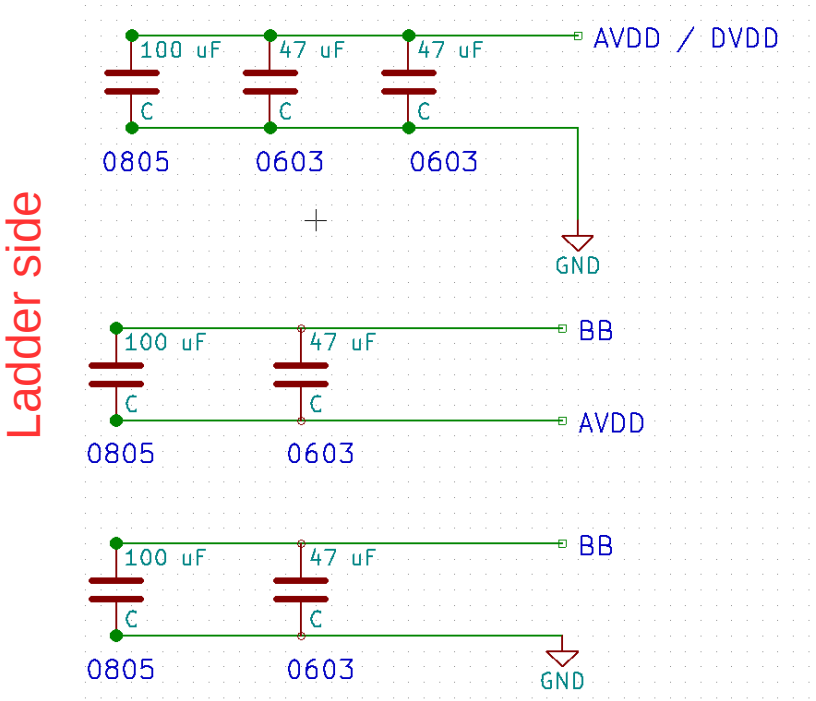
Readout scheme and off-detector components

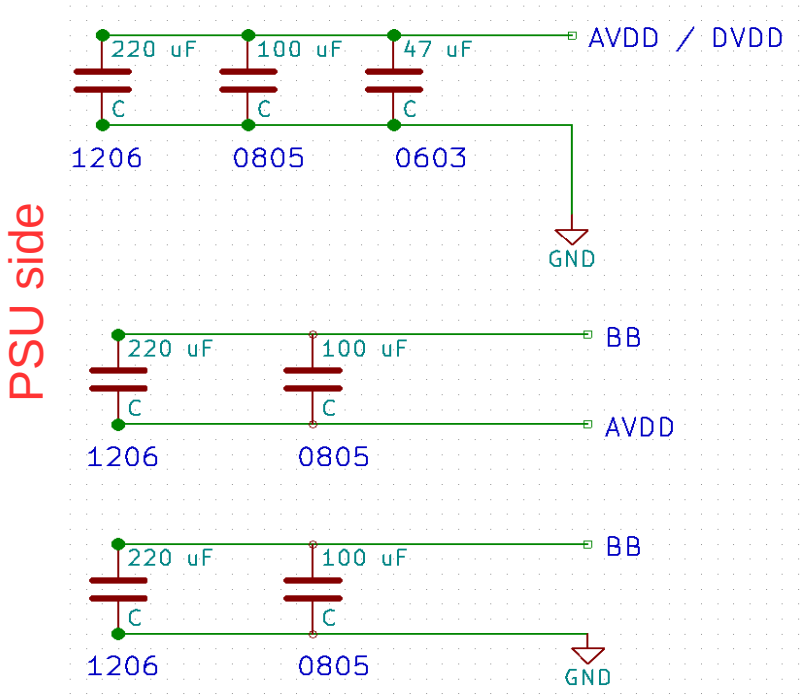
- Between 132 and 272 high speed data signals (1.2 Gb/s) per disk.
- Between 96 and 136 clock and slow control signals per disk.
- Total of 1496 Twinax cables for read-out and control organized in FireFly cables.
- 80 Readout Units (concentrator boards) ~6 m away, where TID about <1 krad.
- Optical fibers organized in trunk cables.
- 10 CRU for data + 1 for Power Supply Unit control and 6 FLPs.



New disk PCBs

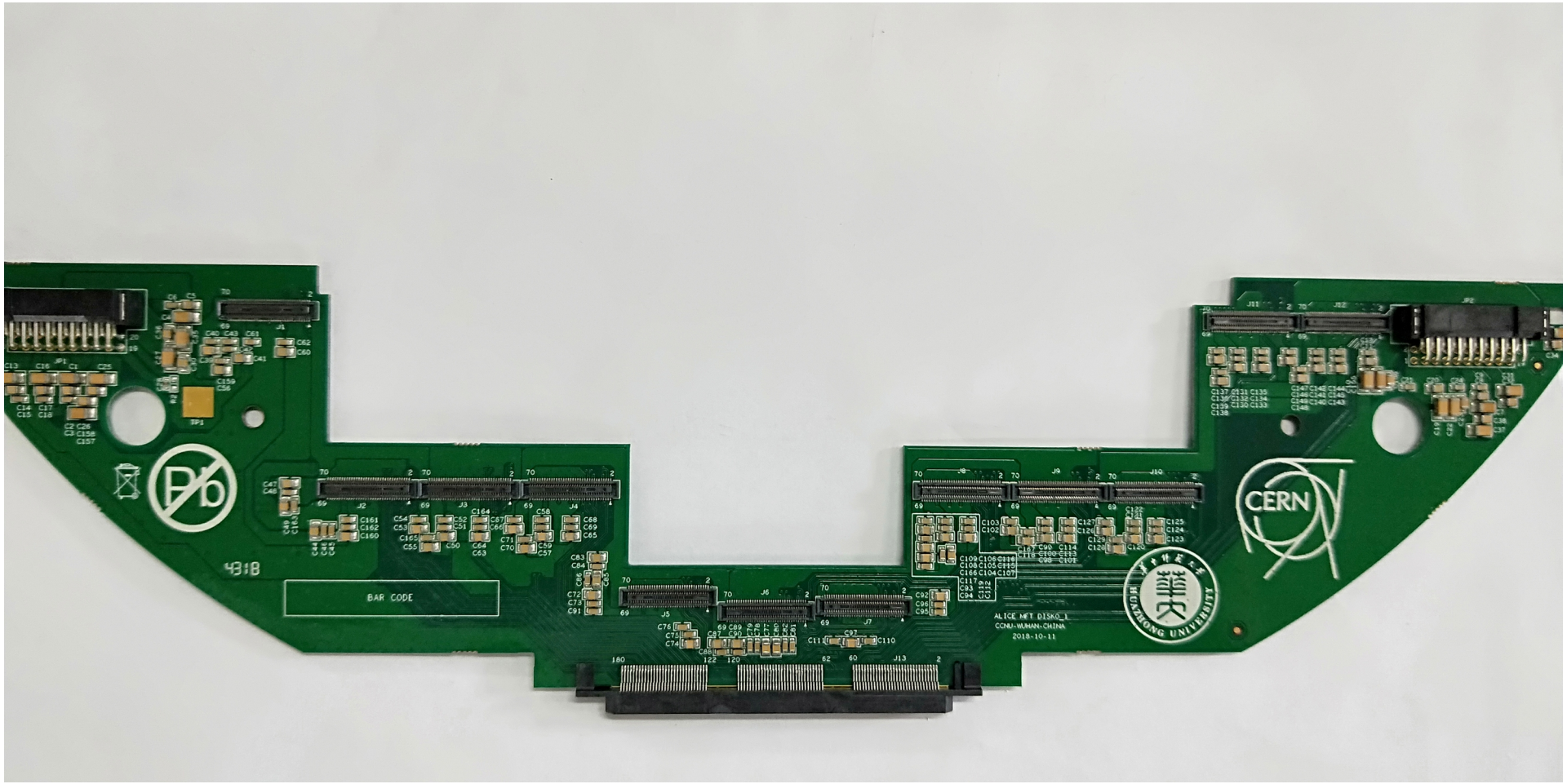
- PCB prototypes of disks 0/1, 2 and 4 already produced and working well.
- New version of disk 0/1 PCB (disk 0/1) with improved capacitors has been produced and it's currently being validated in French labs (metrology and electrical tests).
- The other PCBs will follow the same strategy.



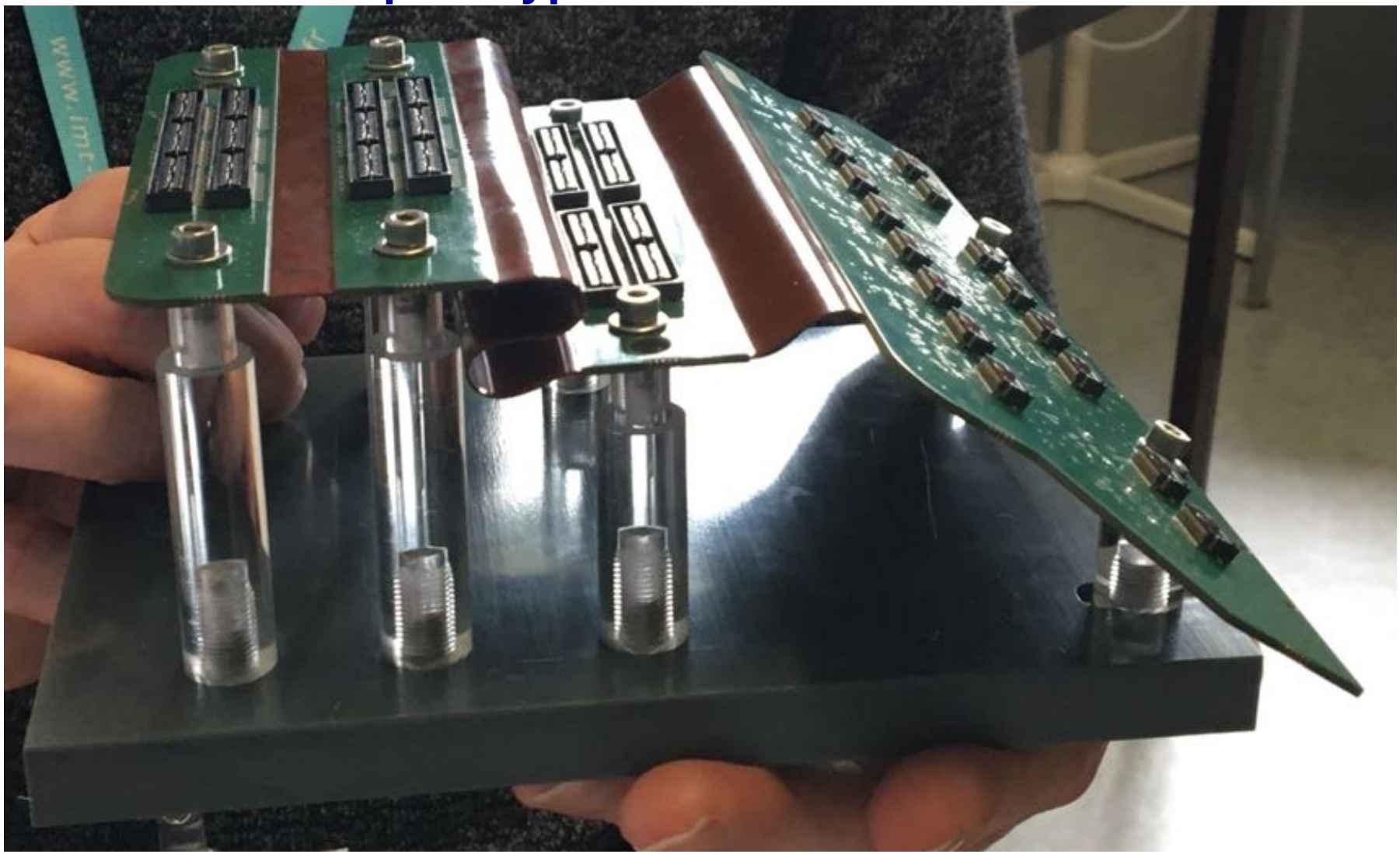


New disk PCB 0/1

- All capacitors below ladder and power connectors to avoid mechanical interference.

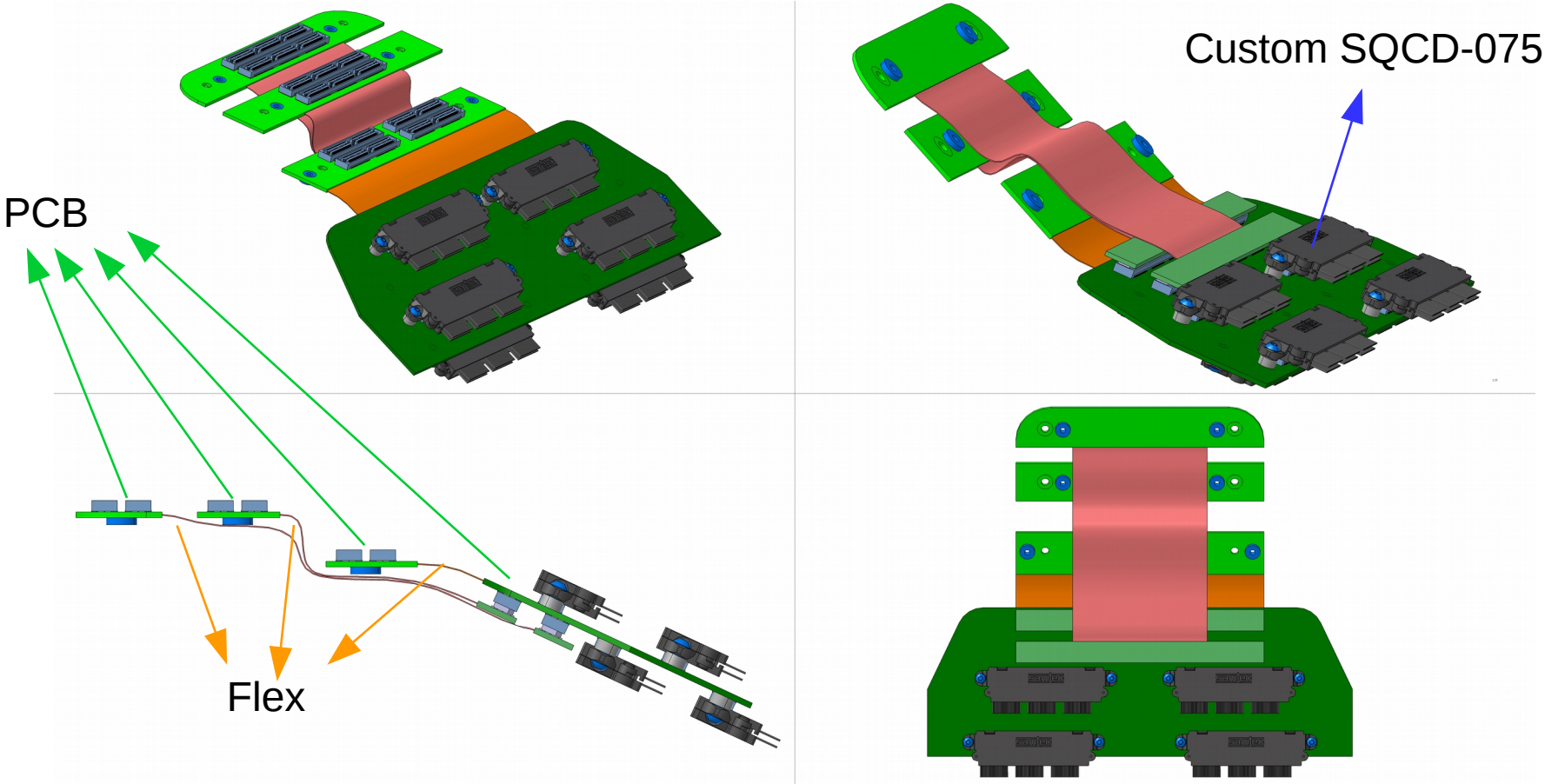


MB012 – first prototype



Mother Board 012 – new version

- A new Mother Board must be designed: 4 PCBs connected by 3 **independent** flex **SIGN/GND/SIGN** → 3 independent cards (MB0, MB1 and MB2).

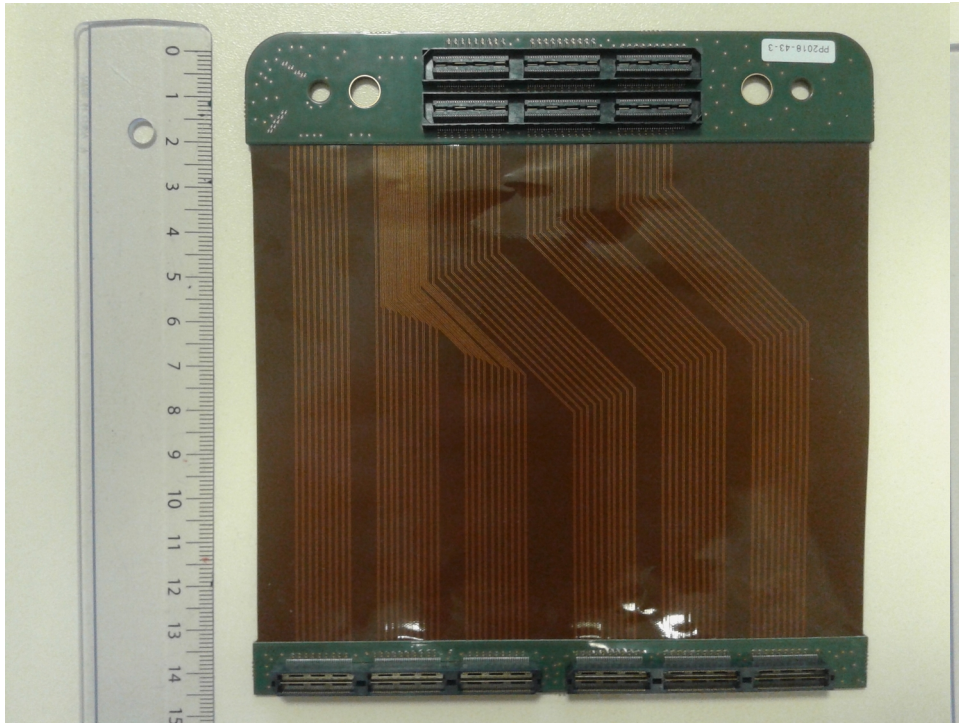


- MB0 = MB1, except for the size.

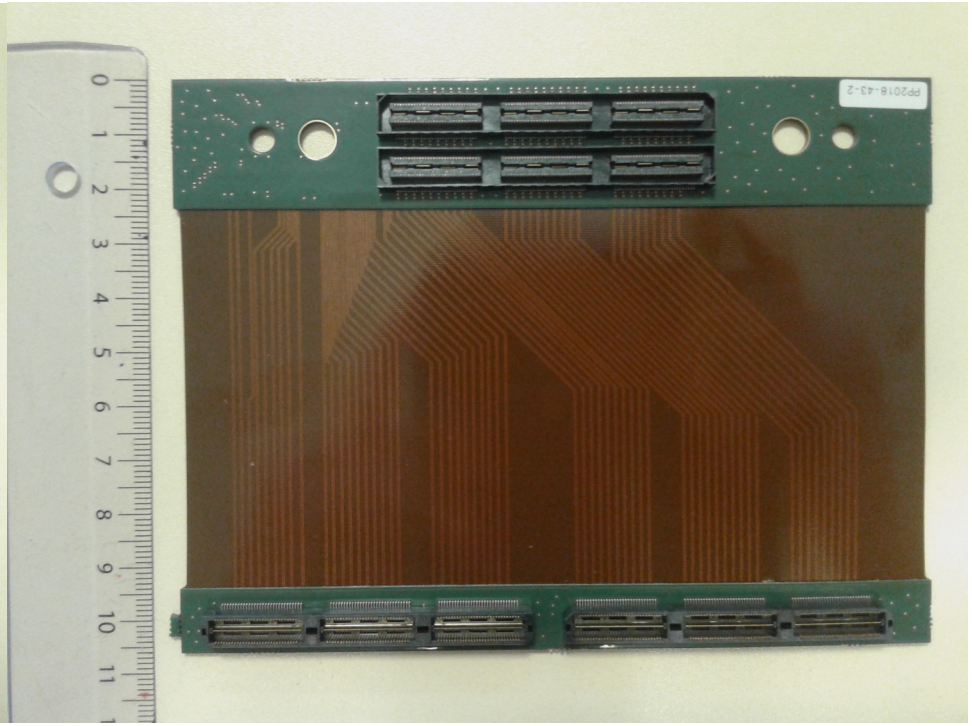
Mother Board for disk 0 and 1

- 3 prototypes of each types now produced: 1 in Nantes for metrology, 1 in Lyon to integrate the test bench and 1 in Saclay for electrical checks.

Mother Board – disk 0

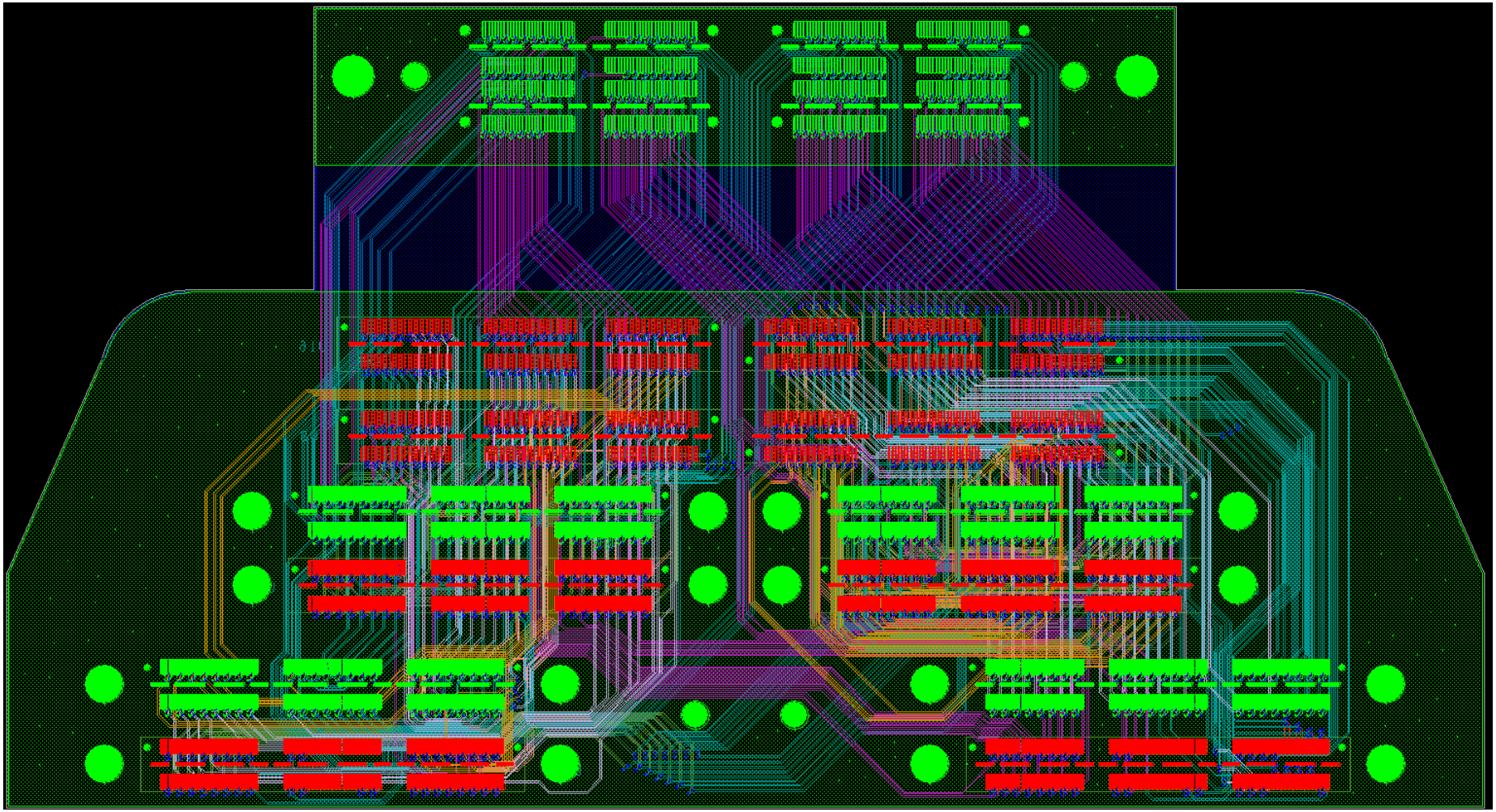


Mother Board – disk 1



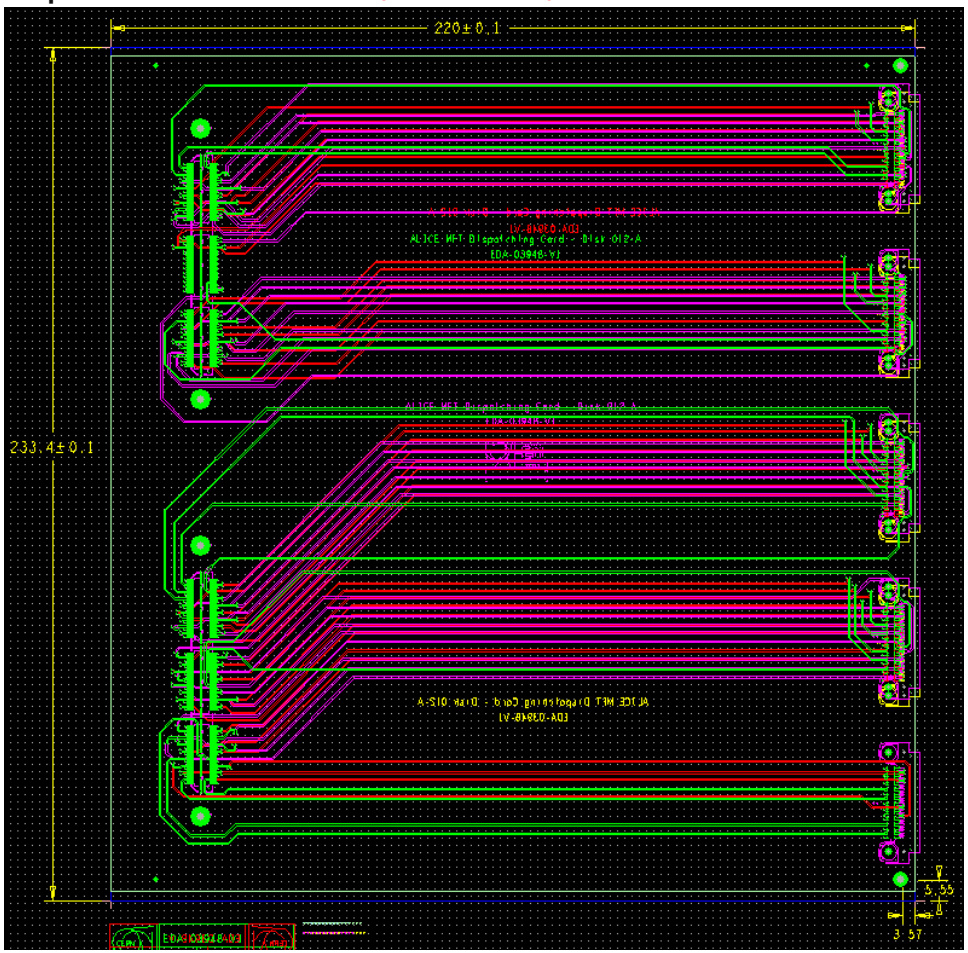
Mother Board disk 2

- Layout of MB2 almost completed.



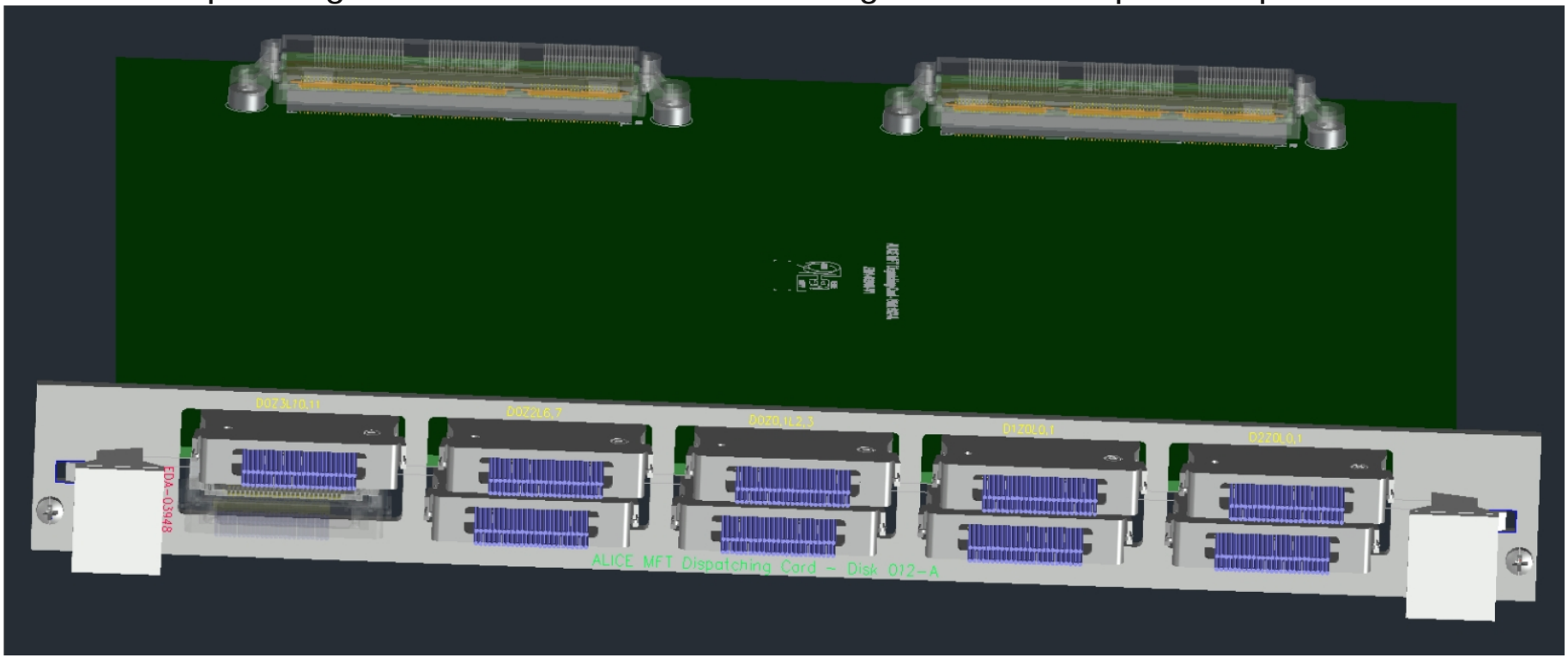
Dispatching cards

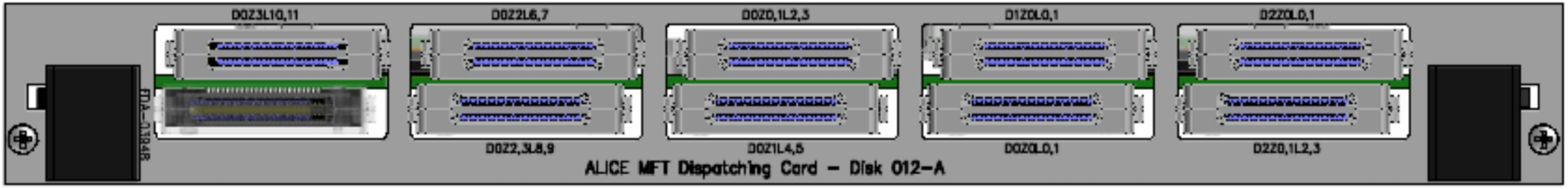
- RU can accept as input only one ladder per slot → some dispatching cards are needed.
- To be hosted in the RU crate.
- 4 cards to be developed: 2 for Disks 0, 1 and 2, 1 for disk 3 and one for disk 4.



Dispatching cards

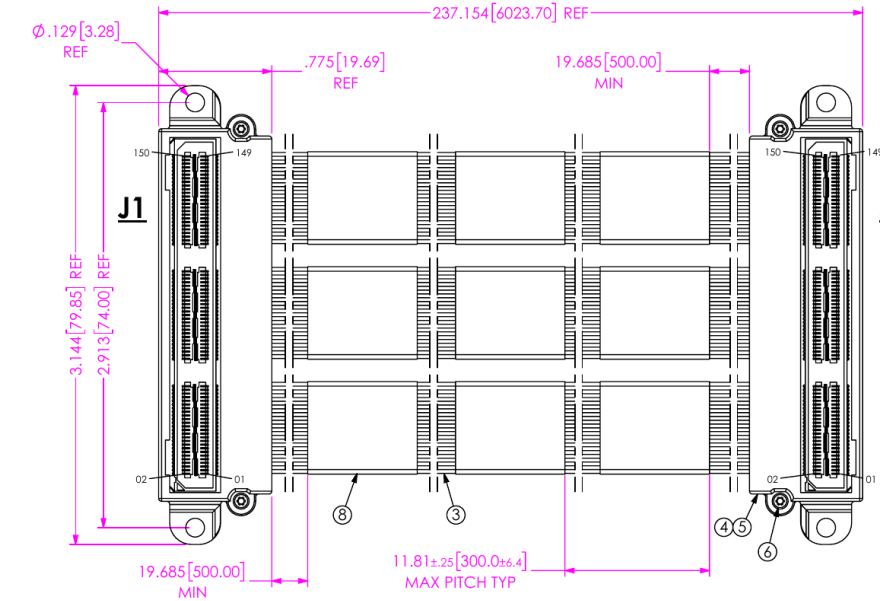
- First dispatching card finalized at CERN. Working now to develop a front panel.

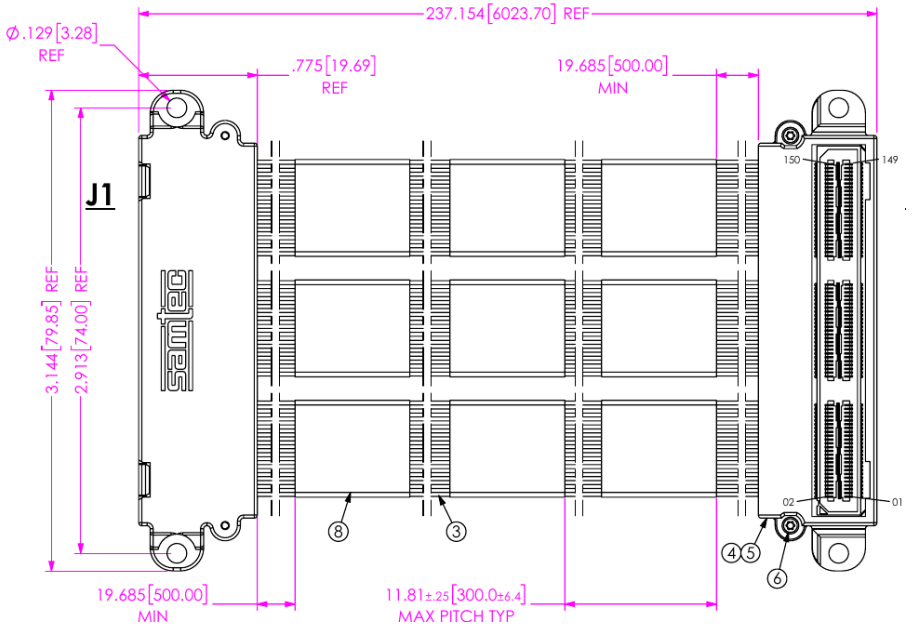


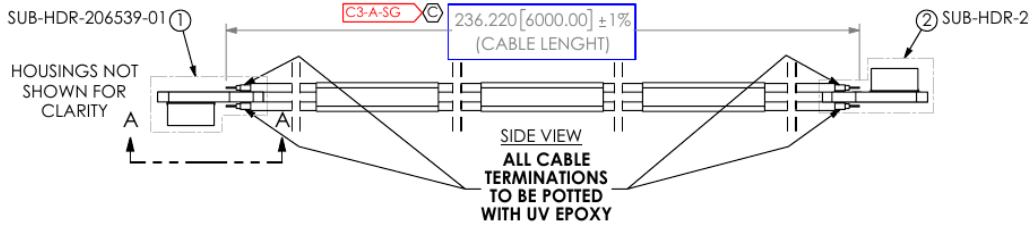


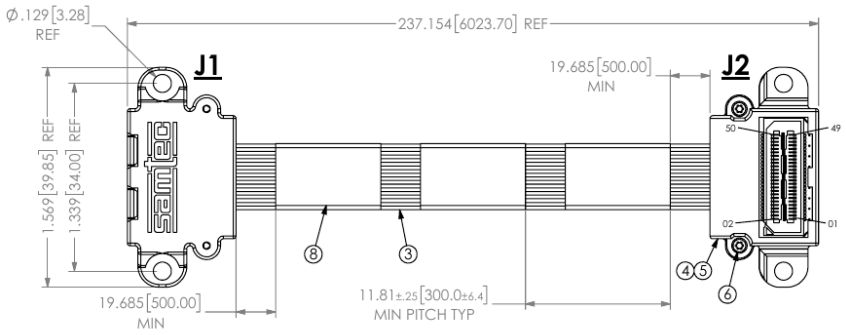
Cables from cone to RU crates

- Big variety of cables to minimize the volume in the cone.
- 4 types from disks/PSU to patch panel and 4 from patch panel to RU crates.
- Pinout and wrapping finalized with Samtec.



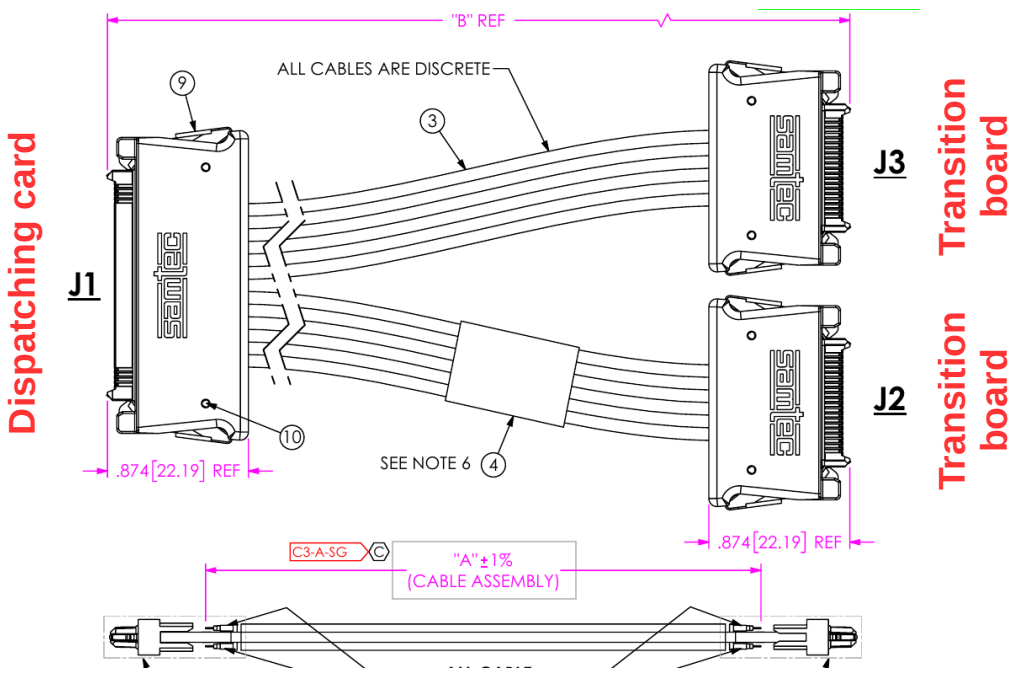






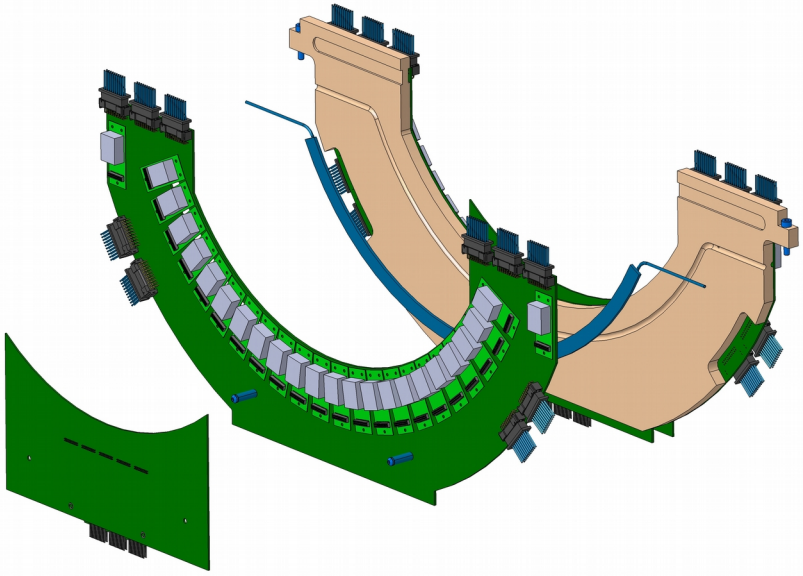
Cables for RUs

- Other cables must be developed to connect the dispatching cards to the readout unit.
- Correspondence 1:1 ladder-transition board input.
- Samtec asked to modify the cable used by ITS. Prints now finalised.
  - less differential pairs (8 instead of 12);
  - smaller connectors on dispatching cards.



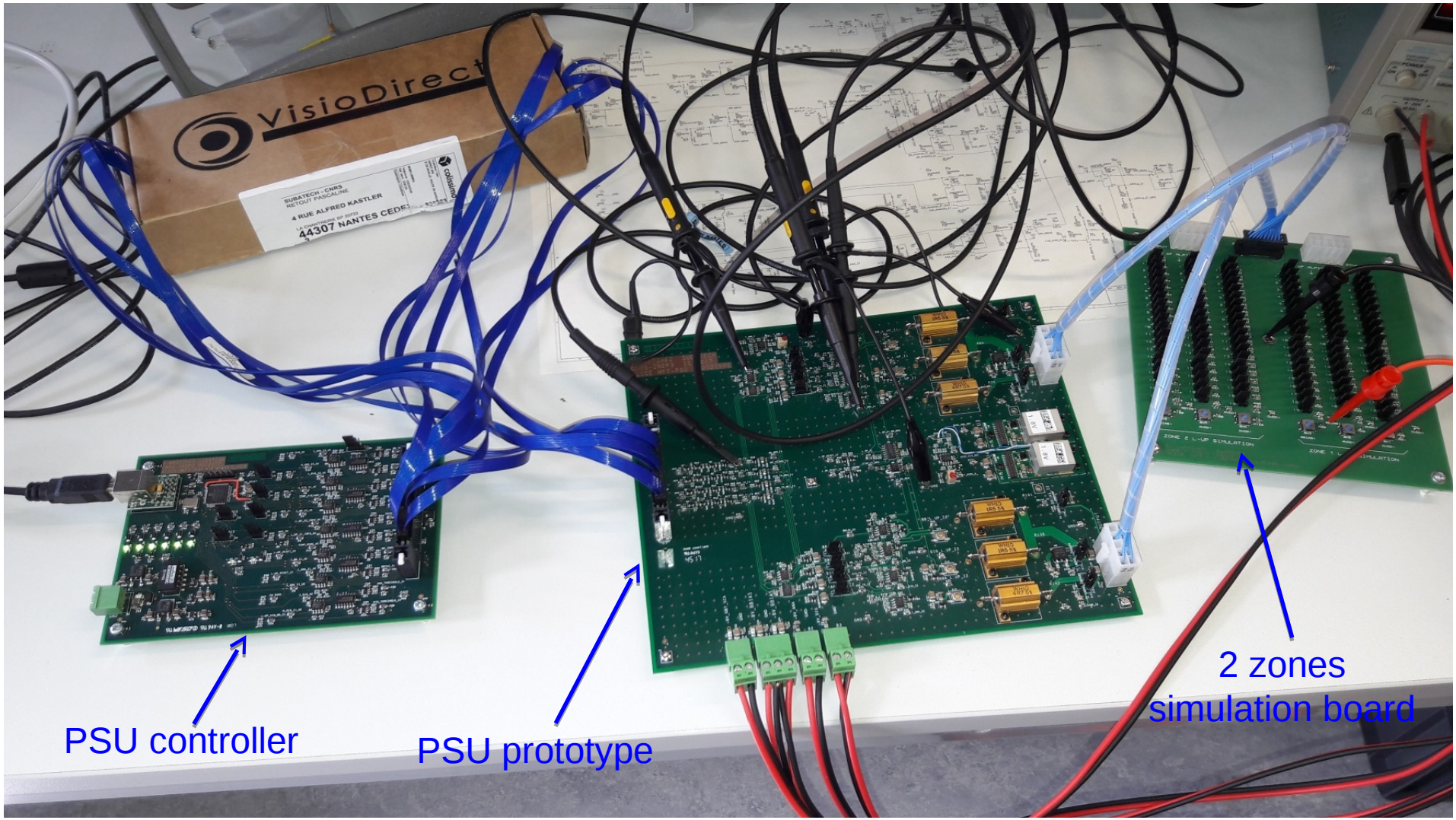
SIGNAL MAPPING							
J1	TYPE	J2	J3	J1	TYPE	J2	J3
1	GND	2	-	2	GND	1	-
3	DP	4	-	4	DP	3	-
5	DP	6	-	6	DP	5	-
7	GND	8	-	8	GND	7	-
9	DP	10	-	10	DP	9	-
11	DP	12	-	12	DP	11	-
13	GND	14	-	14	GND	13	-
15	DP	16	-	16	DP	15	-
17	DP	18	-	18	DP	17	-
19	GND	20	-	20	GND	19	-
21	DP	22	-	22	DP	21	-
23	DP	24	-	24	DP	23	-
25	GND	26	25	26	GND	25	26
27	DP	-	23	28	DP	-	24
29	DP	-	21	30	DP	-	22
31	GND	-	19	32	GND	-	20
33	DP	-	17	34	DP	-	18
35	DP	-	15	36	DP	-	16
37	GND	-	13	38	GND	-	14
39	DP	-	11	40	DP	-	12
41	DP	-	9	42	DP	-	10
43	GND	-	7	44	GND	-	8
45	DP	-	5	46	DP	-	6
47	DP	-	3	48	DP	-	4
49	GND	-	1	50	GND	-	2
ALL GND COMMON AND TIED TO CABLE SHIELD AND CONNECTOR LATCHES (6PLCS)							
J2 & J3 PINS NOT LIST ARE NC							

Power Supply Unit: design constraints

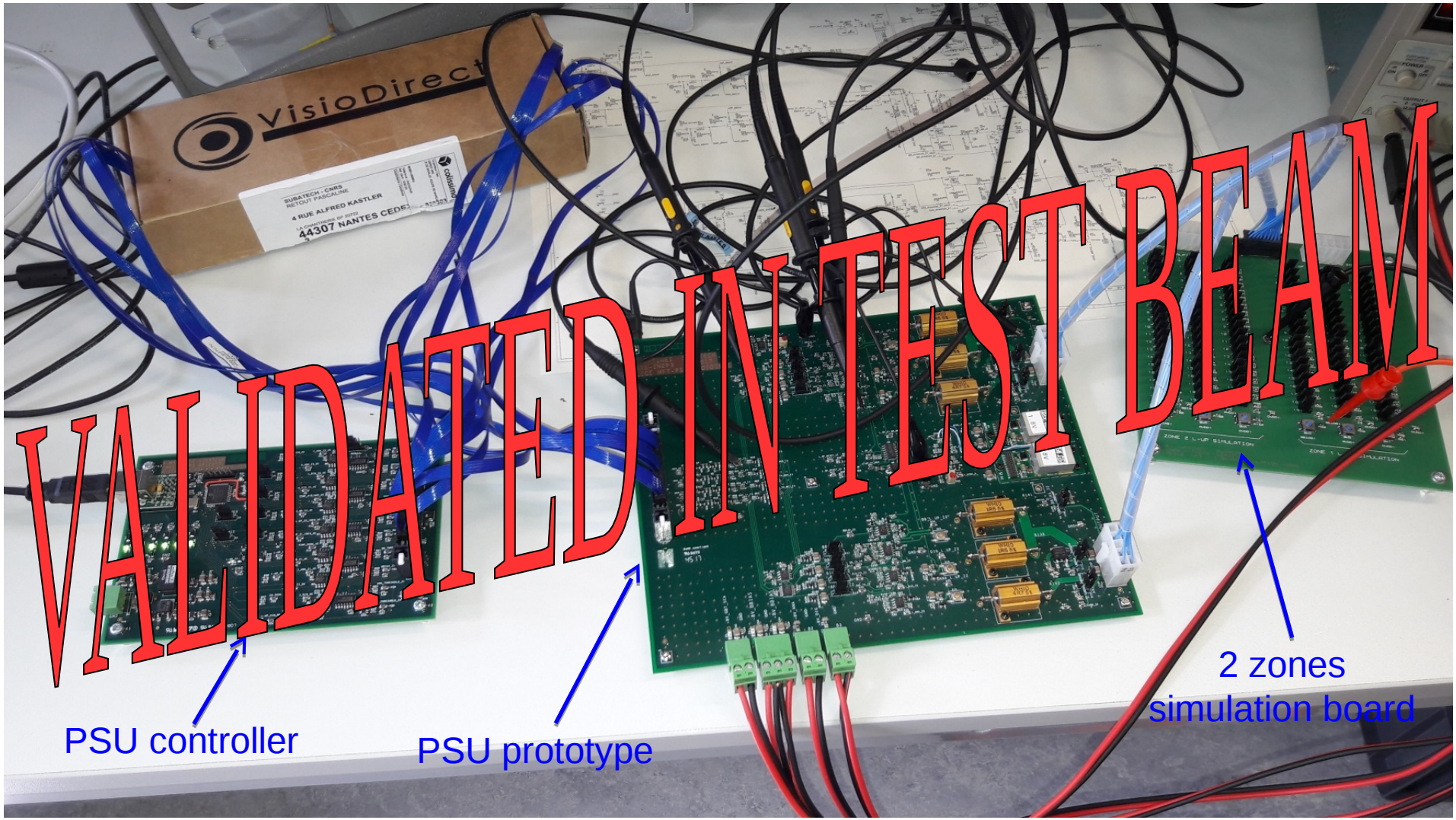


- MFT Power Supply Unit features:
  - Four PSU for total MFT
  - One PSU provides power for five half planes
  - Separated Analog and Digital power supply (1,8V)
  - BBIAS negative votlage generation [0 ; -3V]
  - Latch-up detection on each output and each zone
  - Voltages, currents and temperatures monitoring via GBT-SCA
  - BBIAS voltage and latch-up current threshold control via GBT-SCA
  - Radiation tolerant components (up to 75krad)

PSU prototype



PSU prototype



Power Supply Unit – prototype optimization

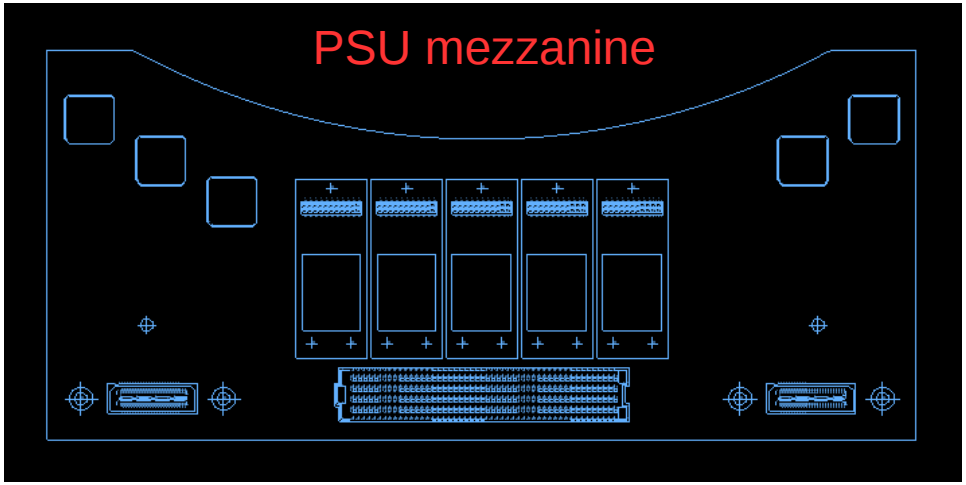
- Some optimization implemented and validated with the prototype

  1) New operational amplifiers to improve the measure of the currents.

  2) MUX system improved with transistor to better deal with high irradiation.

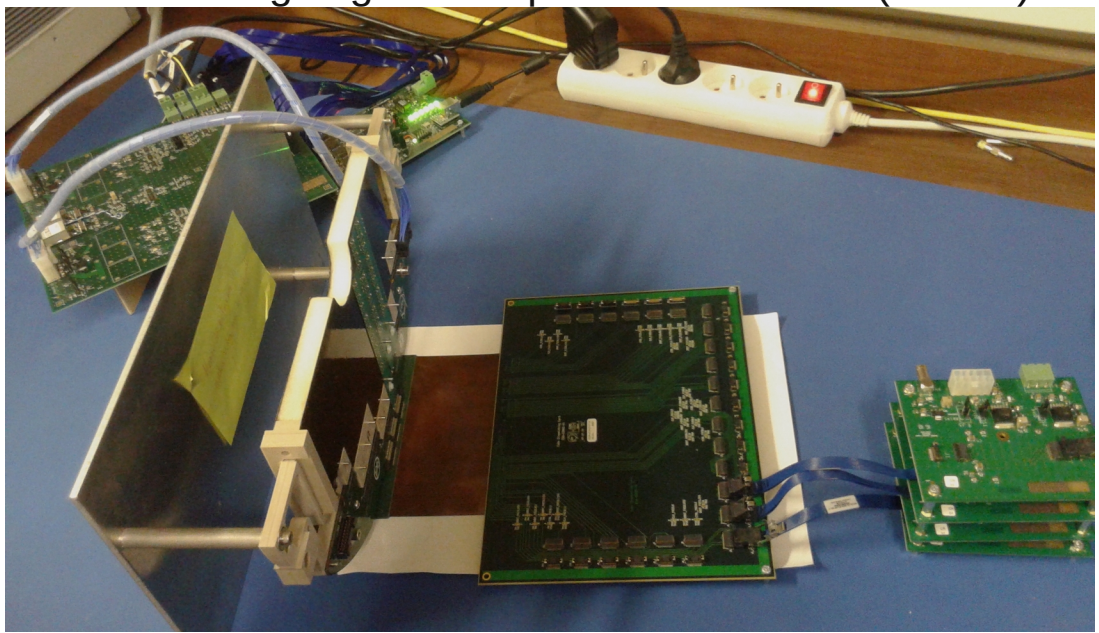
  3) Possibility to know which line (AVDD, DVDD or BB) caused a latch-up.

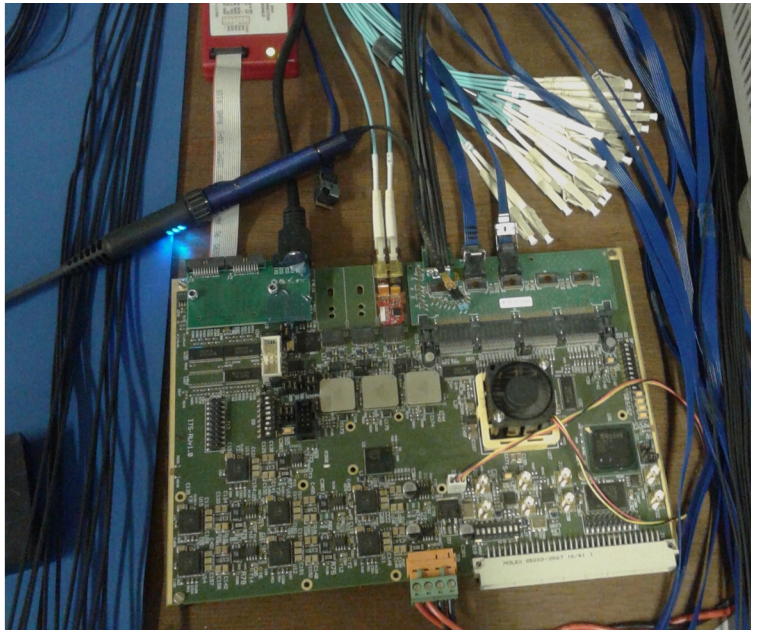
  4) System to shut-down analog or digital line in case of DCDC failure of digital or analog line in the same zone → tested in simulation.
- Mechanical design of PSU main+mezzanine finalized.
- Schematics ready, working on layout (DCDC and main connectors placed, pinout defined).



Signal integrity measurements

- Present setup in Lyon include:
  - half-disk prototype used for test bench (3+3 ladders of 3 chips each)
  - PSU prototype
  - MB0 or 1
  - fake MB2
  - fake dispatching card
  - transition board
  - RUv1.0
- 8 m long SAMTEC custom made cable between fake dispatching card and RU.
- Total of 8 connections ladder. They will be 9 (max) in real life → quite realistic test bench.
- Test ongoing with chips in PRBS mode (1.2 Gb).





Backup slides

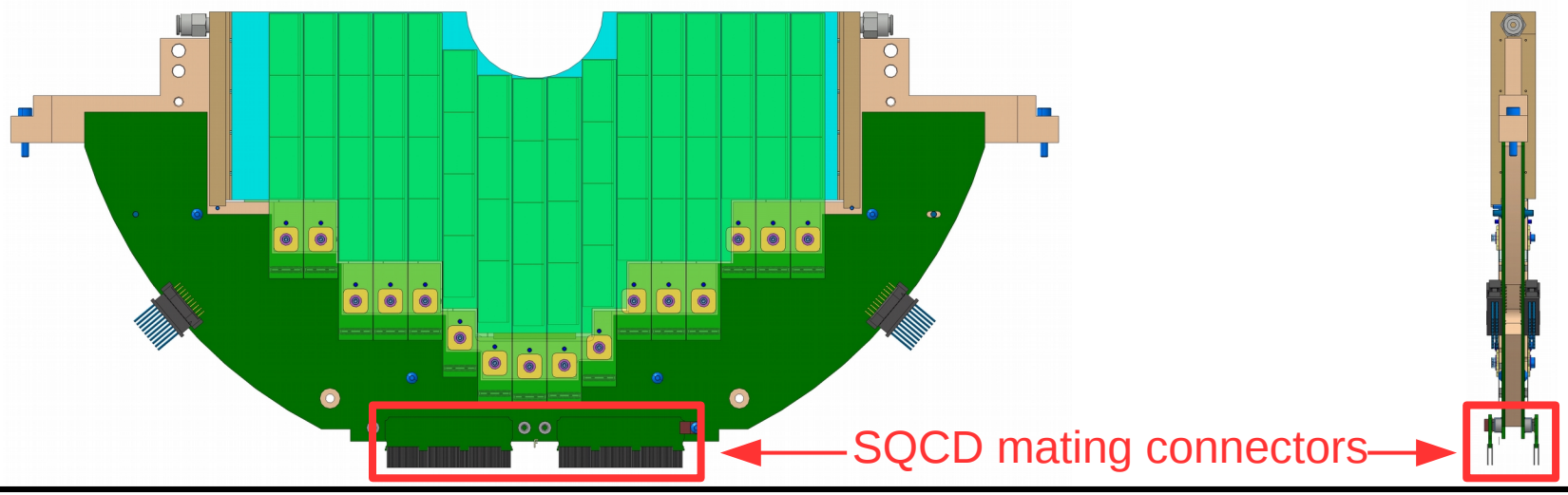
MFT readout design requirement

- Functions:
  - transfer data signal to the outside world (RU, CRU…);
  - provide clock and slow control signals to the chip;
  - provide power (analog, digital and back bias) and ground to the chips;
  - transfer supplementary data from sensors (voltages, currents, temperature control).

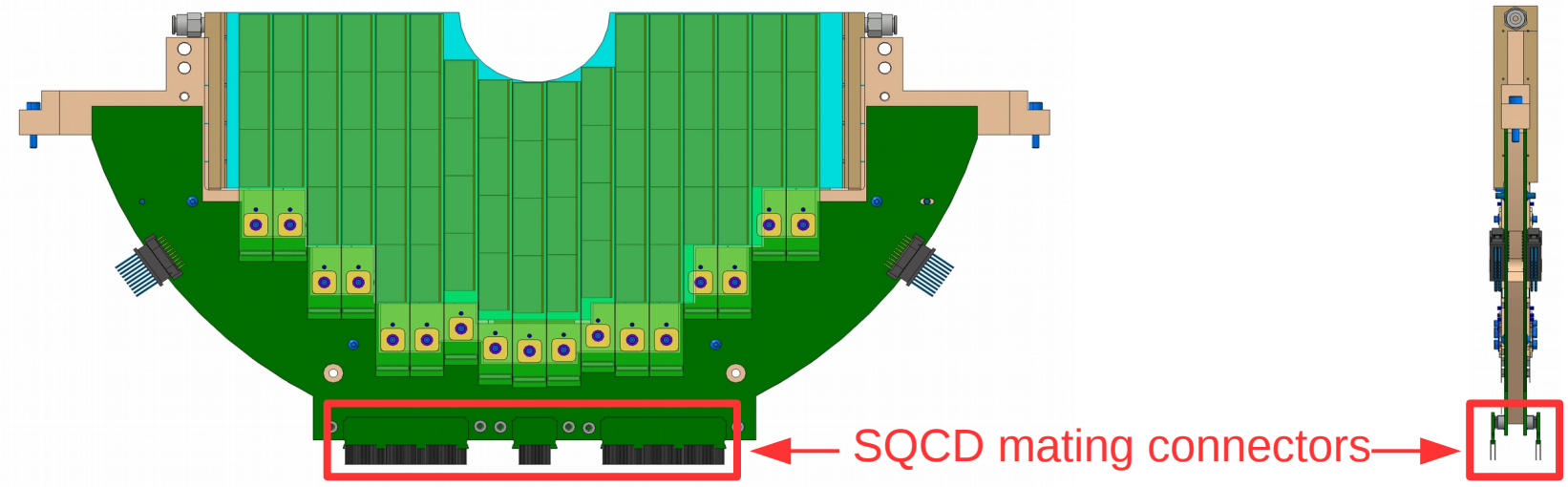
- Constraints:
  - preserve data signals up to 1.2 Gb/s;
  - very limited space on all on-detector components;
  - data from sensors should be integrated in the data flow.

New disk design without MB3+PSU and MB4

Disk3

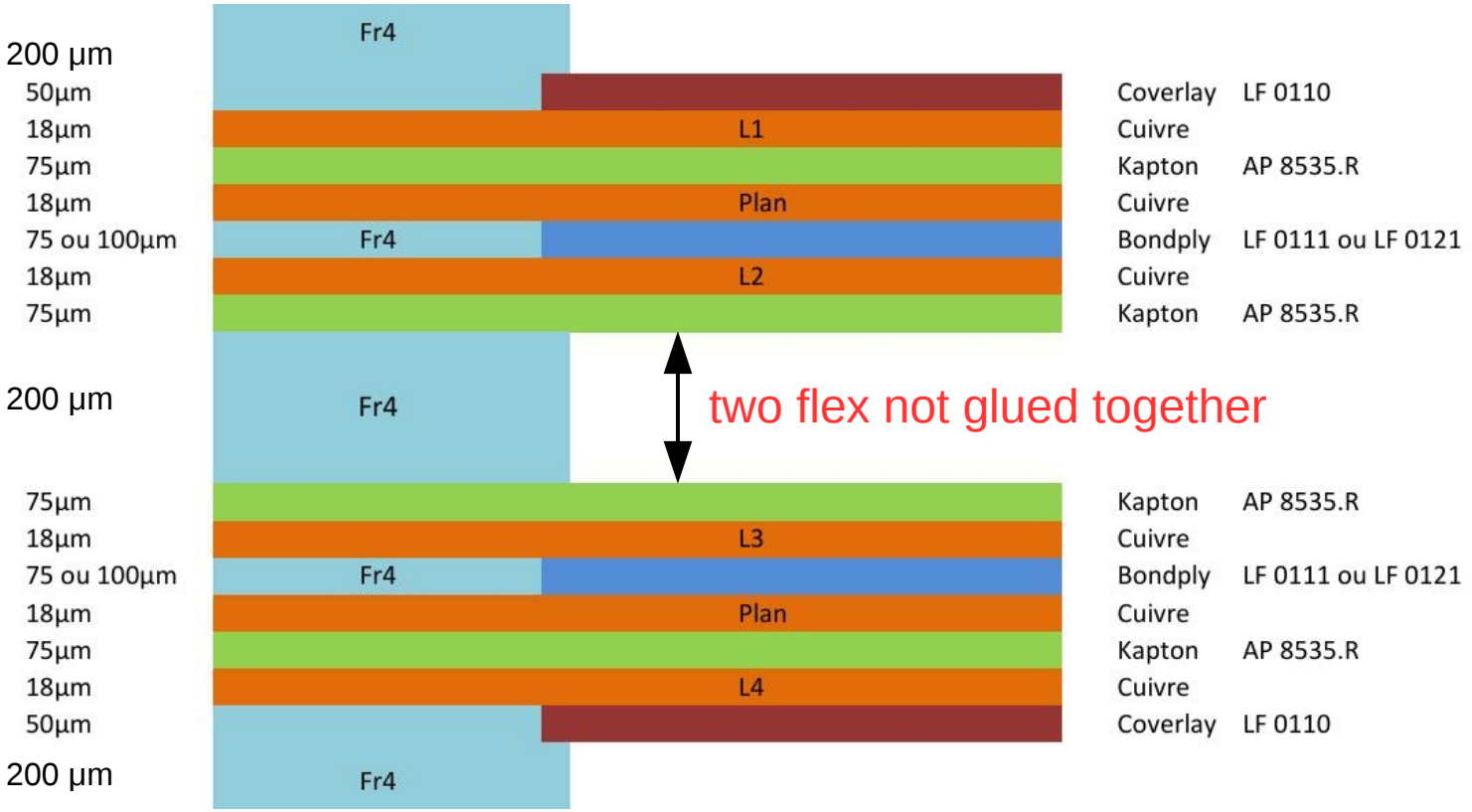


Disk4



Mother Board 012

- 2x3 layers in the flex: **SIG/GND/SIG + SIG/GND/SIG**.



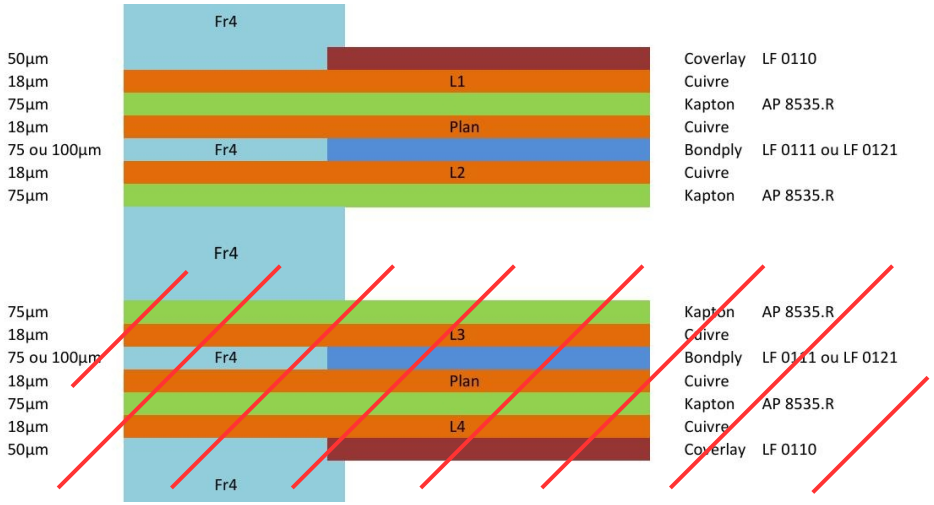
- Stack-up discussed with Techci in order minimize the rigidity of the flex.
- 100 Ω of equivalent impedance between P and N, 50 Ω between the GND are the only constraints.

Proposed stack-up of the new Mother Board 0 and 1

- Proposed stack-up (dielectric not considered).
- ½ of the old Mother Board stack-up.

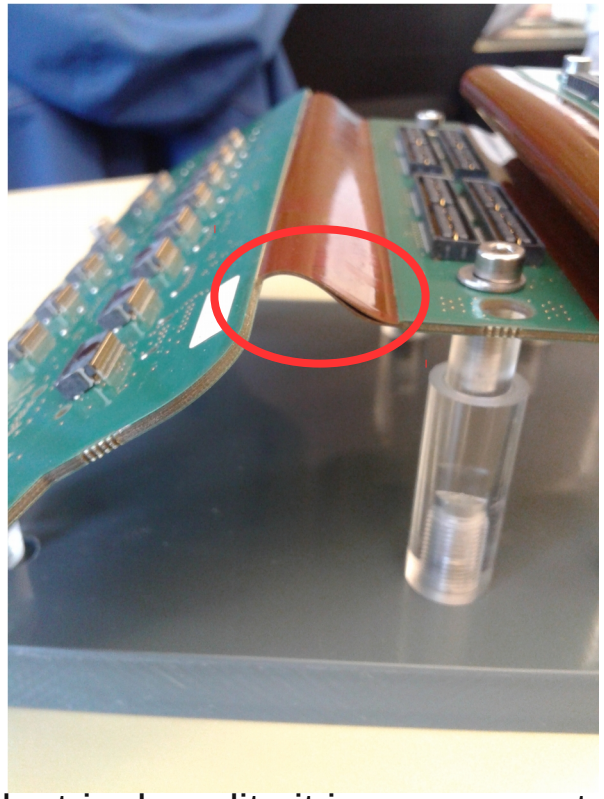
PCB	FLEX	PCB
Top		Top
Layer 1 (SIGN)	Layer 1 (SIGN)	Layer 1 (SIGN)
GND	GND	GND
Layer 2 (SIGN)	Layer 2 (SIGN)	Layer 2 (SIGN)
Bottom		Bottom

Old Mother Board



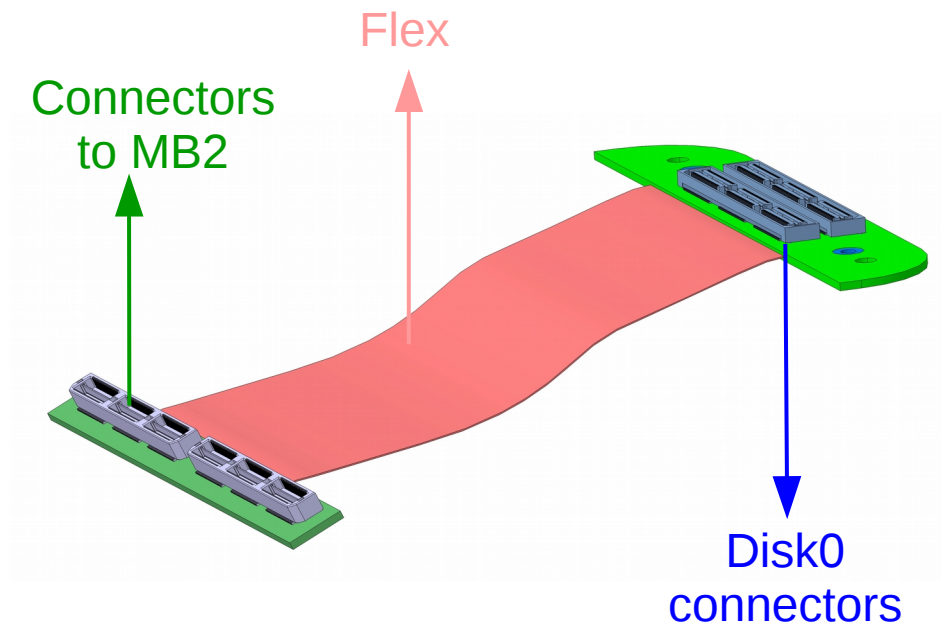
Flex rigidity

- Flex part of the Mother Board turned out to be too rigid, despite all the optimizations.
- Signals and ground layers (Cu) are the reason of such a rigidity.

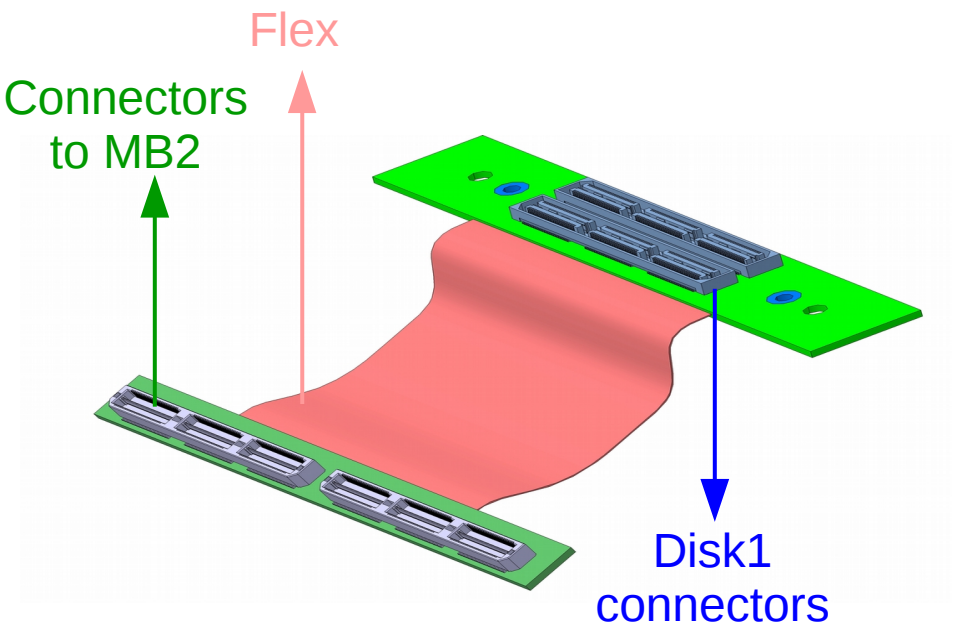


- To route all the signals and to guarantee a good electrical quality it is necessary to keep three layers of copper per disk.
- Solution→change the Mother Board design decoupling the three disks without changing their position in the cone (see next slides).

Design of MB0 and MB1

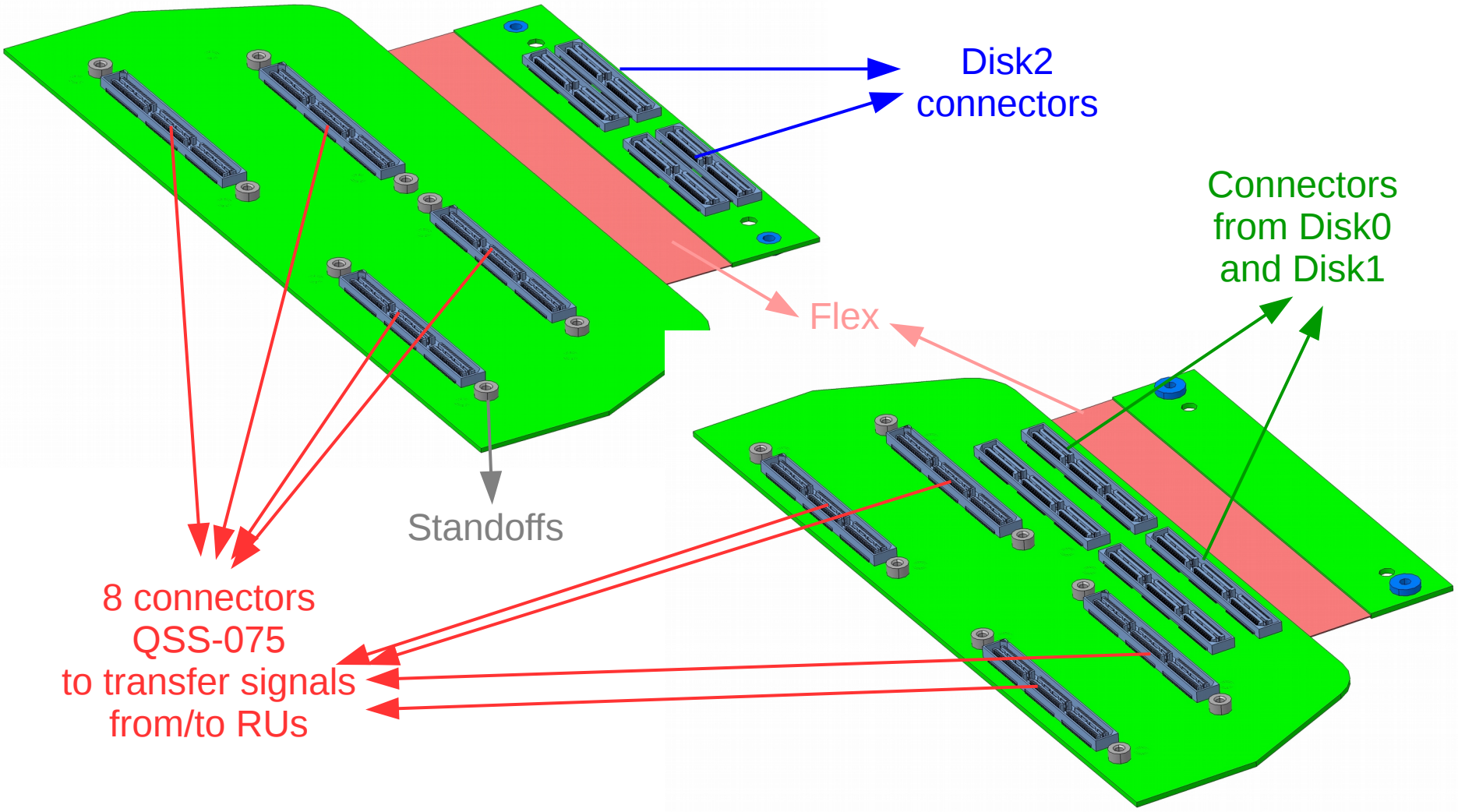


MB0



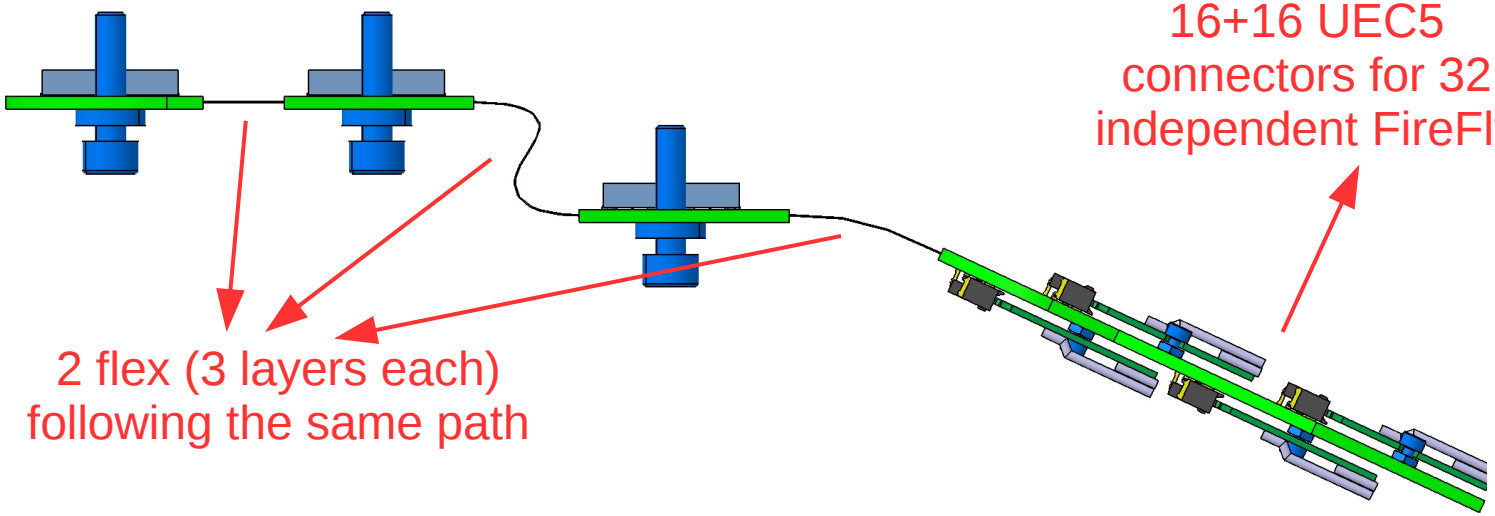
MB1

Design of MB2

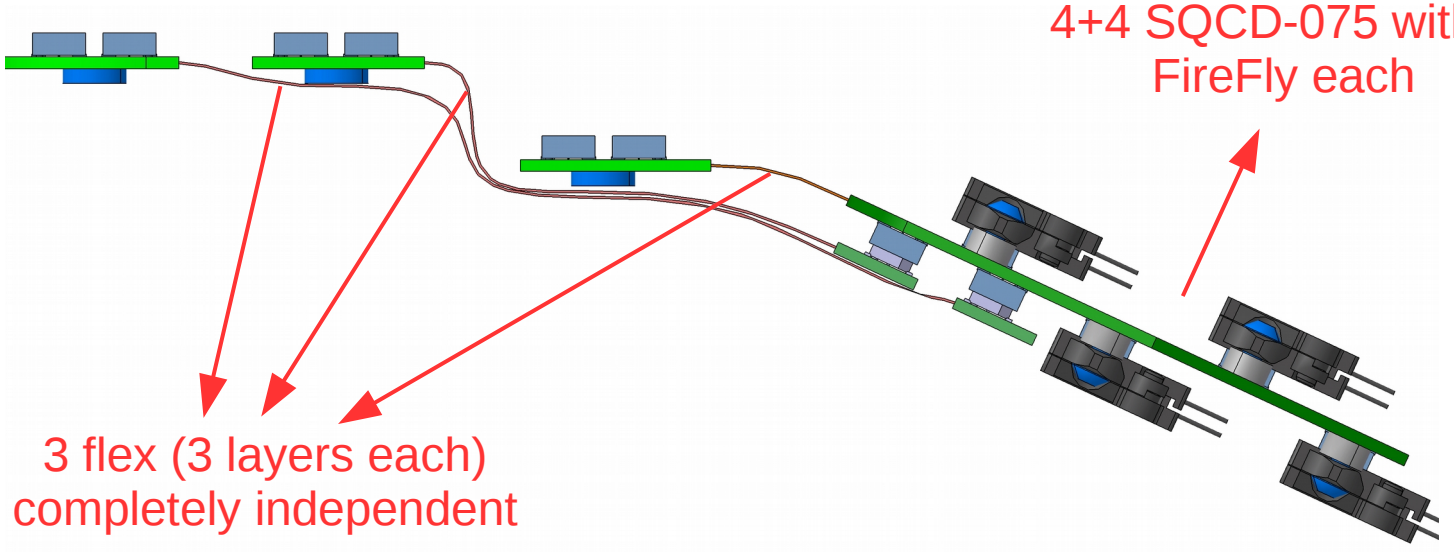


Old vs new Mother Board

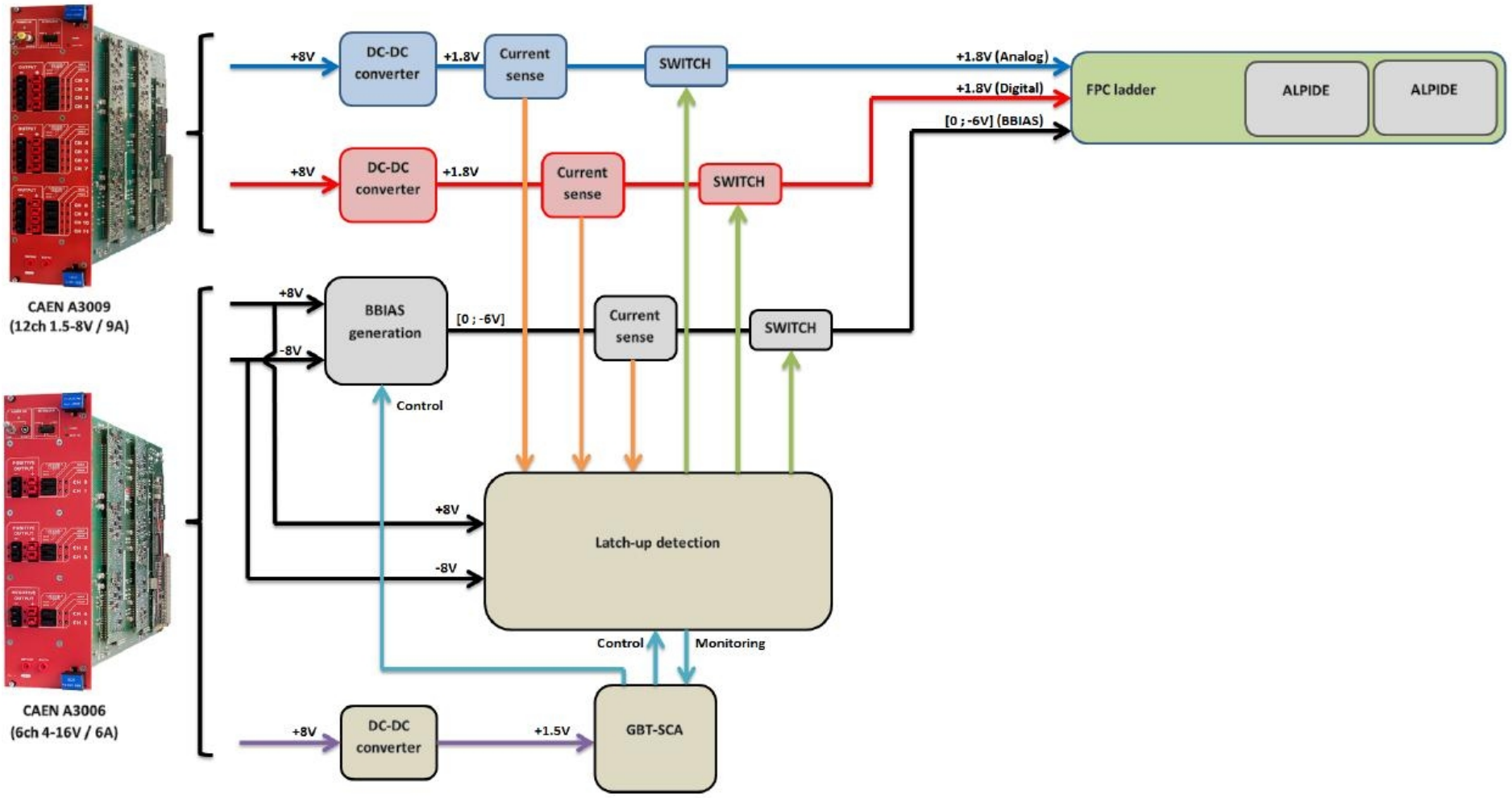
Old



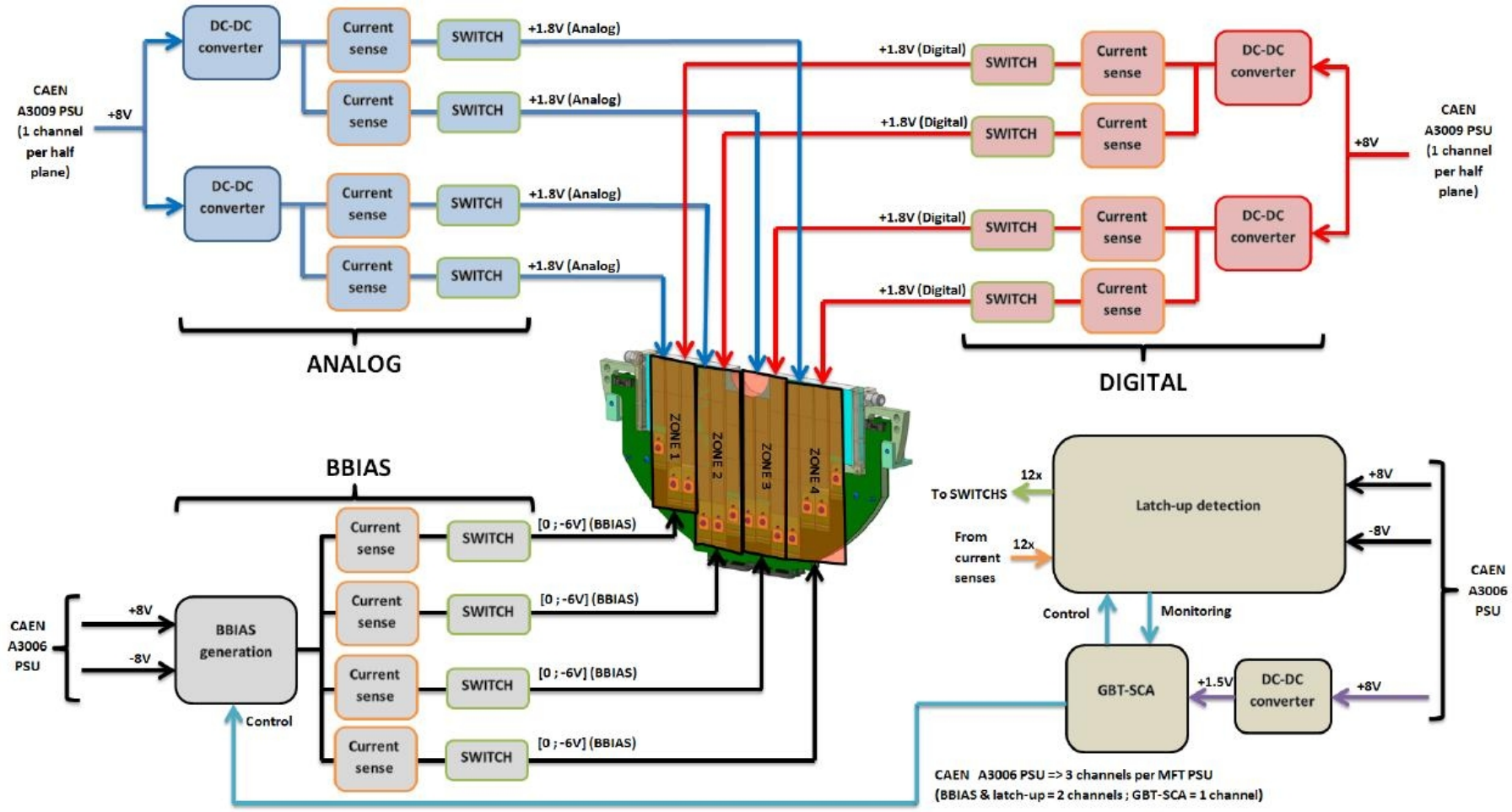
New



PSU to ladder block diagram



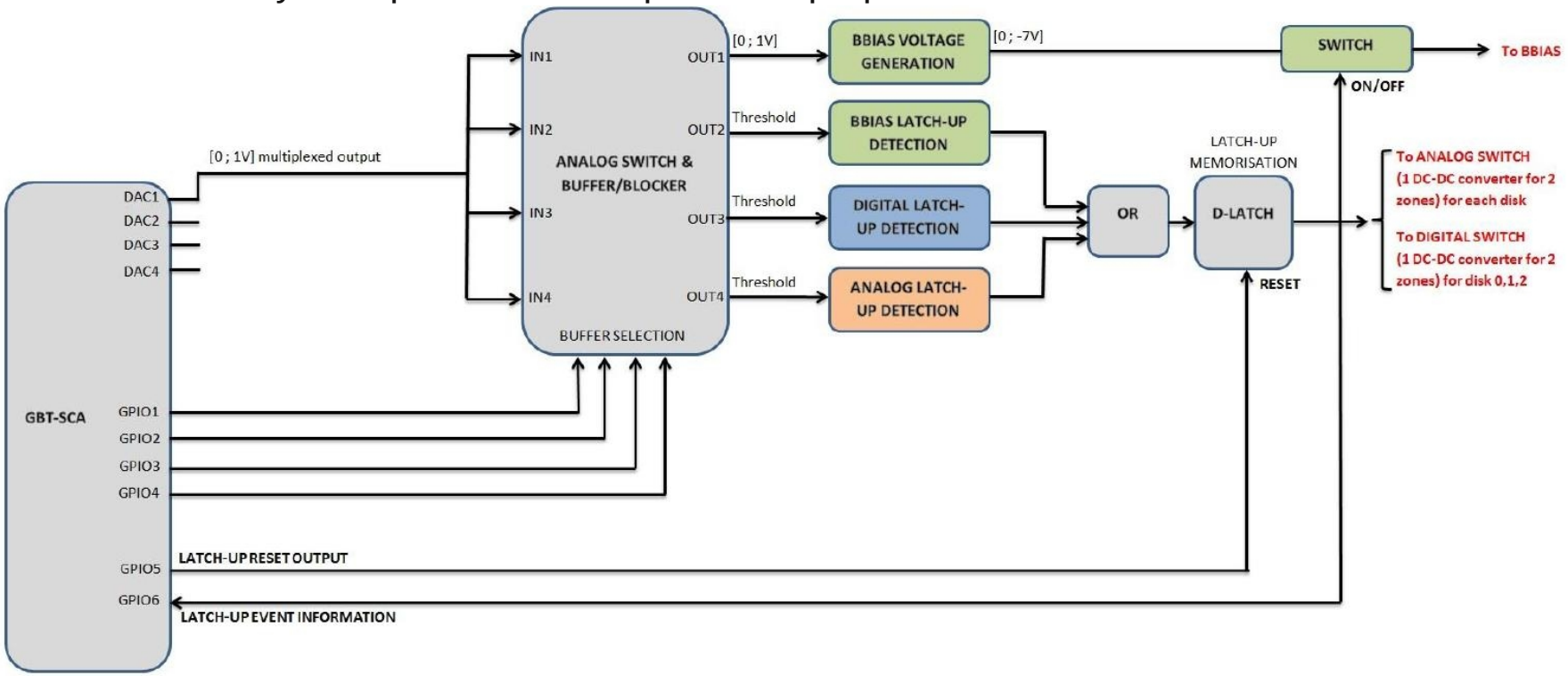
PSU to disk block diagram



1 DC/DC converter per zone for digital voltage in disk 3 and 4

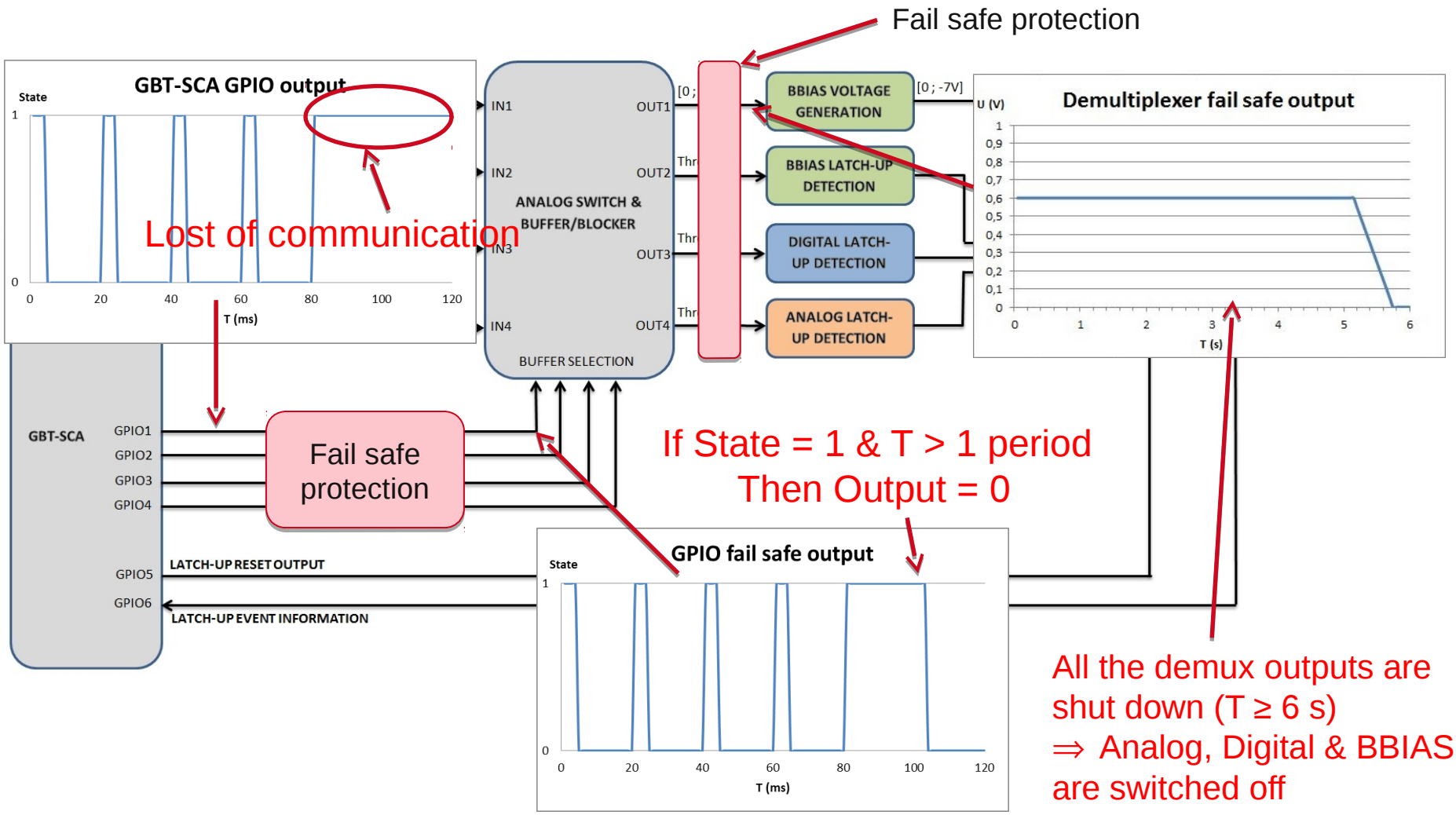
Power Supply Unit: demultiplexer solution

- 1 GBT-SCA per disk: 4 zones x 4 voltage levels = 16 voltage levels.
- GBT-SCA only 4 outputs → demultiplexer as proposed solution.

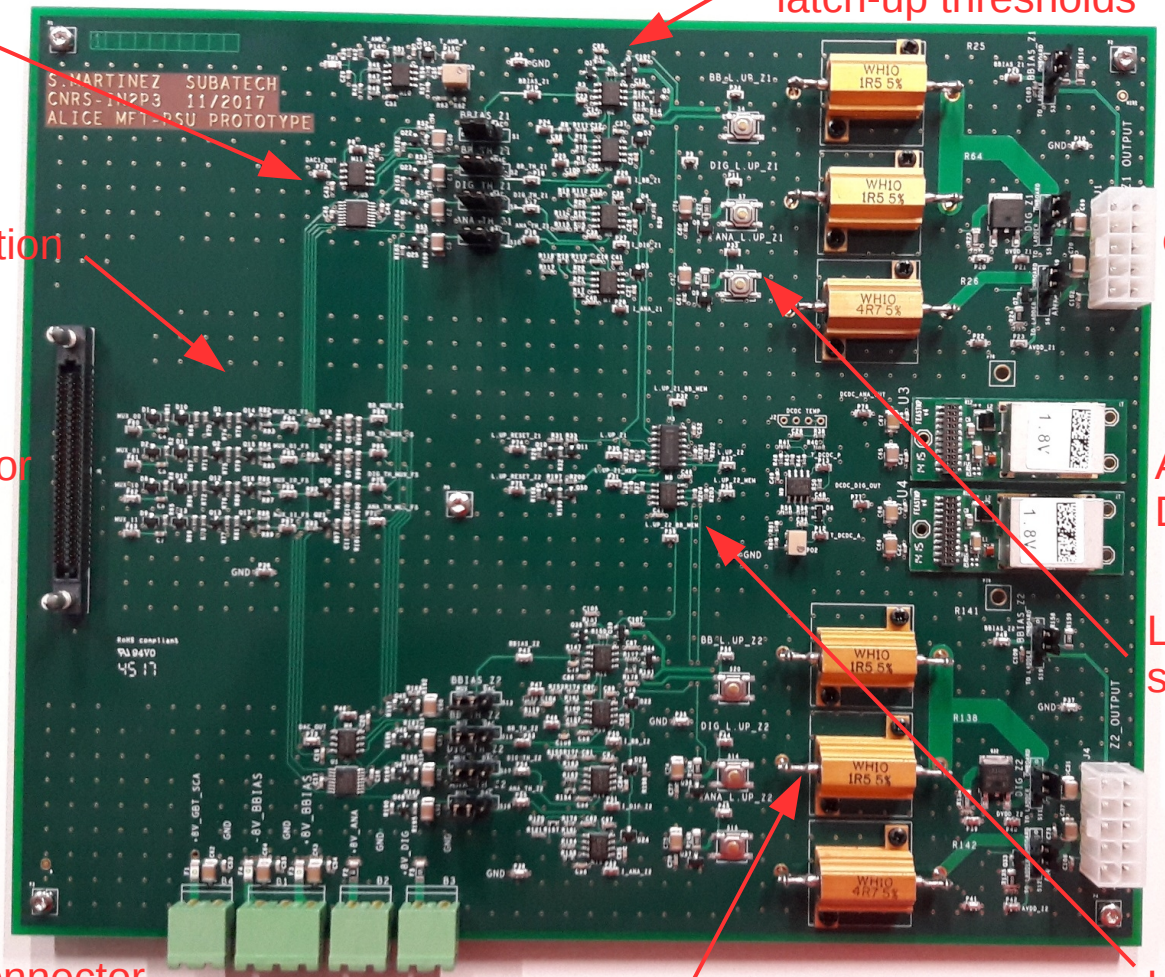


- **Automatic passive fail safe protection is add on the GPIO output of the GBT-SCA and the demultiplexer output. If more than one period of multiplexing doesn't occurs, all voltage outputs are shuted down.**

Power Supply Unit: fail safe principle



Power Supply Unit: first prototype



BB generation + BB, DVDD and AVDD latch-up thresholds

Demultiplexer

Fail safe protection

Connector to microcontroller or GBT-SCA

Power IN connector

Power OUT connector

Analog and digital DCDC converters

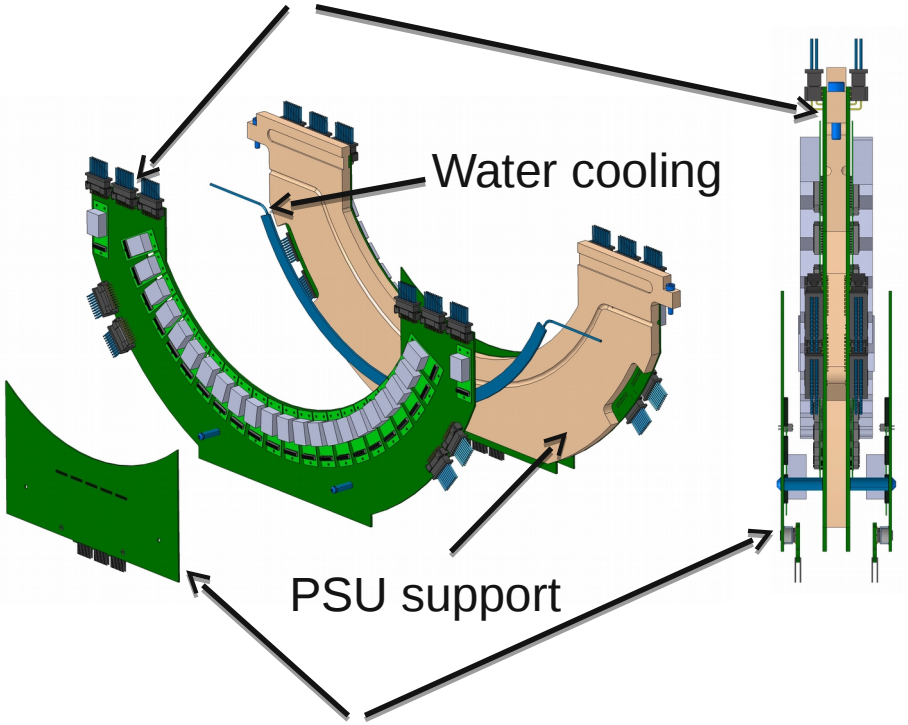
Latch-up simulation switches

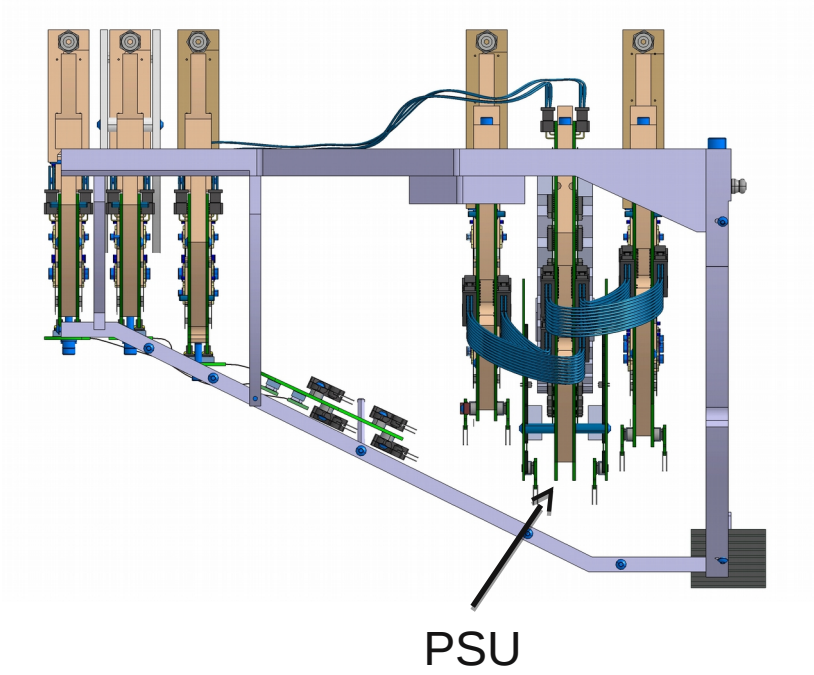
On-board resistors

Latch-up memorization

PSU actual layout design

PSU main board (24 DC-DC converters, L-up detection, BBIAS…)



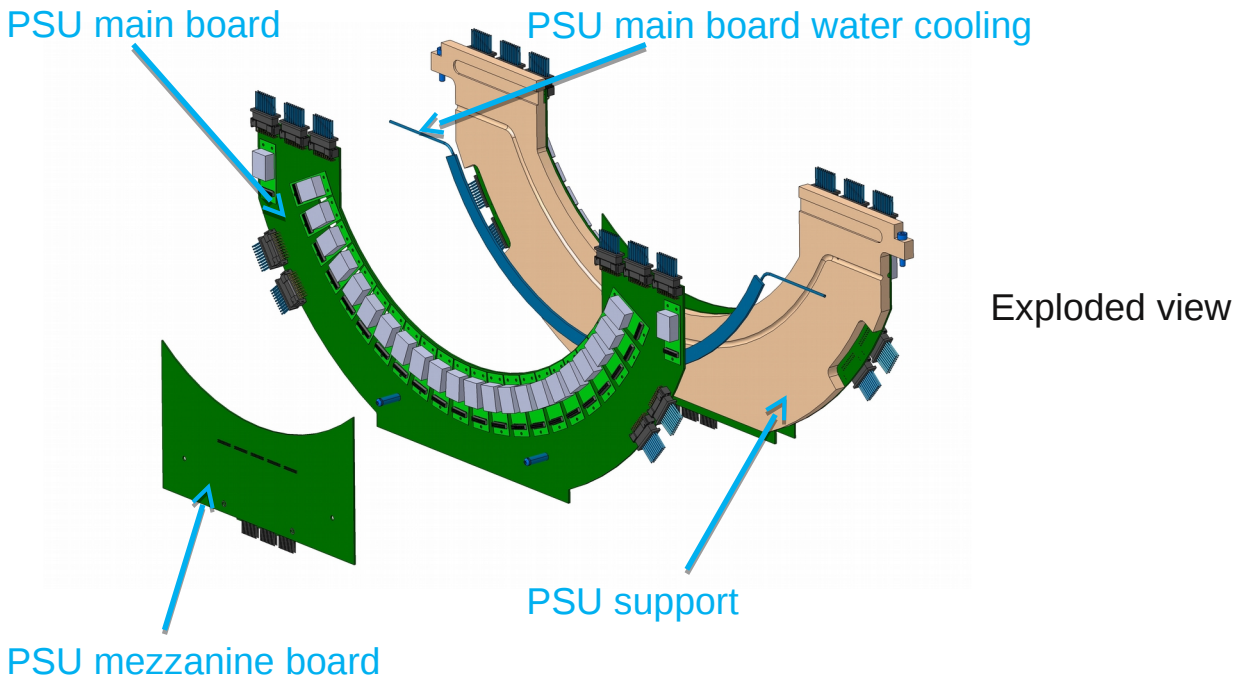


PSU mezzanine board (5 GBT-SCA, 5 DC-DC converters…)

We verified that all the components can fit onto the PSU main and mezzanine board.

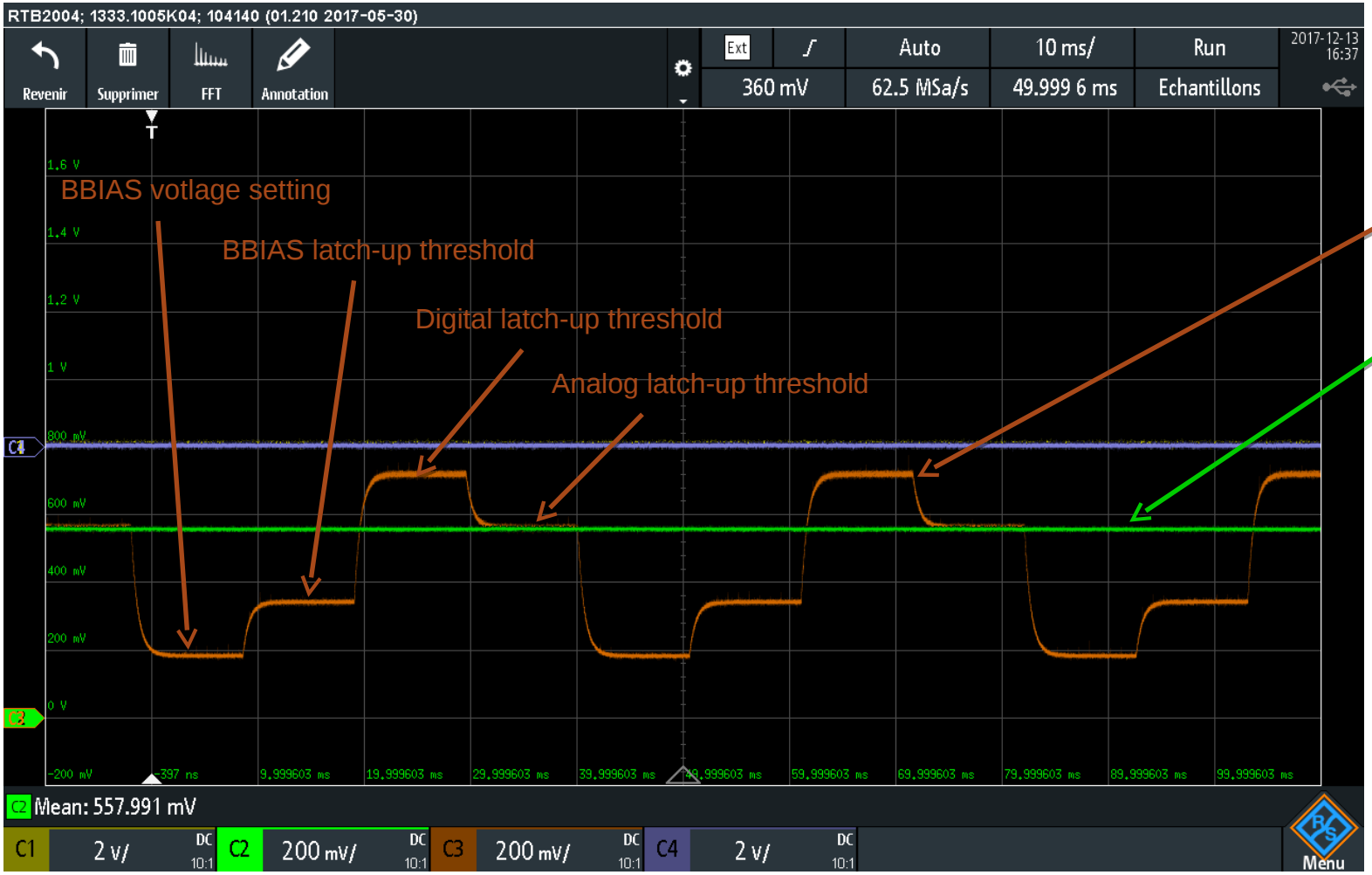
PSU layout

- The main board dissipates 16W of power and needs a water cooling for the DCDC converters
- The mezzanine board dissipates 700mW and do not need a water cooling

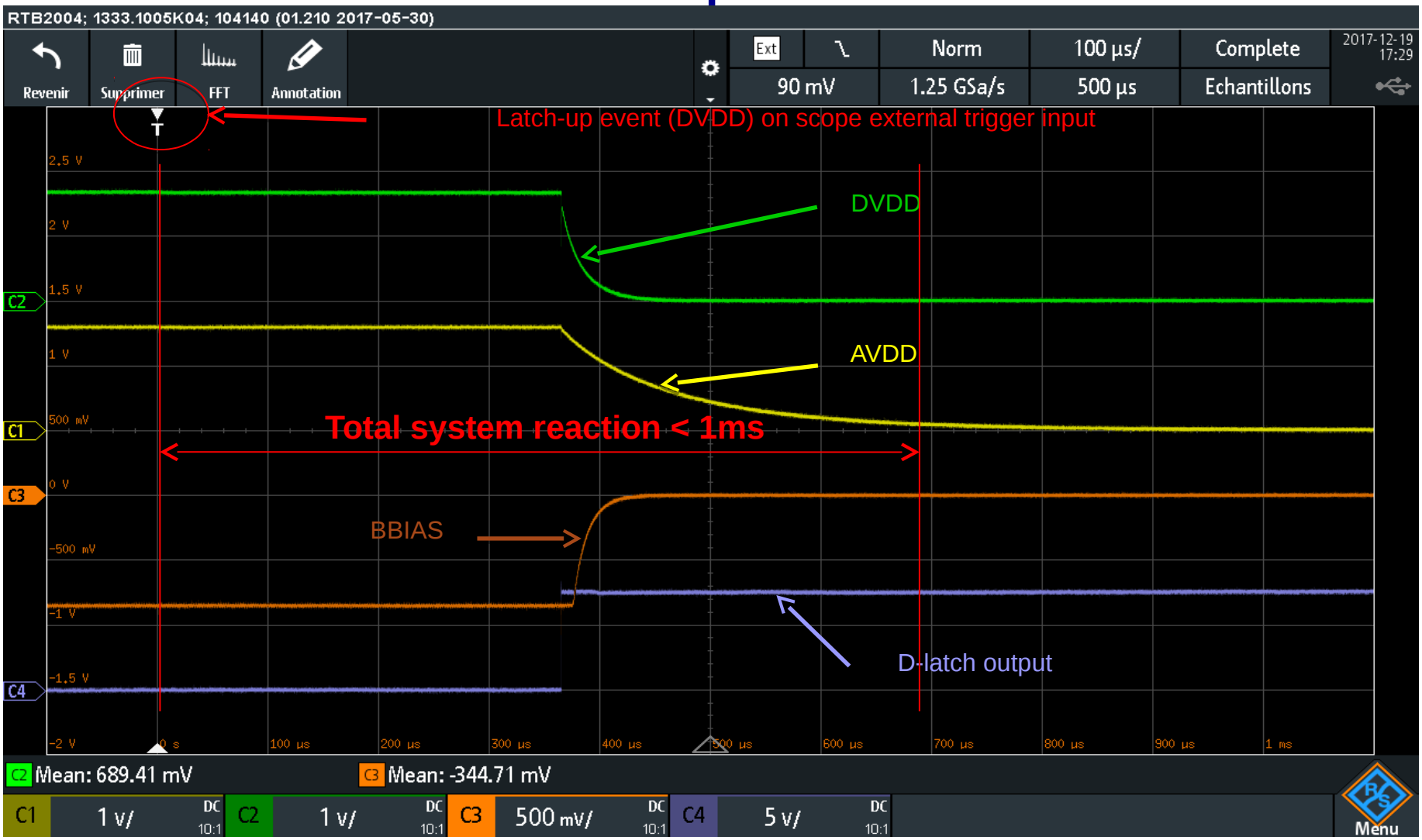


Exploded view

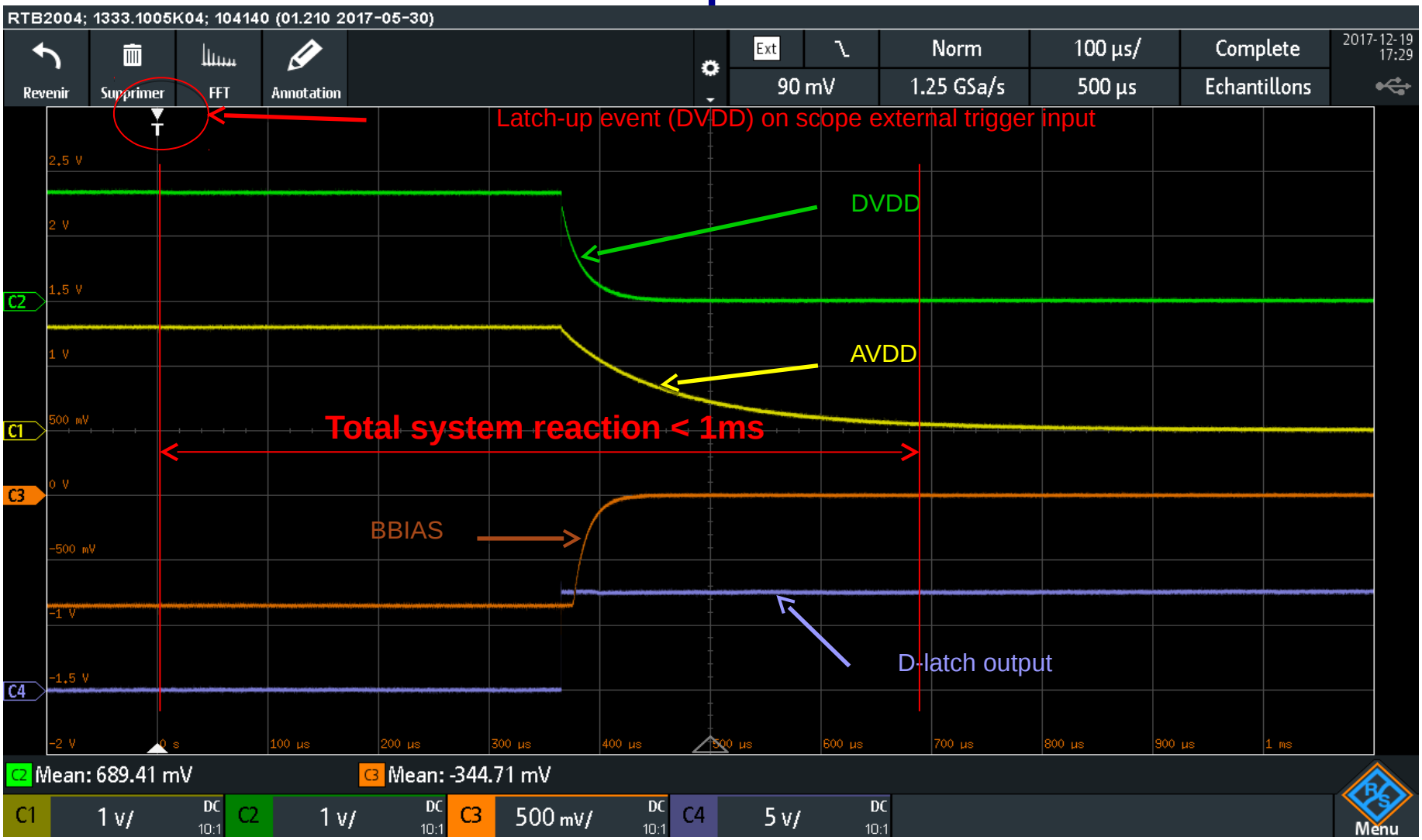
MUX and DEMUX signal output



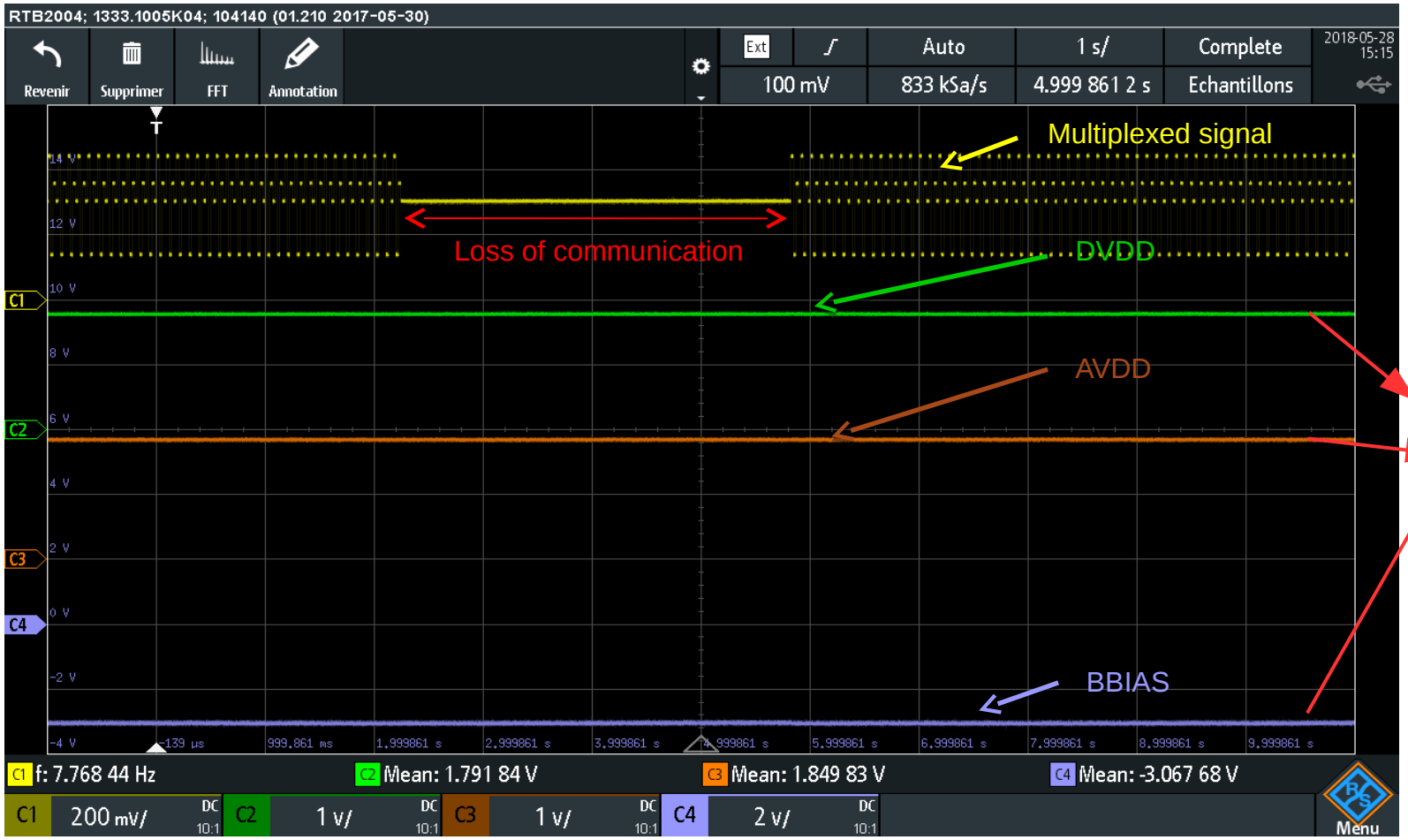
PSU reaction after a latch-up



PSU reaction after a latch-up

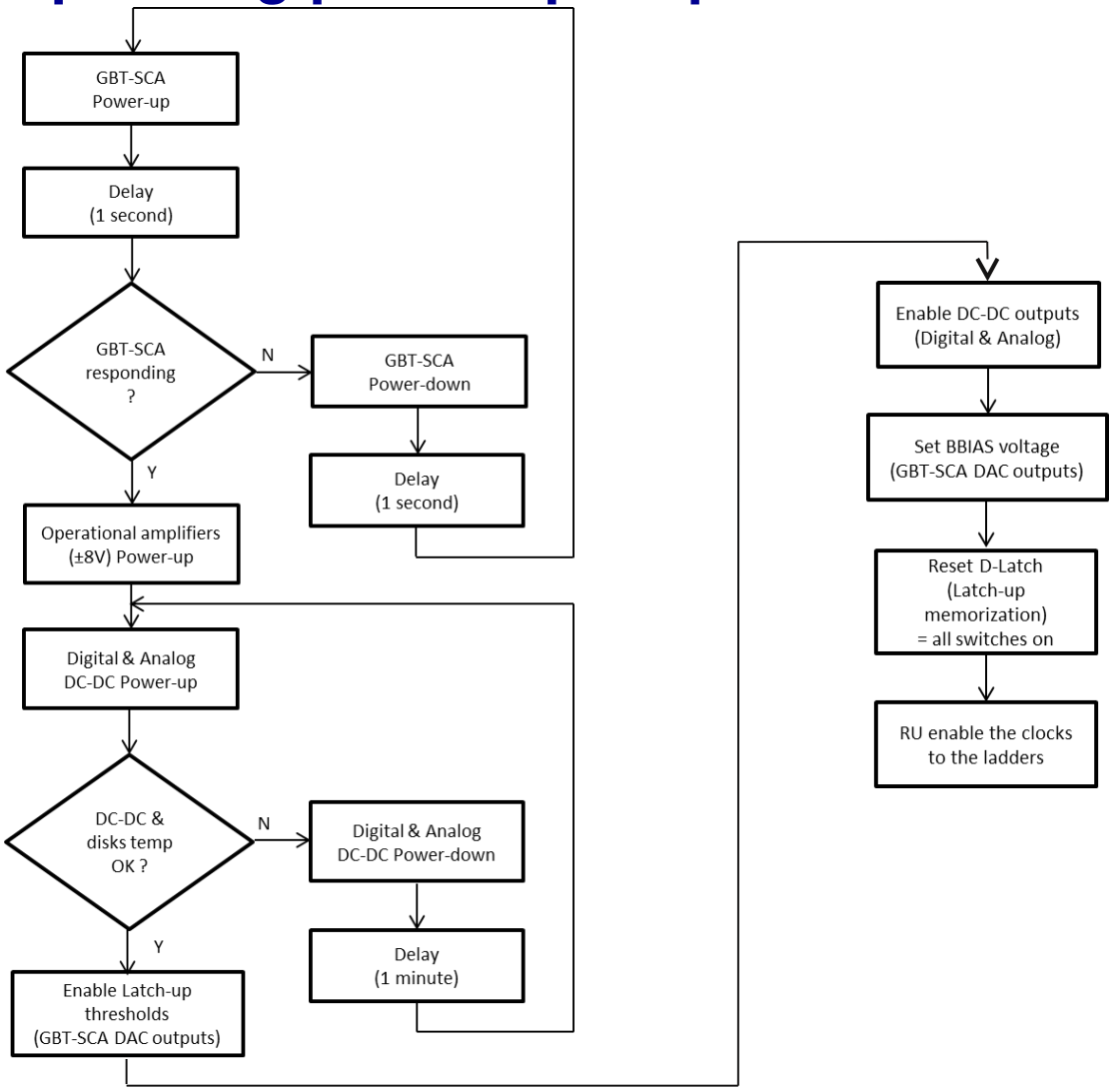


PSU reaction after a short loss of communication

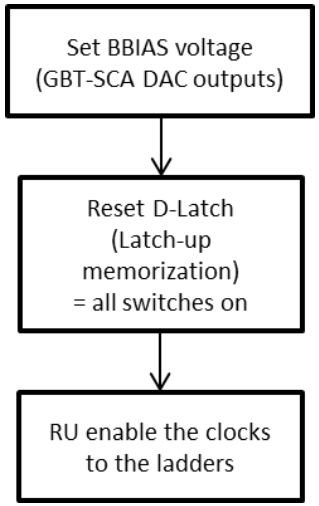


- Endurance test carried out over six days. No anomaly, no communication loss.

PSU operating power up sequences

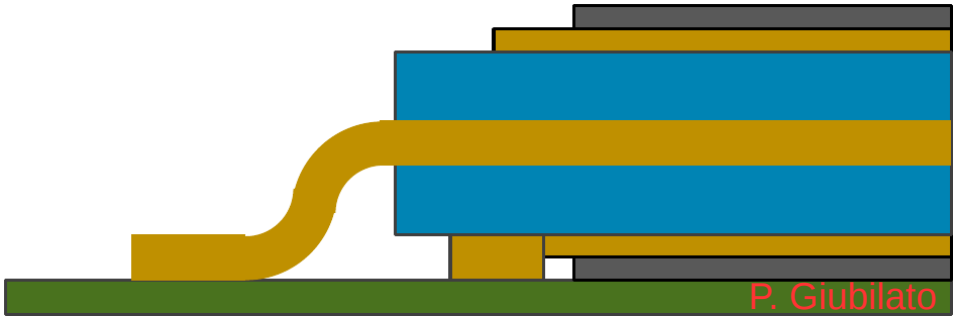


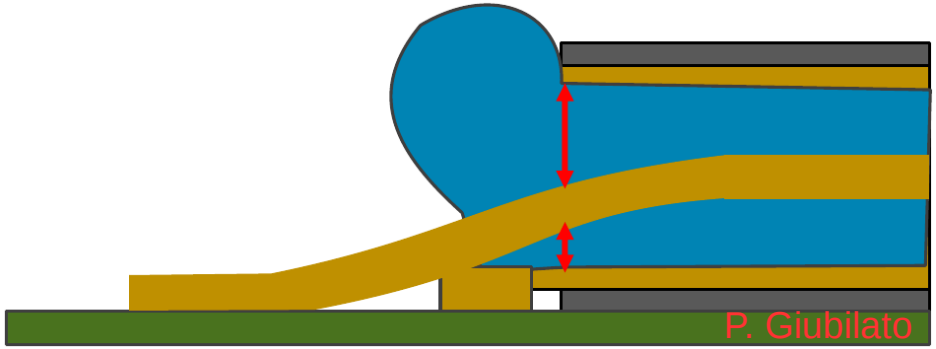
PSU operating power up sequences (after latch-up)



Readout cable issues

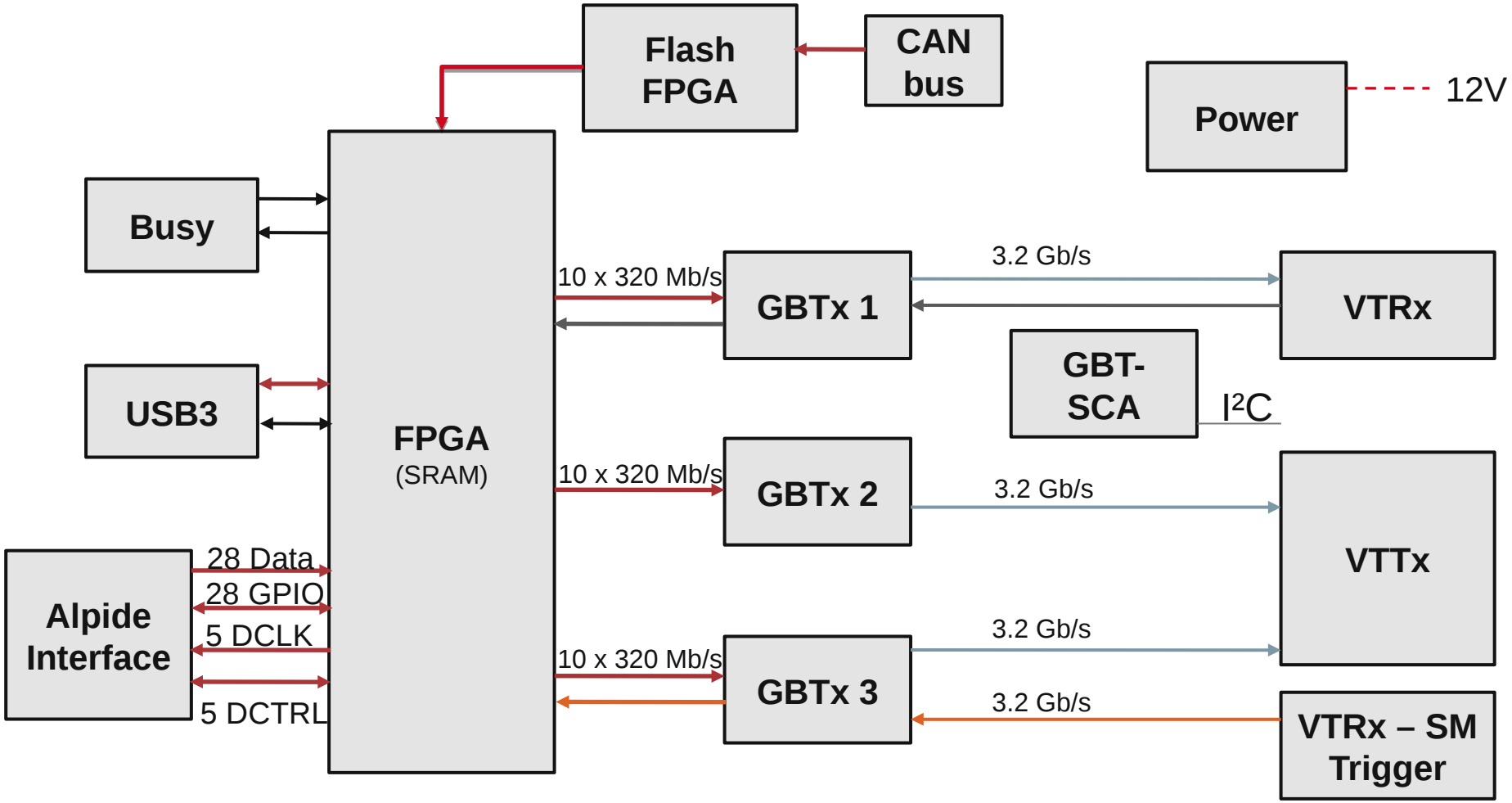
- Melting of the custom made dielectric while soldering the cable to the PCB, as it has lower melting point respect the standard one:
  1) may short the central conductor with the shielding,
  2) even if no short happens, the change in geometry affects the z_0 of the cable.



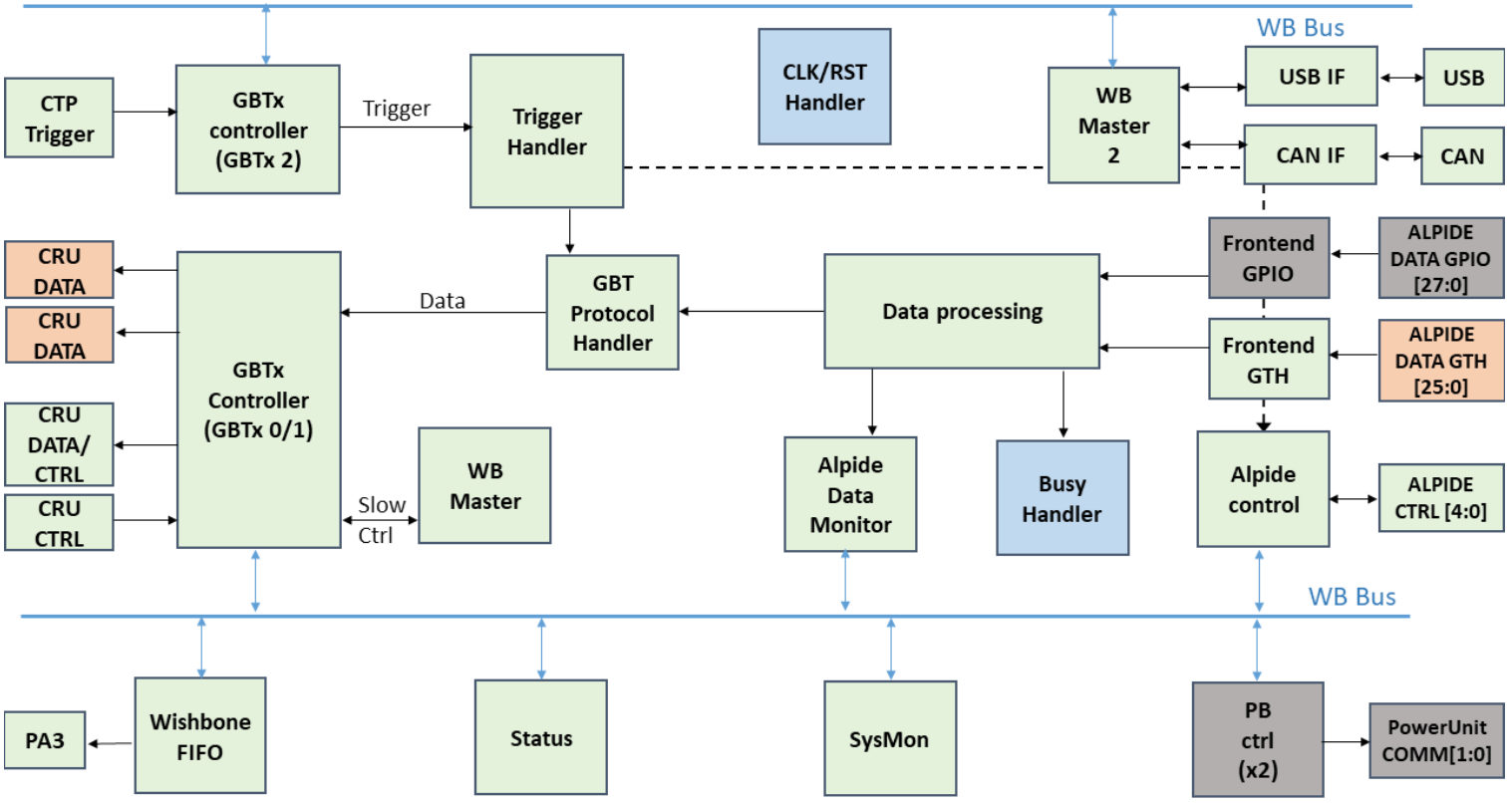


- Solutions tried (and working): use of Bismuth soldering, pre-forming the cable end, use of newly-developed low-pressure tool to partially relief the mechanical strain.
- SAMTEC has to implement all those solutions in an automatic production process → delivery delayed. First sample foreseen for end of November.

Readout Unit overview



Readout Unit Firmware blocks



Common to ITS & MFT

Specific to MFT

Not fully implemented

Specific to ITS