

# MFT DCS Status

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for MFT DCS team  
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Hiroshima Univ.

20<sup>th</sup> November, 2018

12<sup>th</sup> ALICE ITS Upgrade, MFT and O2 Asian Workshop

# Outline

- MFT DCS team in Japan
- **Development Progress of DCS**
  - hardware architecture
  - final tuning of DCS and FSM
  - FSM panels
  - Logical view
- **Test bench at Hiroshima**
- **Summary**

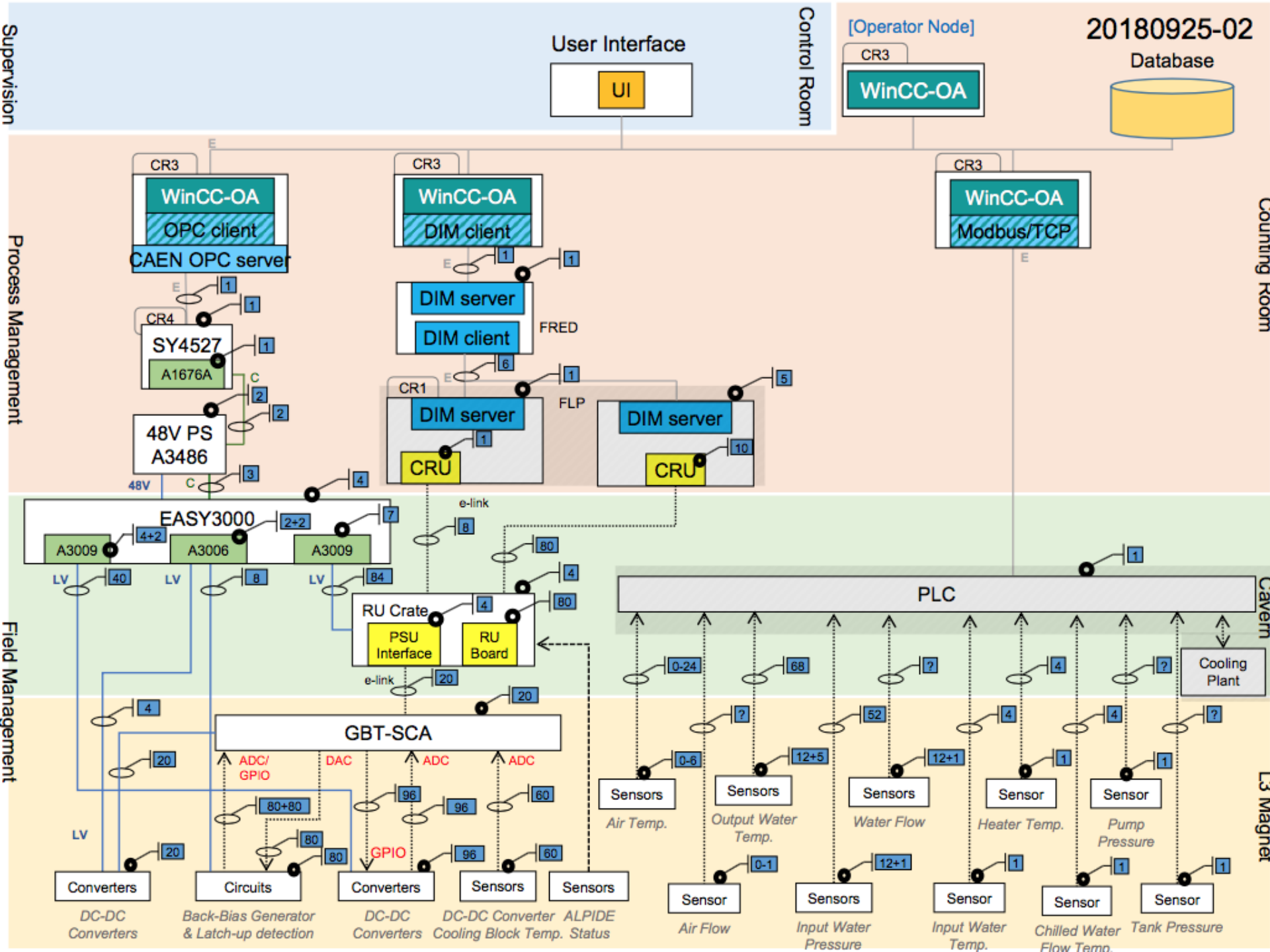
# MFT DCS team in Japan

- Kenta SHIGAKI (convener)
- Ken OYAMA (advisory)
- Kosei YAMAKAWA (PhD student)
- Motomi OYA (master's course from 2019)

Dr.YAMAGUCHI (new post doctor at Hiroshima Univ.)  
will join MFT team from December

- Performance check for Physics
  - Yuji KAWAMOTO
  - Takumi OSAKO
  - Kazuki YOSHIKAWA
  - Kaede KAMANO
  - Takehito KONDO



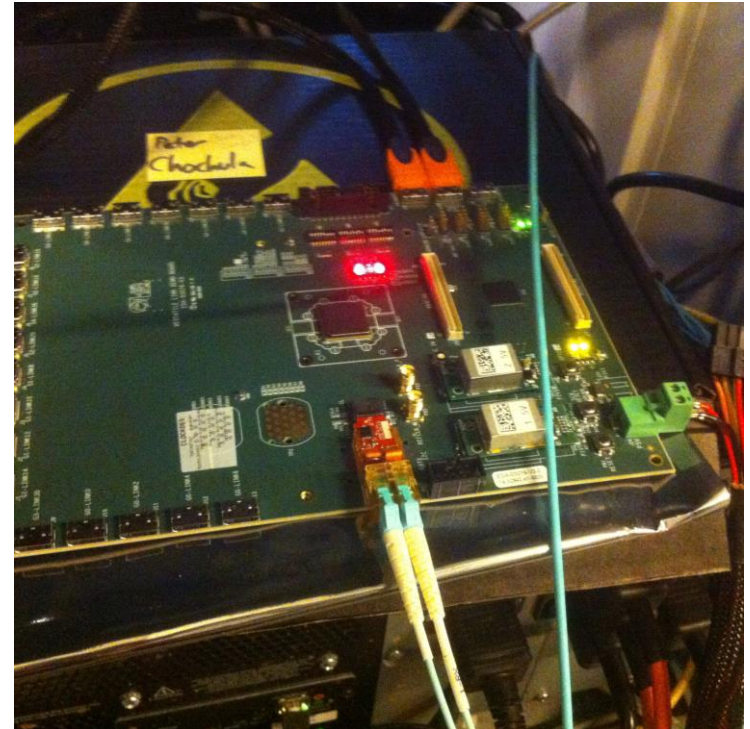


# Hardware Architecture

- Test Bench of CAEN System at CERN
- GBT-SCA Command Sequence



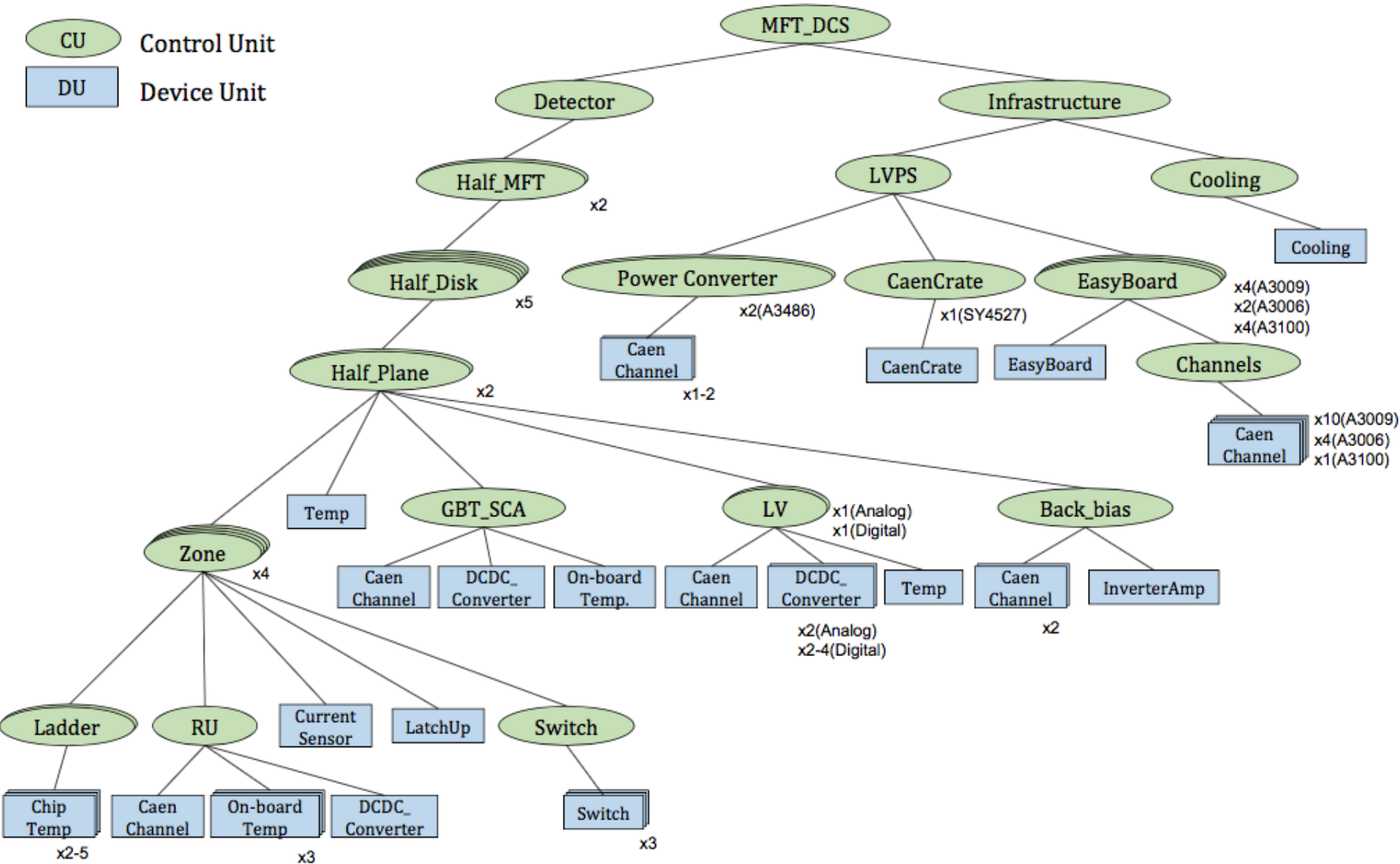
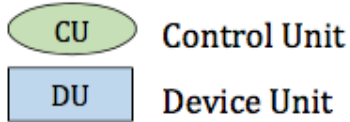
Test bench of CAEN system



VLDB (The Versatile Link Demonstrator Board)

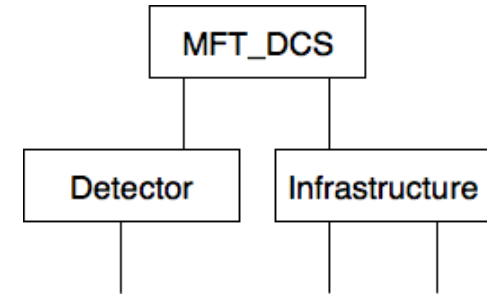
# Finite State Machine

Ver. 20180204\_1



# Finite State Machine

- Implementation of FSM tree is completed
- Testing and making a small modification



States and Actions (mft\_dcs\_cern - mft\_dcs\_cern; #1)

Object Type: MFT\_DCS\_OT Panel: MFT\_DCS\_OT.pnl

Simple Config Object Parameters Copy from Type:

State List

Init: NOT\_READY, SUPERSAFE, RESTORING\_SAFE, MOVING\_SUPERSAFE, SAFE, MOVING\_READY, MOVING\_SAFE, READY, ERROR

Action List

GO\_READY, GO\_SUPERSAFE, GO\_SAFE

State: NOT\_READY Color: [Blue] Action: GO\_READY

When List

```

when ( $ANY$fWCHILDREN in_state (ERROR) ) move_to ERROR
when ( $ALL$mFT_INFRA_OT in_state NOT_READY ) move_to SUPERSAFE
when ( $ALL$fWCHILDREN in_state READY ) move_to READY
  
```

Add Remove Rename Make a copy Add Remove Action Parameters

Type Overview Type Diff... Apply OK Cancel

SUPERSAFE

GO\_SUPERSAFE

SAFE

GO\_SAFE

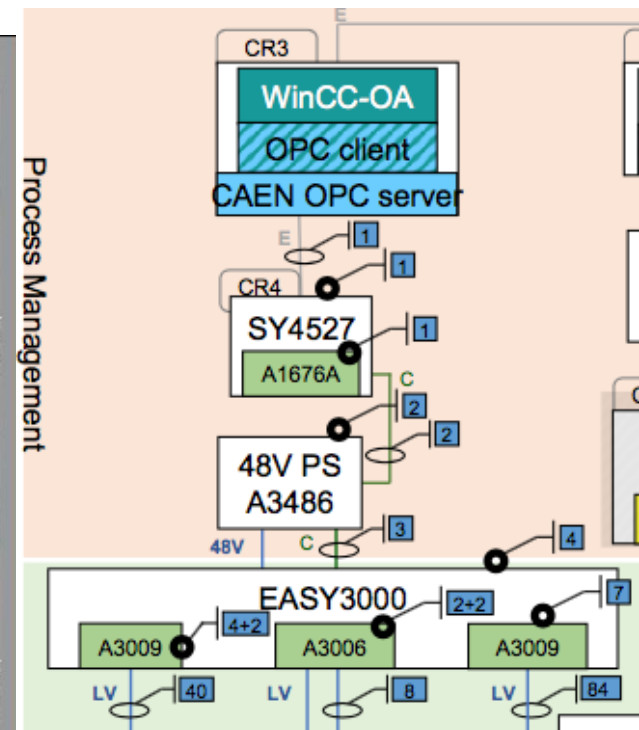
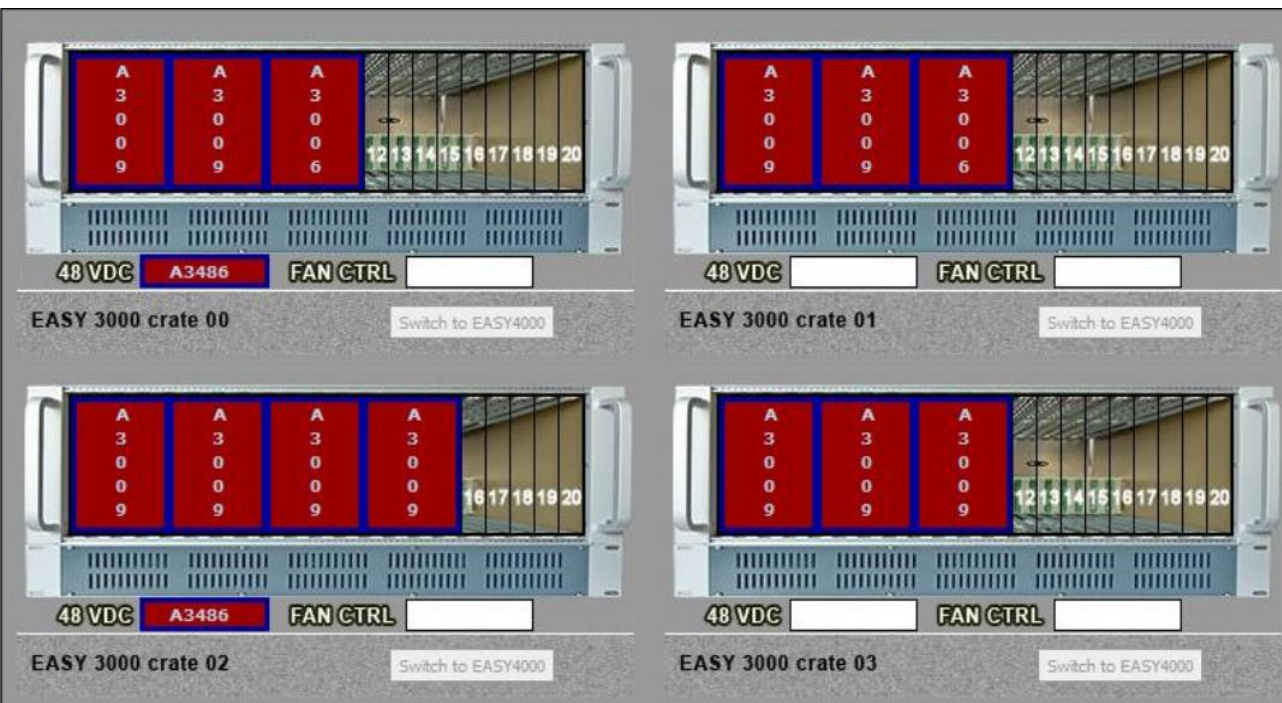
READY

GO\_READY



# Final tuning

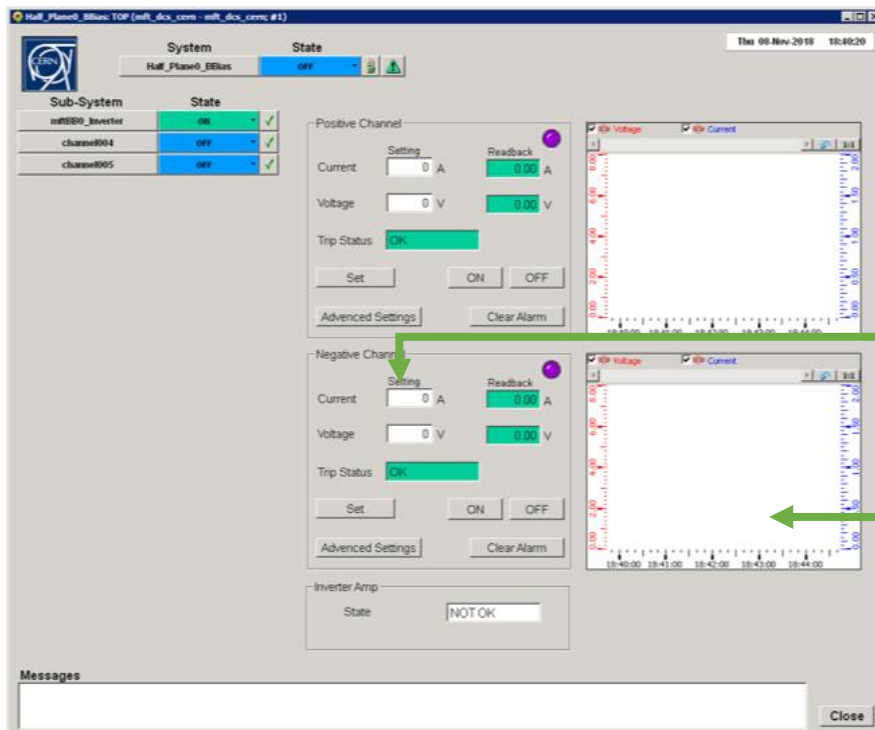
- A3009× 4 →DCDC Converter→Zone
- A3009× 7 →DCDC Converter→RU Board
- A3006→Back-Bias Generator→ALPIDEs
- A3006→DCDC Converter→GBT-SCA





# FSM Panels

- Implementation of FSM Panels
- For both MFT experts and ALICE shifters
- Panels show each states clearly



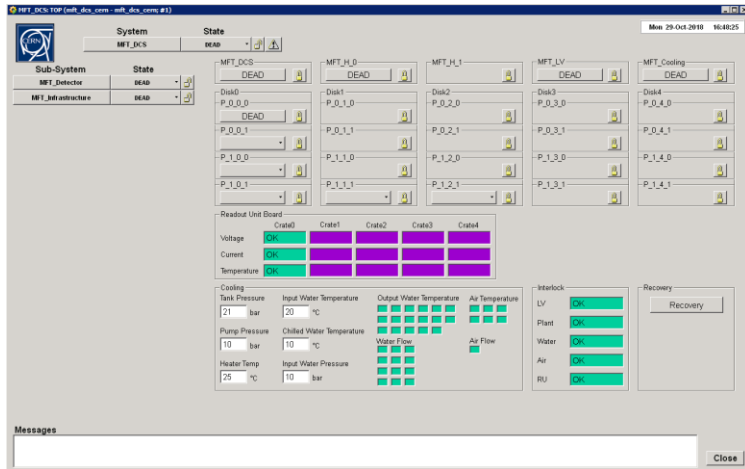
Half\_Plane\_0\_Bbias

Display voltage and current

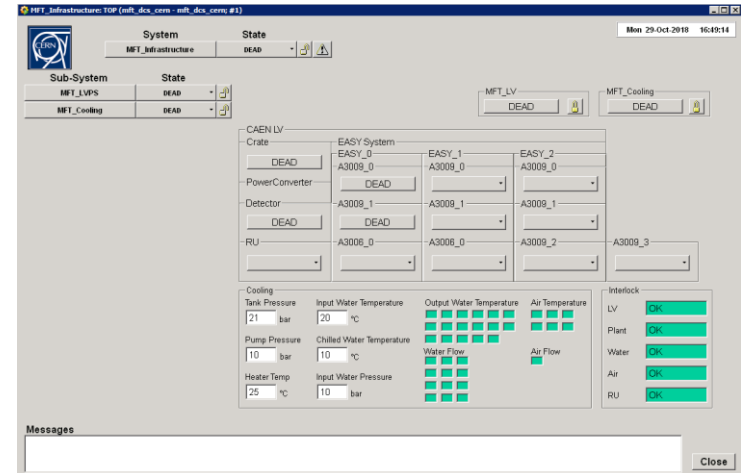
Trending

# FSM Panels

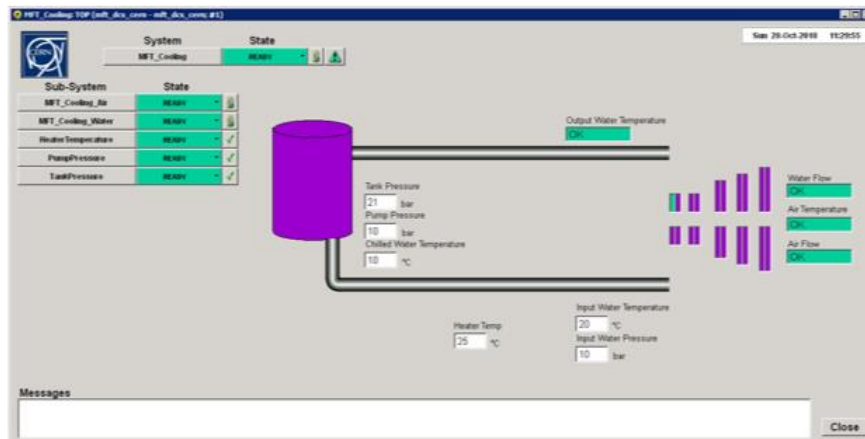
## MFT\_DCS



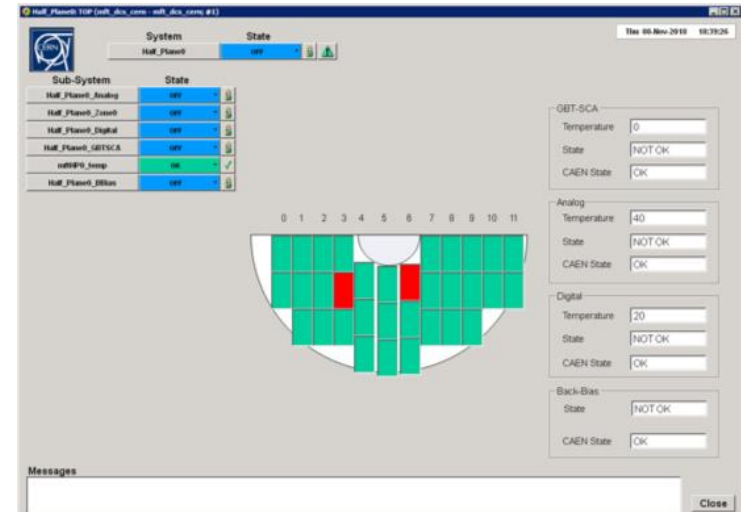
## MFT\_Infrastructure



## MFT\_Cooling



## Half\_Plane



# FSM panels

## CAEN Channels

The screenshot shows the 'Channels TOP' control panel. At the top, the 'Object' is 'Channels' and the 'State' is 'OK'. A table on the left lists 12 channels (channel000 to channel011), all with a state of 'OFF'. The main area contains 12 individual channel control panels, each with 'Setting' and 'Readback' fields for both Current (A) and Voltage (V). Each panel includes 'Set', 'ON', 'OFF', 'Advanced Settings', and 'Clear Alarm' buttons. A 'Messages' box is at the bottom left.

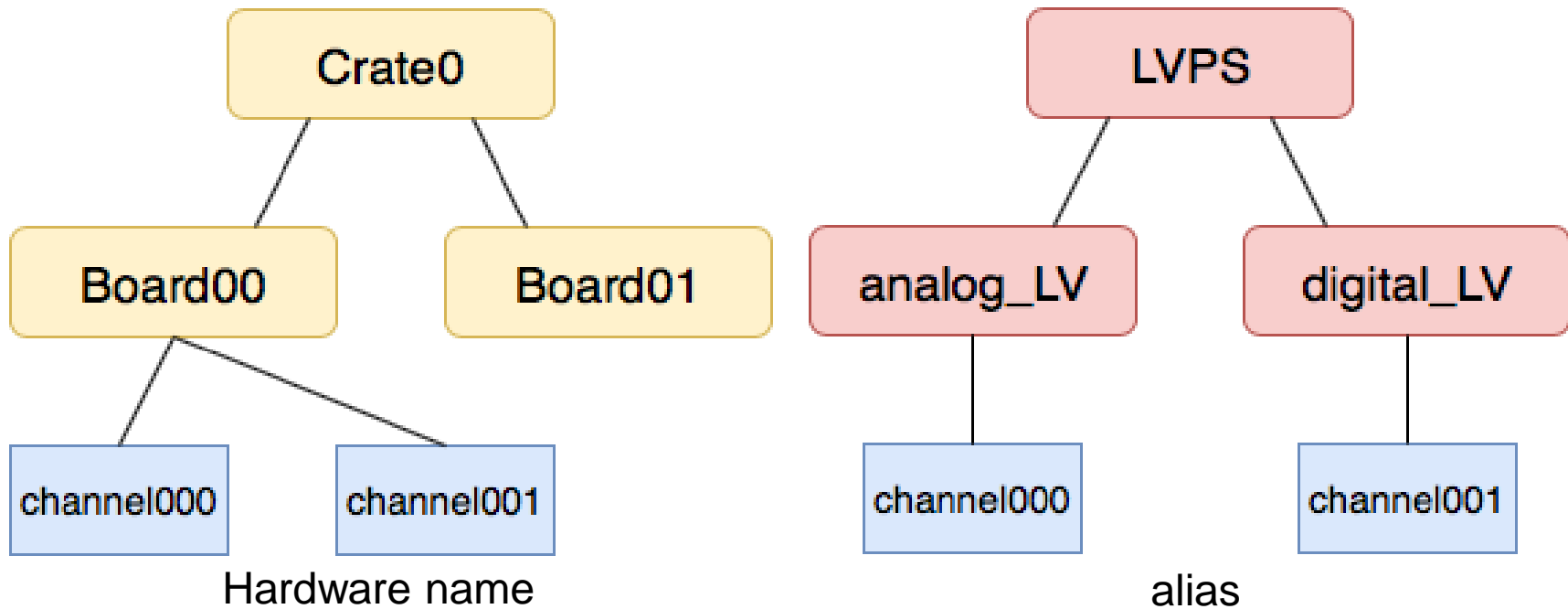
## Single channel

The screenshot shows the 'Half\_plane\_0\_digital\_LV/channel000: TOP' control panel. The 'Device' is 'channel000' and the 'State' is 'DEAD'. The 'Parameters' section shows 'Current' set to 2 A with a readback of 97764826 A, and 'Voltage' set to 1 V with a readback of 98855591 V. The 'Trip Status' is 'OK'. A graph on the right shows a step function for voltage and current over time. The 'Messages' box is at the bottom.

Time (s)	Voltage (V)	Current (A)
14:16:00	0.00	0.00
14:16:05	3.00	0.00
14:16:10	3.00	2.00
14:16:15	3.00	2.00
14:16:20	6.00	2.00
14:16:25	6.00	2.00
14:16:30	6.00	0.00
14:16:35	6.00	0.00
14:16:40	0.00	0.00

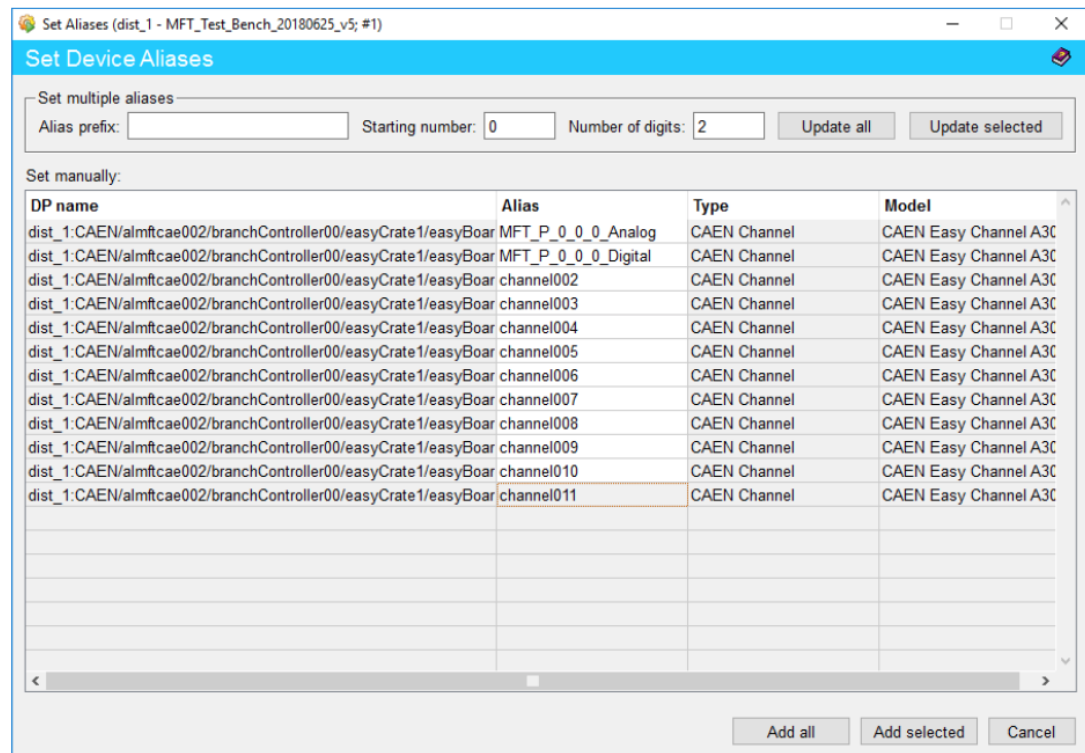
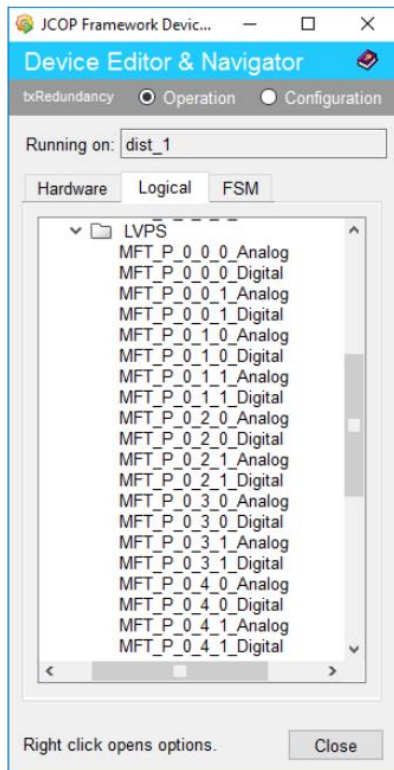
# Logical View

- Creation alias
- Alias clarify what things are used for
- FSM and script can use alias



# Logical View

- Use alias to implement FSM and hardware.
- Whether to link with the database is under discussion



# Full Scale Test Bench

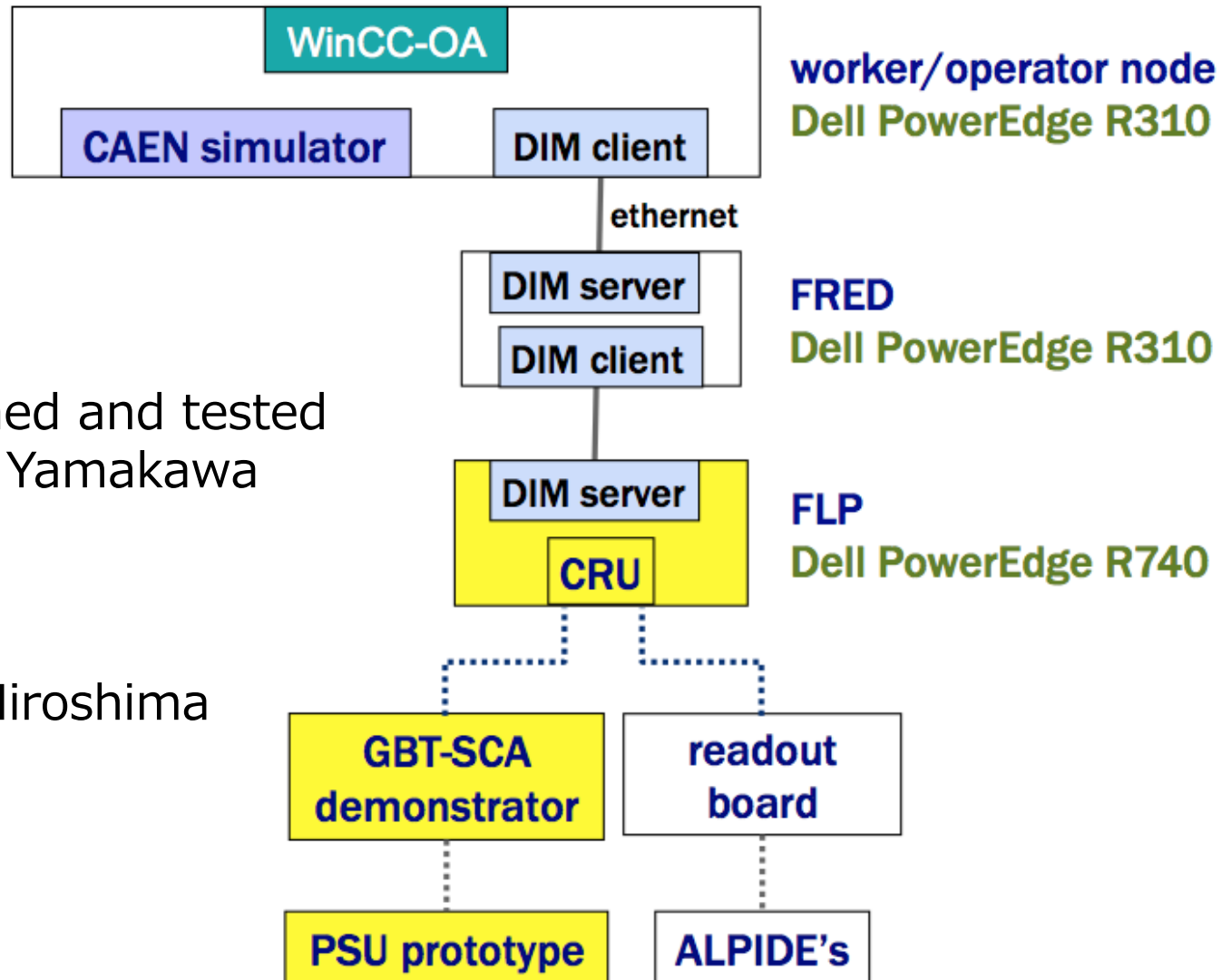
- Setup a test bench at Hiroshima
- Component
  - WinCCOA PC for operator/worker node
    - ↳Dell PowerEdge R310
  - FRED
    - ↳ Dell PowerEdge R310
  - CAEN simulator

- FLP(already delivered at CERN)
  - ↳ Dell PowerEdge R740
- CRU(installation will be done)
- GBT-SCA demo board (VLDB)
- PSU prototype

Purchase or loan  
from CERN/ALICE/MFT



# Full Scale Test Bench



To be commissioned and tested  
at CERN by Kosei Yamakawa



To be started at Hiroshima  
from December

# Future Work

- Testing and tuning DCS and FSM
- Detector design
  - on-detector sensors
  - on-detector GBT-SCA I/O port map
- Interlock scenarios
- Full scale test bench

# Summary

- Dr.YAMAGUCHI will join in December 2018
- Development of DCS is in progress
  - create FSM panels
  - alias CAEN channels
  - final tuning
- A few remaining things to do
- Test bench at Hiroshima will start in December