Update on the detector read-out and slow control

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CRU - CERN

OUTLINE

1. test on-going with detectors
2. measurements with TPC full FPGA, FW, LHCb full FPGA, ALICE full FPGA firmware

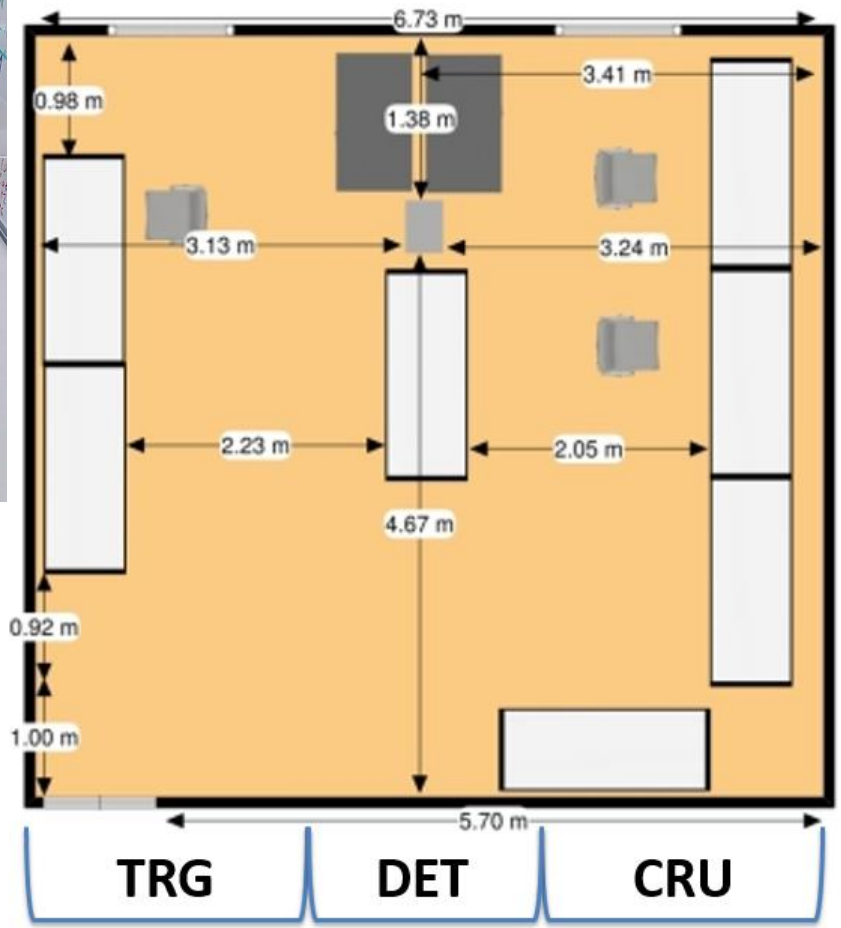
CRU TEST SUMMARY

DET	FLP	CRU	GBT	FEE	READOUT	DCS through CRU (custom script)
TPC @ CERN	5	4 (2 in one FLP)	36	18	CONTINUOUS(1)	SCA
ITS @ CERN	2	4 (4 in one FLP)	5	5	PACKET(1)	SCA – SWT
ITS @ USA (Univ. of Texas)	1	1	1	1	PACKET(1)	SCA – SWT
MID @ SUBATECH	1	1	1	1	CONTINUOUS(2)	SCA
MFT @ IPNL	1	1	1	1	PACKET(2)	SCA – SWT
TOF @ INFN Bologna	1	1	2	2	PACKET(2)	Not used
MCH @ CERN	1	1	1	1	CONTINUOUS(1)	SCA
TRD @ GERMANY (MUENSTER UNIV)	1	1	TRD custom link (under dev)	1	CONTINUOUS(2)	Not used
TRG @ CERN	Communication between LTU and 8 CRUs -> tested. Trigger delivery to CRU and forwarding to FEE -> tested					
DCS @ CERN	DCS Slow Control chain (ALF-FRED) -> tested. Installation in detector set-up -> on going					

CRU FW	**>= 2.5.0**
O2 Readout(1)	**>= 14.0.1**
O2 ReadoutCard(2)	**>= 8.12.1**

SCA: slow control protocol used by SCA chip on the FEE
SWT: custom slow control protocol implemented over GBT data payload

CRU – TRG test lab @ CERN (4 / S-059)



Tests ongoing with ITS

- 5 RUs (5 GBT links) connected to 1 CRU:
  - SCA, SWT configuration and monitoring -> OK.
  - DMA :
    - readout in packet mode,
    - triggers generated from CRU (ctp-emulator),
    - readout.exe used, official O^2 readout software.

- **Work in progress:**
  - Final CRU – RU link configuration
    - 1 link for trigger and 1 link for SWT. Currently is one link used for both.
    - LTU integration.
  - Detector configuration using DCS framework (ALF-FRED). DCS chain installed in bld.167, waiting for feedback.
  - Evaluation of SWT protocol requirements:
    - Time needed to configure 1 RU
    - Request for broadcast (still under evaluation) … see next slide

Tests ongoing with ITS (under evaluation)

CRU – ITS SWT on multiple channels

SWT as present

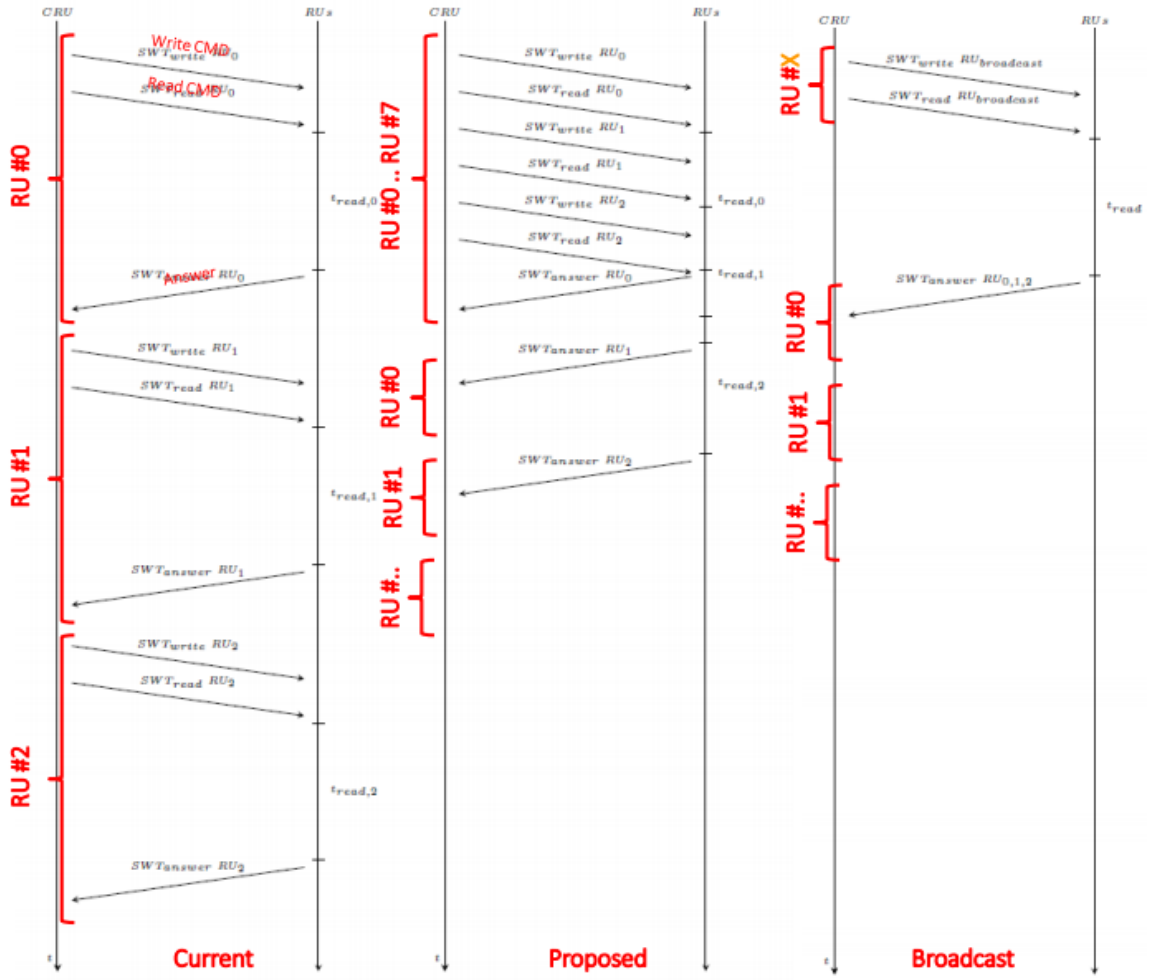
- Each Common Readout Unit (CRU) is connected to 8 Readout Units (RUs). Current CRU implementation has a multiplexer connecting to a single RU. **If a RU answers on a different channel than the one selected, the data are lost**.
- The answers for the SWT on a single RU can take "long time" for some operations, prompting for a "push" mechanism.

Uplink FIFOs on CRU

- What ITS proposes is a per-channel FIFO to store the results of the SWTs. This would greatly reduce the time to query information from multiple RUs.
- Each channel FIFO should have a depth of 1024 words.

CRU SWT broadcast

- If a per-channel FIFO is possible, it might be beneficial to broadcast the SWTs to different RUs.
- This would also greatly reduce the time required to execute periodic reads of the same values in different boards.
- This might also be done with a mask: instead of broadcasting to all the boards only a subset could be set with a 1-hot mask.



(a) Current implementation. (b) 1 FIFO per channel.

https://indico.cern.ch/event/771625/contributions/3206178/attachments/1752568/2840239/20181114_WP10_ITS_SUF_v1.pdf

Tests ongoing with MFT

- 1 RUs (1 GBT link) connected to 1 CRU:
  - SCA, SWT configuration and monitoring -> OK.
  - DMA (to be tested, same ITS firmware):
    - readout in packet mode,
    - triggers generated from CRU,
    - readout.exe used, official O^2 readout software.

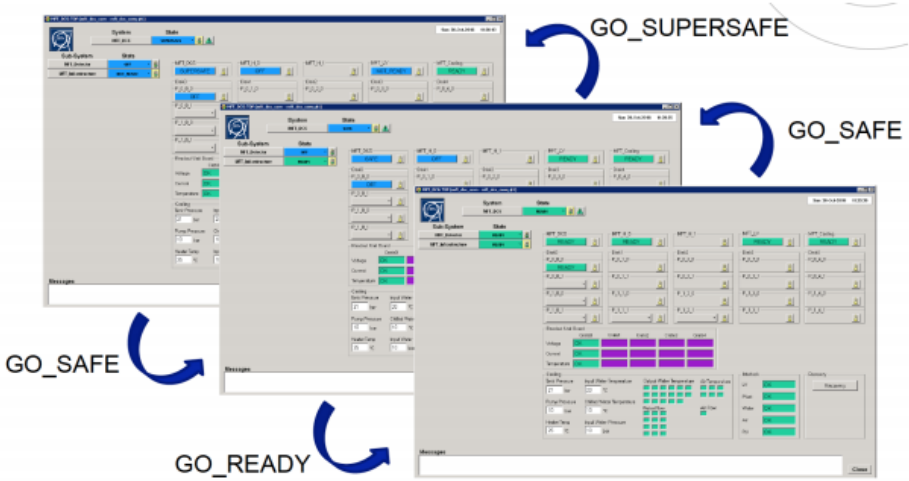
- Some issues reported in the past, to be checked if they are still valid.

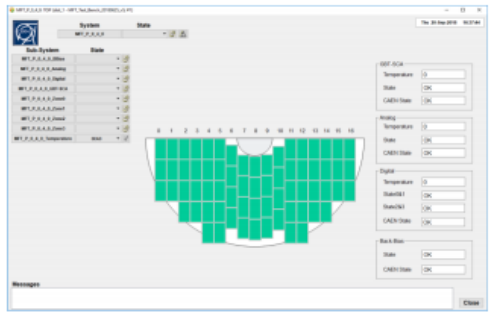
Tests ongoing with MFT

- Additional SCA feature to control multiple SCA chips with one GBT link

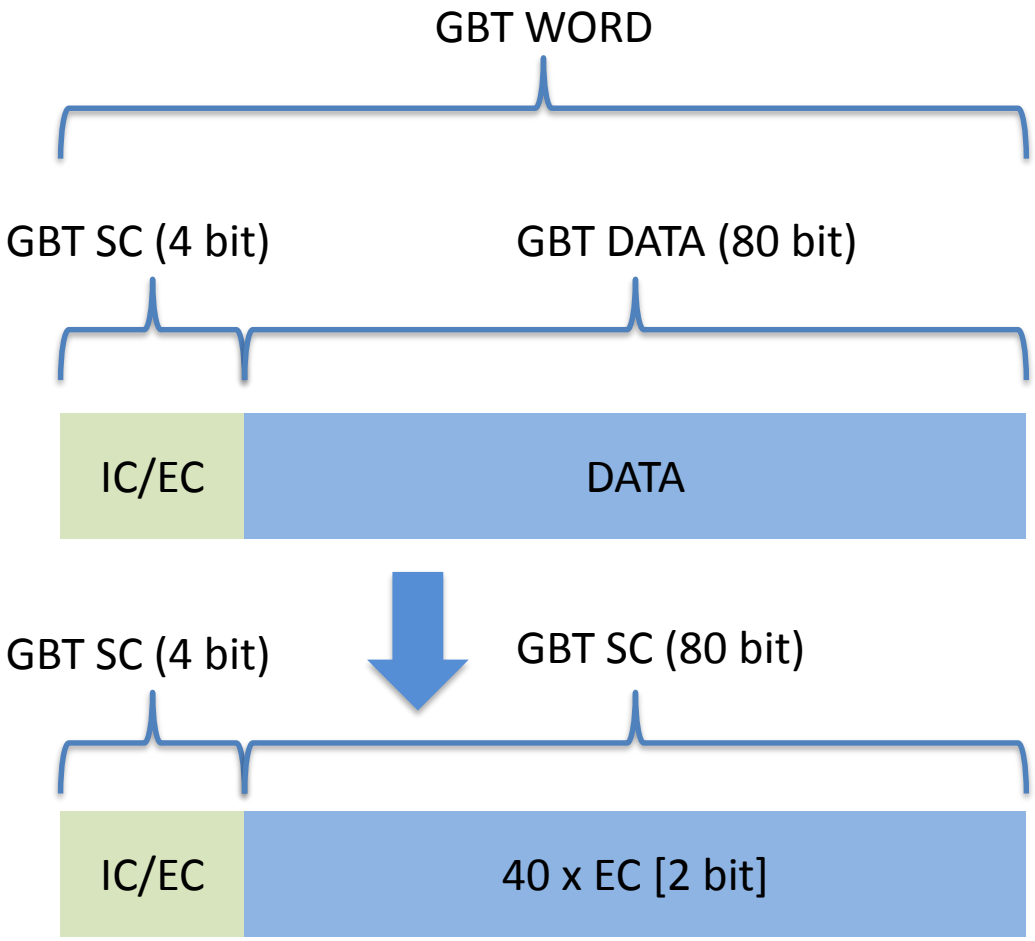
MFT – Services (WP7)

- DCS development very advanced
  - Development of all panels almost finalized
  - Definition of operation procedures on-going (SUPERSAFE, SAFE, …)
- Detector control using GBT-SCA (on PSU) through CRU
  - Development on-going using CRU/FLP/ALF/FRED/WinCC chain
  - Test bench to be set up at CERN and then sent to Hiroshima



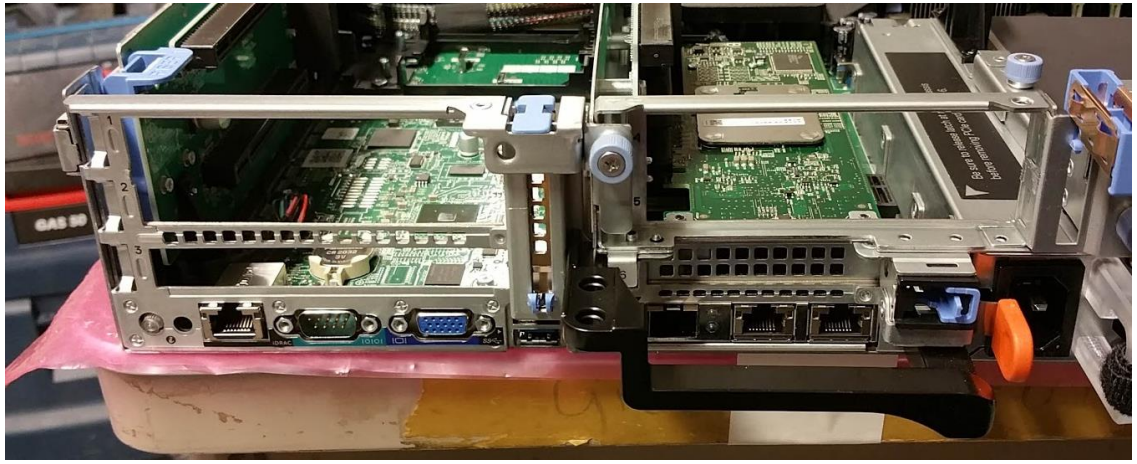


ALICE MFT

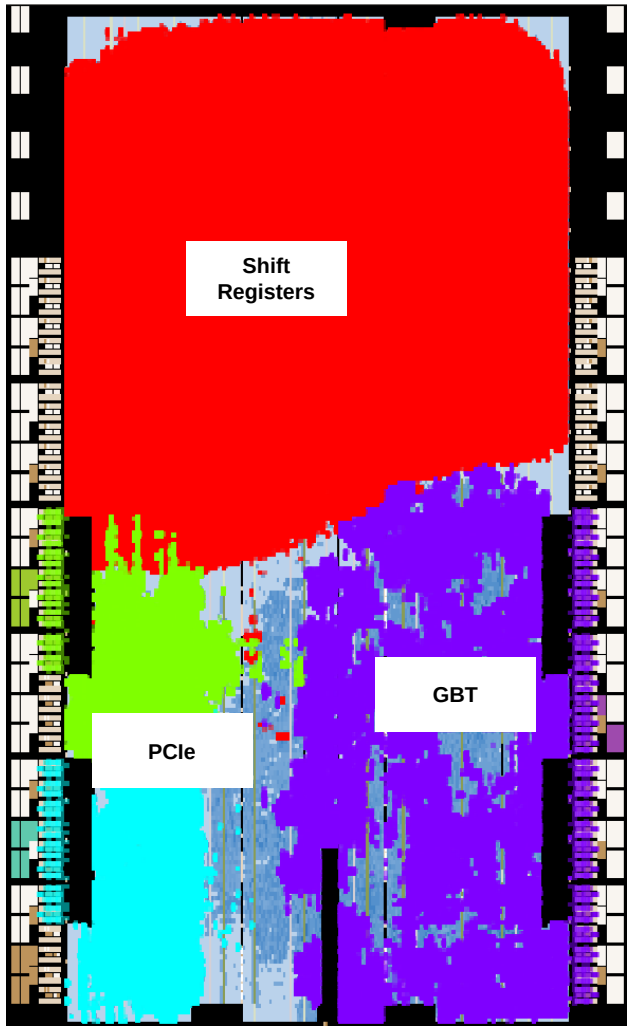


Tests ongoing with MFT-Japan

- 1 FLP delivered at CERN
  - Preparation at CERN in progress:
    - Cutting of the FLP chassis.
    - O^2 software.
    - CRU software.
  - Arria X development kit available.



CRU STRESS TEST - 750K FFs



Flow Summary	
Logic utilization (in ALMs)	312,636 / 427,200 (73 %)
Total registers	997490
Total block memory bits	17,917,984 / 55,562,240 (32 %)
Total DSP Blocks	0 / 1,518 (0 %)
Total HSSI RX channels	41 / 72 (57 %)
Total HSSI TX channels	41 / 72 (57 %)
Total PLLs	56 / 144 (39 %)

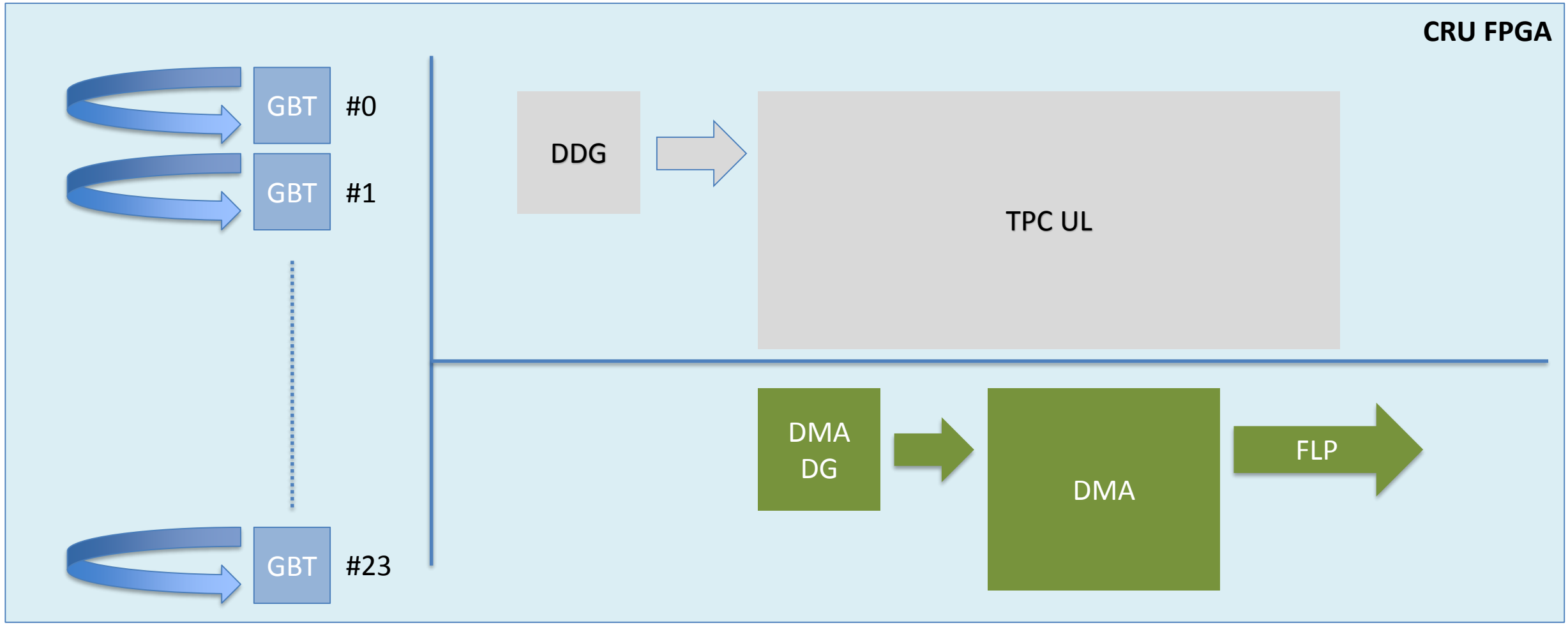
Errors per Second vs Toggling Rate (250K FFs)

		Errors per Second vs Toggling Rate				
CRU (Arria 10 ID)	TX	0%	25%	50%	75%	100%
	#	[EPS]	[EPS]	[EPS]	[EPS]	[EPS]
00540186-2858030e	**5**	**3**	**-**	**-**	**-**	**17**
	8	**12**	**-**	**-**	**-**	**6796**
00540186-28520504	**0**	**0.006**	**0.14**	**0.6**	**17.8**	**67**
00540186-28580507	**8**	**13**	**358**	**3190**	**21242**	**131831**
00540186-2858060a	*****	**0**	**-**	**-**	**-**	**0**
00540186-2855060b	**8**	**0**	**0.6**	**0.6**	**58.3**	**1756**
00540186-2855ff0f	*****	**0**	**-**	**-**	**-**	**0**

- Different cards show different level of sensitivity
- Different links (in the same card) show different level of sensitivity (link #8 looks to be the most sensitive)
- Error rates are proportional to the toggling rate
- Only transmitters affected (this can be seen when we switch between internal/external loopback mode due to link order reversion in the MiniPODs)
- The low rate errors detected in wide bus mode are completely eliminated by the FEC in GBT mode (the FEC error counters show all the corrections)

CRU STRESS TEST – TPC UL stress test

- TPC-UL firmware based on CRU firmware 2.5.0



CRU STRESS TEST – TPC UL stress test

#	Type	PCI Addr	Vendor ID	Device ID	Serial	FW Version	Card ID
0	CRU	02:00.0	0x1172	0xe001	0	0-0-bc5a2739	00000002-00000000
1	CRU	03:00.0	0x1172	0xe001	0	0-0-bc5a2739	00000002-00000000
2	CRU	81:00.0	0x1172	0xe001	0	0-0-bc5a2739	00000002-00000000
3	CRU	82:00.0	0x1172	0xe001	0	0-0-bc5a2739	00000002-00000000

python report.py -i 2:0.0

Link ID	GBT TX mode	GBT RX mode	GBT mux	Datapath mode	Enabled in datapath
Link 0 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 1 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 2 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 3 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 4 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 5 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 6 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 7 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 8 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 9 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 10 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 11 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 12 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 13 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 14 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 15 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 16 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 17 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 18 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 19 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 20 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 21 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 22 :	GBT	GBT	TTC:CTP	packet	Enabled
Link 23 :	GBT	GBT	TTC:CTP	packet	Enabled

DMA test
2 Eps parallel

Seconds 19319.7
Superpages 12781946880
Bytes 1.0471e+14
GB 104710
GB/s 5.41986
Gb/s 43.3588
GiB/s 5.04763
Errors 0

Seconds 19709
Superpages 14250186240
Bytes 1.16738e+14
GB 116738
GB/s 5.92304
Gb/s 47.3844
GiB/s 5.51627
Errors 0

GBT loopback test

python loopback.py -i 2:0.0 -l all -c 30bit -s all > /tmp/loopback_data_1917
seconds

1

1489381439/ 2715	1489349983/ 1917	1489350882/ 2270	1489366729/ 2730	1489370967/ 2574	1489358271/ 1963
1489364077/ 2148	1489360610/ 2198	**1489363277/ 2469**	1489357000/ 2138	1489353075/ 2223	1489353204/ 2000
1489370168/ 1944	1489354773/ 1887	1489389404/ 1981	1489358021/ 2037	1489361021/ 2693	1489365931/ 3062
1489353553/ 2429	1489379736/ 2111	1489356288/ 2923	1489380347/ 2397	1489358005/ 1909	1489389097/ 2763

2

1489381439/ 2715	1489349983/ 1917	1489350882/ 2270	1489366729/ 2730	1489370967/ 2574	1489358271/ 1963
1489364077/ 2148	1489360610/ 2198	**1489363277/ 2482**	1489357000/ 2138	1489353075/ 2223	1489353204/ 2000
1489370168/ 1944	1489354773/ 1887	1489389404/ 1981	1489358021/ 2037	1489361021/ 2693	1489365931/ 3062
1489353553/ 2429	1489379736/ 2111	1489356288/ 2923	1489380347/ 2397	1489358005/ 1909	1489389097/ 2763

3

1489381439/ 2715	1489349983/ 1917	1489350882/ 2270	1489366729/ 2730	1489370967/ 2574	1489358271/ 1963
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4

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1489353553/ 2429	1489379736/ 2111	1489356288/ 2923	1489380347/ 2397	1489358005/ 1909	1489389097/ 2763

Link#8 errors 13 error per sec

Tests should be repeated … this was the first try before the meeting, it is too early to get conclusions out of these results.

CONCLUSIONs

- Many detectors received the CRU to collect data from their FEE.
  - CRU and O^2 are providing support based on the feedback.
- Tools to stress test the CRU have been developed and can be used to debug the card:
  - ALICE FULL FPGA
  - CRU - TPC UL
  - LHCb framework
- We will repeat the same tests once we gain access to a CRU with the modified PCB

THANK YOU

Tests ongoing with TPC

- 10 FECs (20 GBT links) connected to 1 CRU:
  - SCA configuration and monitoring -> OK.
  - DMA :
    - readout in continuous mode, limited amount of data before dropping packets (2000 time-bins, ~ 33 packages * 8 kB),
    - SYNC trigger generated upon SOx received to start data taking with multiple CRUs,
    - readout.exe used, official O^2 readout software.

- Work in progress:
  - New firmware features.
  - Test with TPC UL in the CRU to check the quality of data.

Tests ongoing with TOF

- 2 DRMs (2 GBT links) connected to 1 CRU
  - DMA :
    - readout in packet mode,
    - triggers generated from CRU,
      - generation of trigger @ fixed BCs.

- Work in progress:
  - Clock forward from LTU – CRU – FEE to be tested.
  - readout.exe used, official O^2 readout software.

Tests ongoing with MID

- 1 FEE (1 GBT links) connected to 1 CRU:
  - SCA configuration and monitoring -> OK.
  - DMA :
    - readout in continuous mode,
    - triggers generated from CRU,

- Work in progress:
  - Clock forward from LTU – CRU – FEE to be tested.
  - readout.exe used, official O^2 readout software.

Tests ongoing with MCH

- 1 SOLAR (1 GBT links) connected to 1 CRU:
  - SCA configuration and monitoring -> OK.
  - DMA :
    - readout in continuous mode,
    - SYNC trigger generated upon SOx received to sync more CRUs,
    - readout.exe used, official O^2 readout software.

- Work in progress:
  - Write software to validate the MCH UL to be developed in firmware.
  - Develop the SC using the DCS framework.

Stress tests with FPGA (LHCb framework)

- LHCb software/firmware
  - installed in our server and modified for our requirements,
  - firmware tested on our cards,
  - ready to install it and provide support to Indian colleagues.