

CRU core firmware

Filippo Costa

CRU





Feedback report with several detector groups

<https://alice-talk.web.cern.ch/c/o2-cru>

Topic	Users	Replies	Views	Activity
🚩 About the O ² CRU category		0	20	Jun 12
TPC Readout with CRU		17	7	3d
Which avalon_mm_slave and how to use it? ³		14	29	Aug 2
CRUv2 not recognized by FLP ²		8	12	Jul 27
☑ CRU USB cable		1	8	Jul 25
CRU hardware				
☑ CRU firmware compilation error				
Is flpproto no longer supported/needed?				
Hardware setting recommendations for FLP prototypes?				
CRU firmware				

[https://gitlab.cern.ch/alice-cru/pcoresng-cru/boards?=#](https://gitlab.cern.ch/alice-cru/pcoresng-cru/boards?=)

Backlog 14 +

- DDG RDH #96
- DATAPATH WRAPPER ODD number of words #95
- DDG odd/even number of words #94
- CRU Serial FLASH #92
- Update the FIELD in the RDH WORD0 #58
- PCIe internal data generator realistic trigger counters #56
- SYNC pattern seems to come irregular (not with a fixed distance as one would expect with a fixed heartbeat). Generated by Control-Pattern generator (Waveform-Player) #34
- ADDRESS SPACE for BAR2 too big #33
- PCIe CVP #51
- Manage flow chunk in dwrapper to avoid discontinuous data stream #67
- CTPEMulator : Implement the possibility to have single shot trigger #71

To Do 6 +

- assign proper device id to CRU #32
- PCIedma : remove old avalons and update pack_cru_core #74
- PCIEDMA Change M_ADDR size to 32 bit #70
- Reduce size of register in avalon slave when not needed #43
- PCIe FIFO Interface documentation #87
- Reduce address space used by I2C #89

Doing 4 +

- change dma_data_in trg generator #44
- Add PCIe error reporting #40
- I2C buses #48
- Generate PCIEDMA using the new QSYS #57

Closed 72

- Create separate dirs for all ips #3
- change make default output #5
- Integrate SWT in the GBTSC #17
- Generated product stored in ip-cru-v2 #6
- Simulation model generation issue #8
- Add counter to check the time it takes to send a SWT word to the ITS FEE and receive back the feedback #15
- modify qsys_gen.sh #9
- CRU SCA core #20
- remove swthandler #93
- Use the time domain multiplexing in GBT link #10
- Validate library removal #13
- Implement SWT protocol to ACK the transaction #16
- Add SUPERPAGE FIFO empty counter #1



Firmware TAG releases

v2.6.0

9bf047b2 · Addition of start/stop run override · 6 days ago

v2.5.0

910ae122 · Removed LINKID offset in datapath_wrappers · 3 weeks ago

v2.4.0

5168b6b8 · add information into the GBT configuration 1 description (· 1 month ago

v2.3.0

873c9ab1 · Issue #111 : changes to sync the TIC input with the one in output · 2 months ago

2.6.0 - 2018-11-09

- Addition of CRUID and dwrapper ID in word 0 of RDH for raw readout
- Patplayer always sends IDLE during configuration
- Addition of trig counter monitors
- Addition of start/stop run override

2.5.0 - 2018-10-26

- Add trigger re-routing option
- Add enable for runen trigger in patplayer
- Add TPC FEC emulator and ttc trigger select
- DDG send only RDH when SOT/EOT
- Add software controlled reset for clock related component and dwrapper
- Removed a reset in the SWT component to improve timing
- Simplified DMA internal data generator
- Add clk240 alive checker
- Applied fix for timing error in SWT
- CTPEMUCORE removed a critical warning
- Reduced reset fanout in PCIe to improve timing
- Removed unused monitoring logic to improve timing
- Add control for IDLEs between DDG packets
- Start of data taking enabled by SOx
- Add throughput counter to dwrapper
- Removed LINKID offset (both dwrappers are equivalent)



Main feature currently implemented

- Readout :
 - Continuous.
 - Packet.
- TRIGGER :
 - CTP emulator : HB and Triggers (Sox, Eox, PHYSICS).
 - LTU communication.
 - PatPlayer : detector “triggered” specific pattern.
 - MID trigger.
- Slow Control :
 - SCA.
 - SWT.
- Integration of Detector User Logic.
- DDG (Detector Data Generator) : continuous/packet mode.

Next milestone



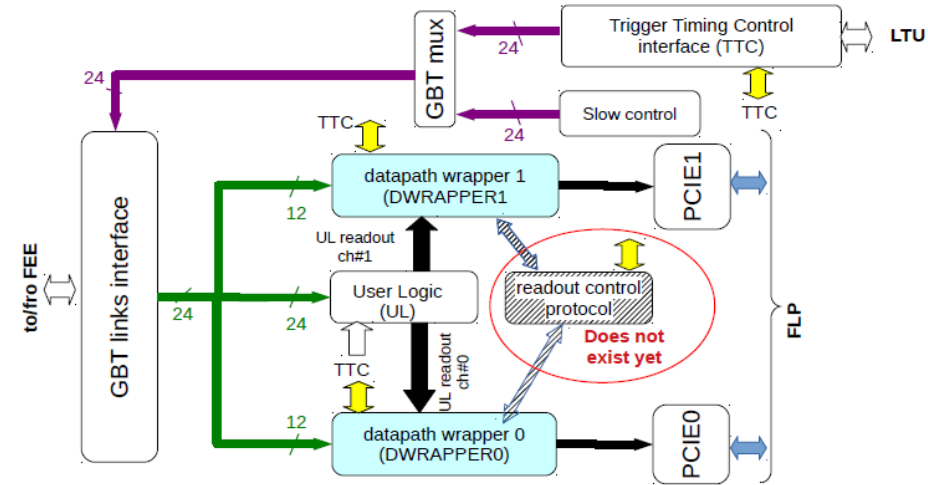
During the last **SYSTEM UPGRADE** the CRU Team presented the “Update on the readout control protocol”

For more details click [here](#)

Major highlights



- Implementation of the new “readout control protocol” in the CRU



Interfaces

- with FEE through GBT (wide or standard)
- with Central Trigger Processor (CTP) through the Local Trigger Unit (LTU)
- with Detector Control System (DCS) and DAQ through PCie

⇒ Talk will focus on DWRAPPERS and readout control protocol



Major highlights

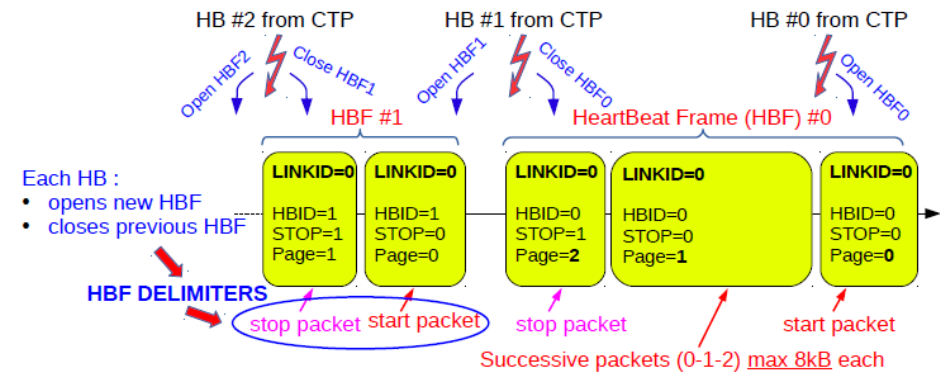


- Implementation of the new “readout control protocol” in the CRU
- Modification to the data transmission protocol

To be able to scrutinize the interleaved packets as they fly-by, we need **delimiters** to assess full and complete Heartbeats Frame transmission.

For all Heartbeats Frame (HBF) a min. of 2 packets should be emitted

- Start packet: 1st packet of a HBF → page #0
- Stop packet: last packet of a HBF → page #n and STOP at 1 (may contain some status, **TBD**)
- Both packets can be RDH only!

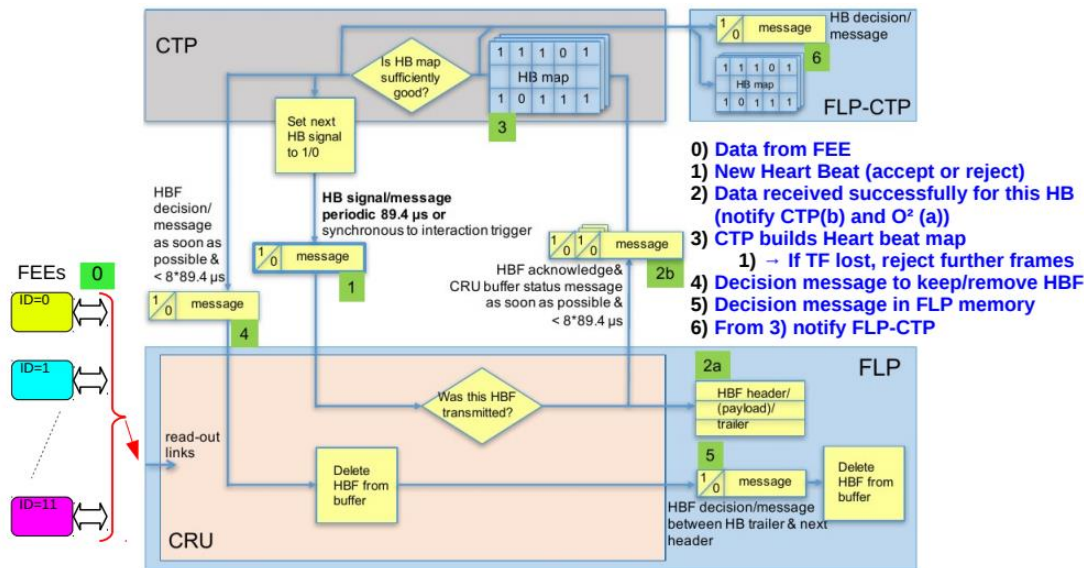


For continuous readout detectors, this will be taken care of by CRU

Major highlights



- Implementation of the new “readout control protocol” in the CRU
- Modification to the data transmission protocol
- CONCLUSIONS



- A solution exists for implementing the flow control protocol
- New HeartBeat Frame (HBF) must be introduced (step #0)
- Definition of HeartBeat Accept Message (HBam) and HeartBeat Decision Message (HBdm) were introduced by CTP and will be implemented

- Detectors must implement the communication protocol described
 - ⇒ This is for FEE with packet type **AND** for user logic
- Is geographical decision in CRU necessary ?
 - ⇒ If yes, please limit the number: 2? (impact on 2b message)
- Is a status word useful ?
 - ⇒ Could be used as payload in the stop packet, used by whom (CTP, O², both?)

- 1 Validate the new communication protocol with FEE (step #0)
- 2 Validate the CRU→CTP→CRU communication loop (steps 2b, 4, 5)
- 3 Validate the flow control with CTP