

Pixel Chip Production and Series Test

마거 매그너스 (CERN)

12th ALICE ITS upgrade, MFT and O2 Asian Workshop Inha University, Incheon, Korea 19-21 November 2018















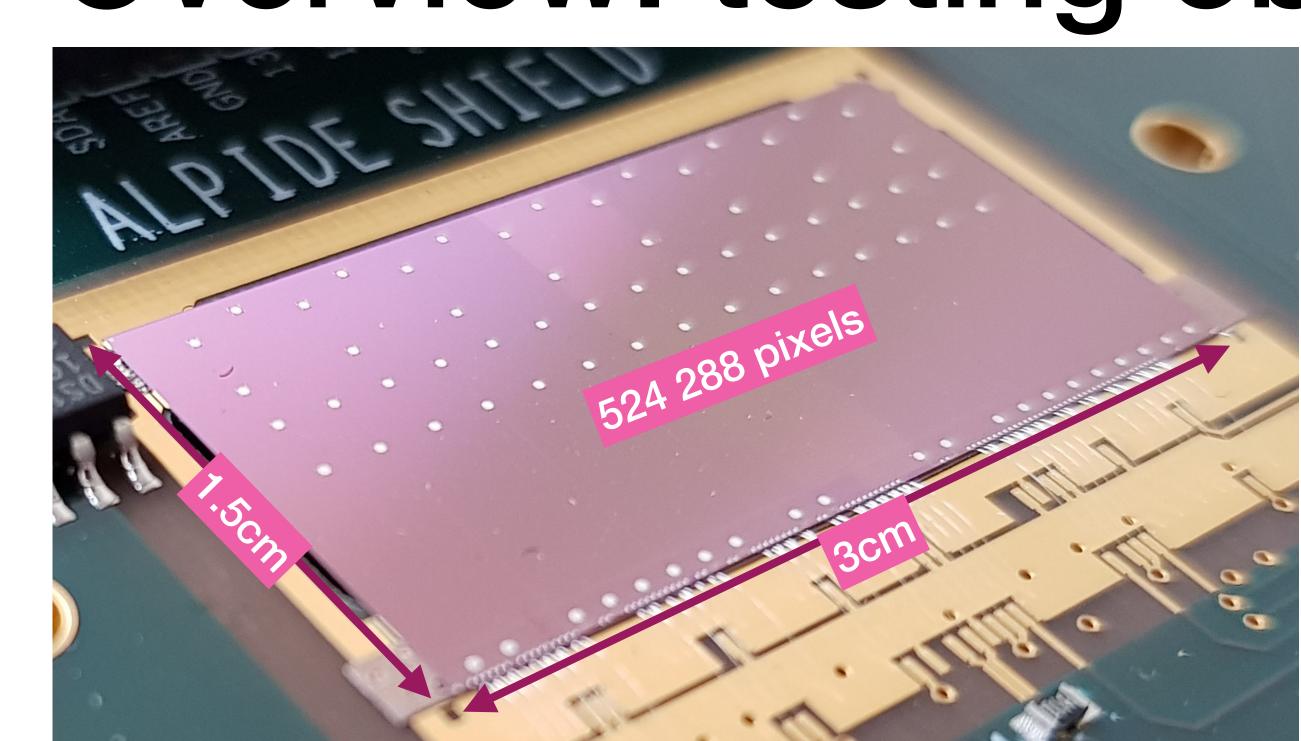
➡ Overview

- ➡ A bit of history
- ➡ Plans
- Yields
- Distribution

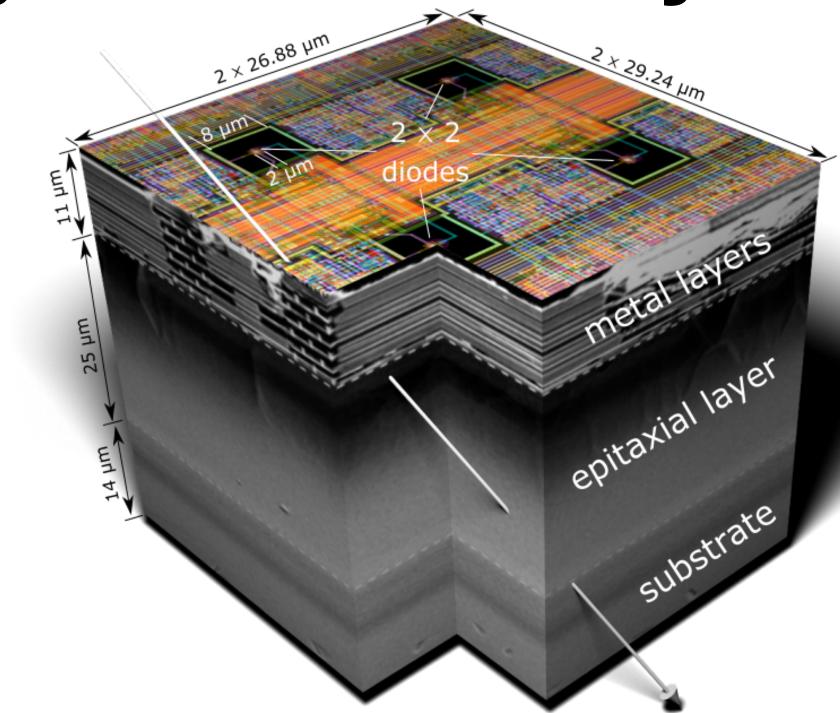
Outline



Overview: testing objective/subject



- delicate objects (mechanical + electrical)
- custom design requiring custom test systems lacksquare
- lots of analogue + digital functionality to be assessed
- more than 60 000 chips to be tested!



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- ~ 60 lots, ~1500 wafers produced
- more to come next year
- Module assembly requires continuous testing of ≥ 1 lot (25 wafers) / week
- + wafer QA (TMEC) + CMOS wafer testing (CERN)

Overview: flow

100 µm (vast majority): Inha/Pusan + Yonsei

Module assembly

CERN (IB, MFT) Bari (IT) Liverpool (GB) Pusan/Inha Strasbourg (FR) Wuhan (CN)

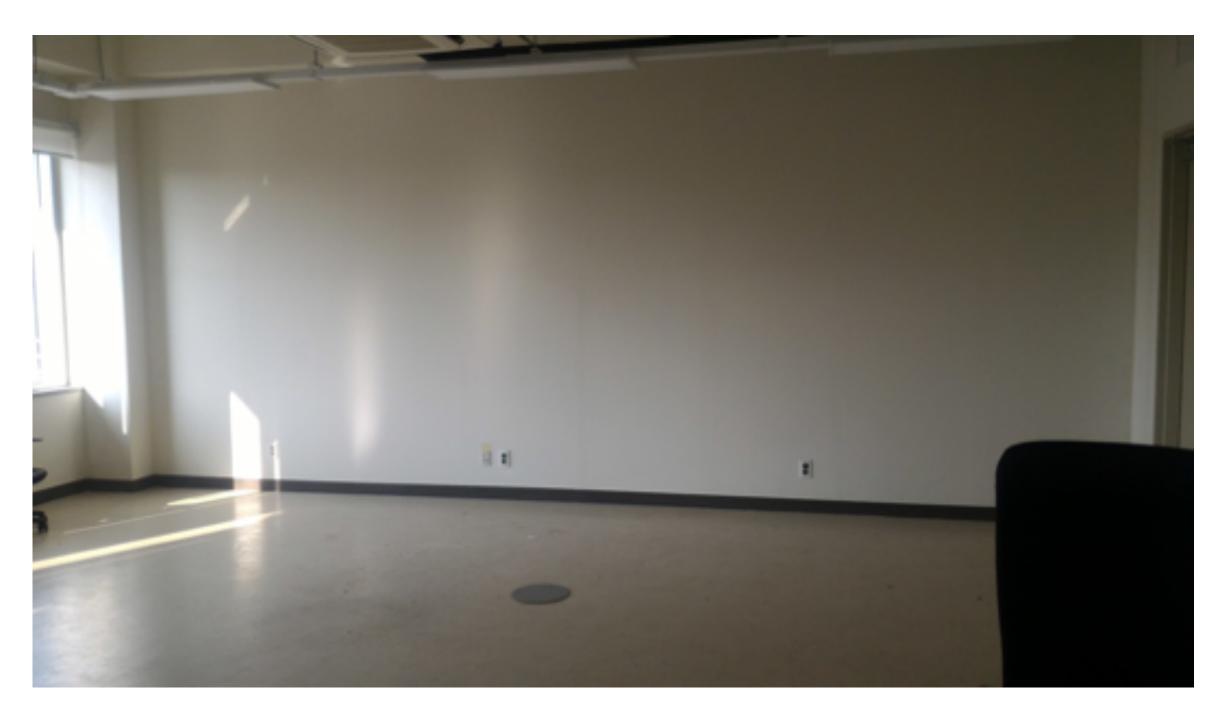
Production ongoing of more chips is ongoing: 15 lots (346 wafers) by end-2018,







- But, we really started from scratch
- Here a few selected moments starting some 40 thousand tested chips ago...



History

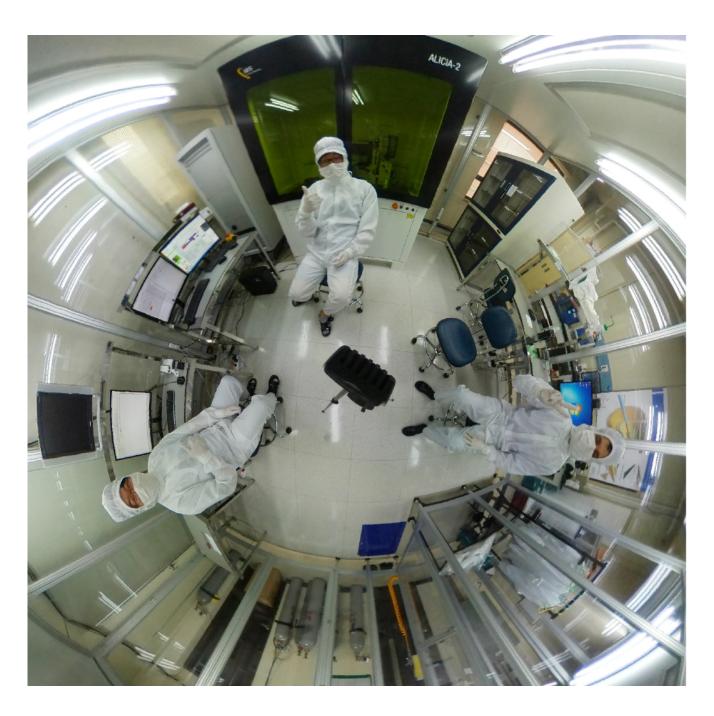
• Today, we have these beautifully working setups and teams operating them smoothly





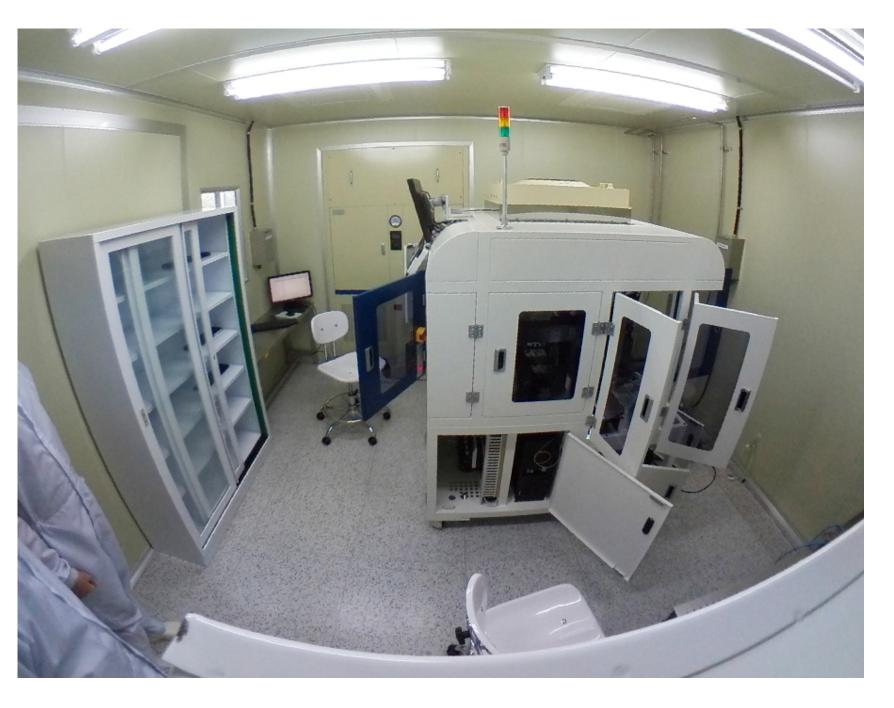
- But, we really started from scratch
- Here a few selected moments starting some 40 thousand tested chips ago...





History

• Today, we have these beautifully working setups and teams operating them smoothly







- First probing system (pALPIDE-2) is commissioned
- Based on "DAQ board" + probe card
- Rudimentary contact test logic, turned out to be very useful
- Still a lot of trial+error
- For example: chip interface pads were not yet finalised, Ni/Au coating still baseline for Laser-soldering

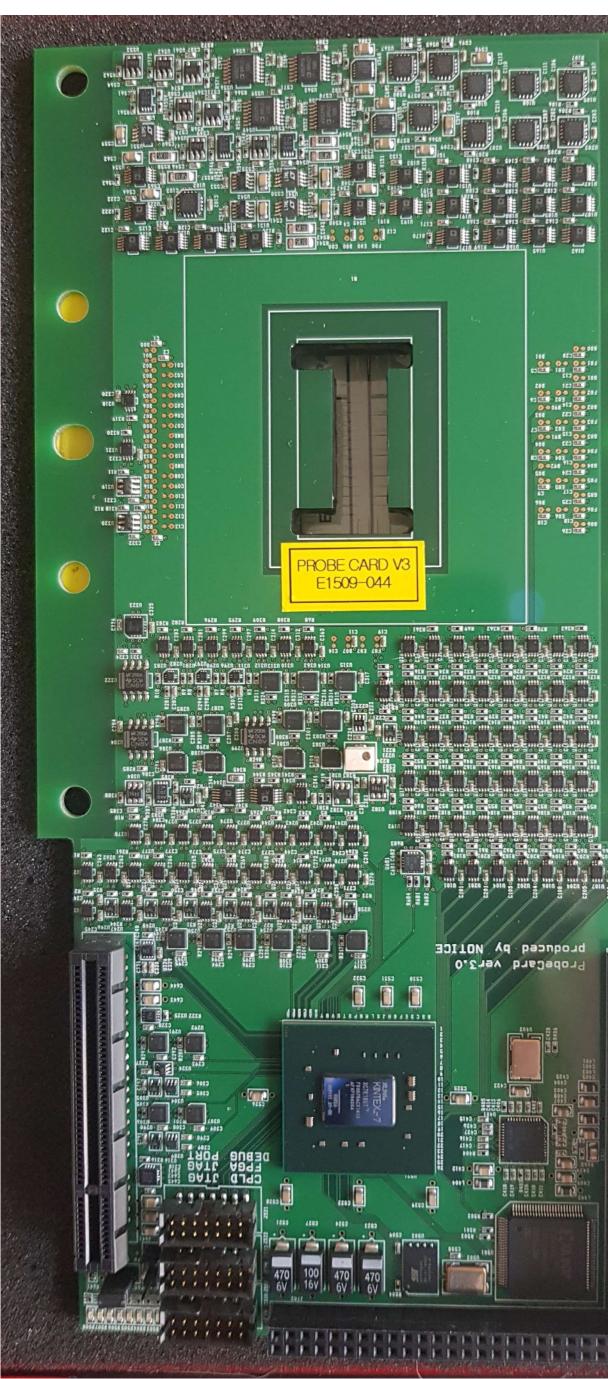
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2015-2016

- Redesign of probe card for pALPIDE-3/-4/ALPIDE
- Fully integrated solution
 - Hardware by notice (KR) via Yonsei
 - Firmware by CERN
- Same card for all chip tests (wafer prober + ALICIA) machines + Yonsei machine)
- Improved contact test logic

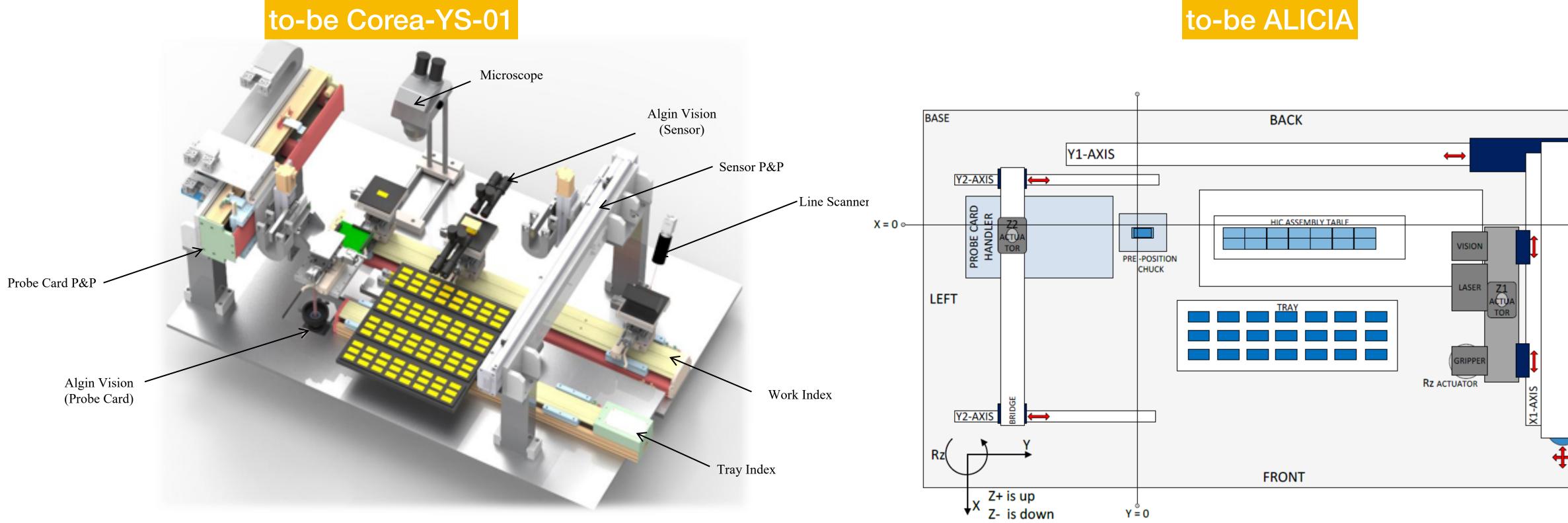




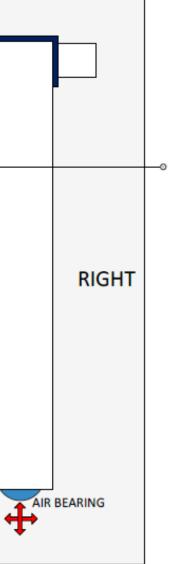


2015-2016

• Machine designs











2015-2016

• Preparation of clean rooms





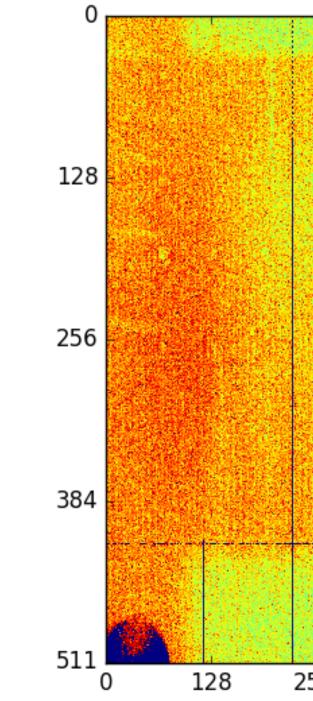








- First ALPIDE pre-production wafer arrive
- Testing result from probe station the same day
- ALPIDE is alive!
- (but light shielding had to be improved....)



Aug 19 2016

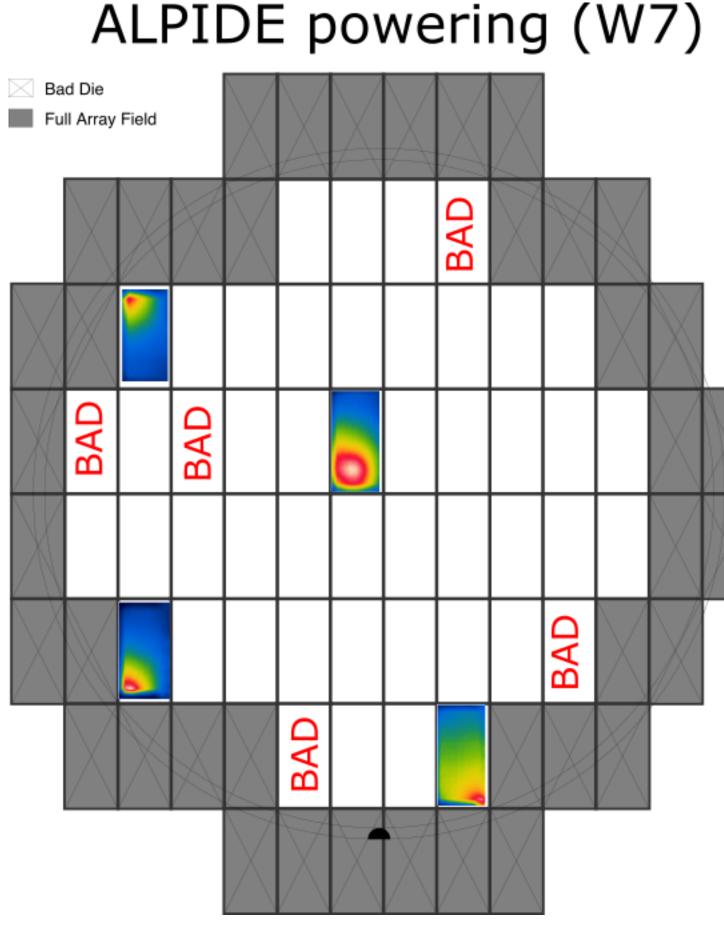
Threshold map 640 896 256 384 512 768 1023





Sep 2016

- First "real" finding from chip probe testing
- Perculiar failure mode of ALPIDE chips at wafer boundary emerged
- Wafer map was changed to use 46 instead of 48 chips
 - more space to circumference \bullet
 - effectively higher yield









Sep 22 2016

• Delivery of Corea-YS-01 to Yonsei Univ.







• Delivery of ALICIA-2 to Pusan Univ.



Nov 7 2016





- Site acceptance test ALICA-2 at Pusan Univ. (Pusan/Inha team)
- All works!

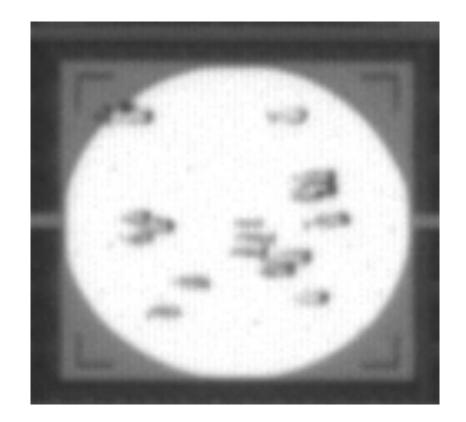


- Test of Corea-YS-01 at Yonsei Univ.
- Probing not reliably (will eventually turn out to be really bad luck)



First half of 2017

- Long period with several delays
- Teams in standby
- No production chip testing
- Lots of testing of probe cards at Yonsei



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July 28th 2017

- First fully automated ALPIDE test at Inha/Pusan
- Smooth running afterwards

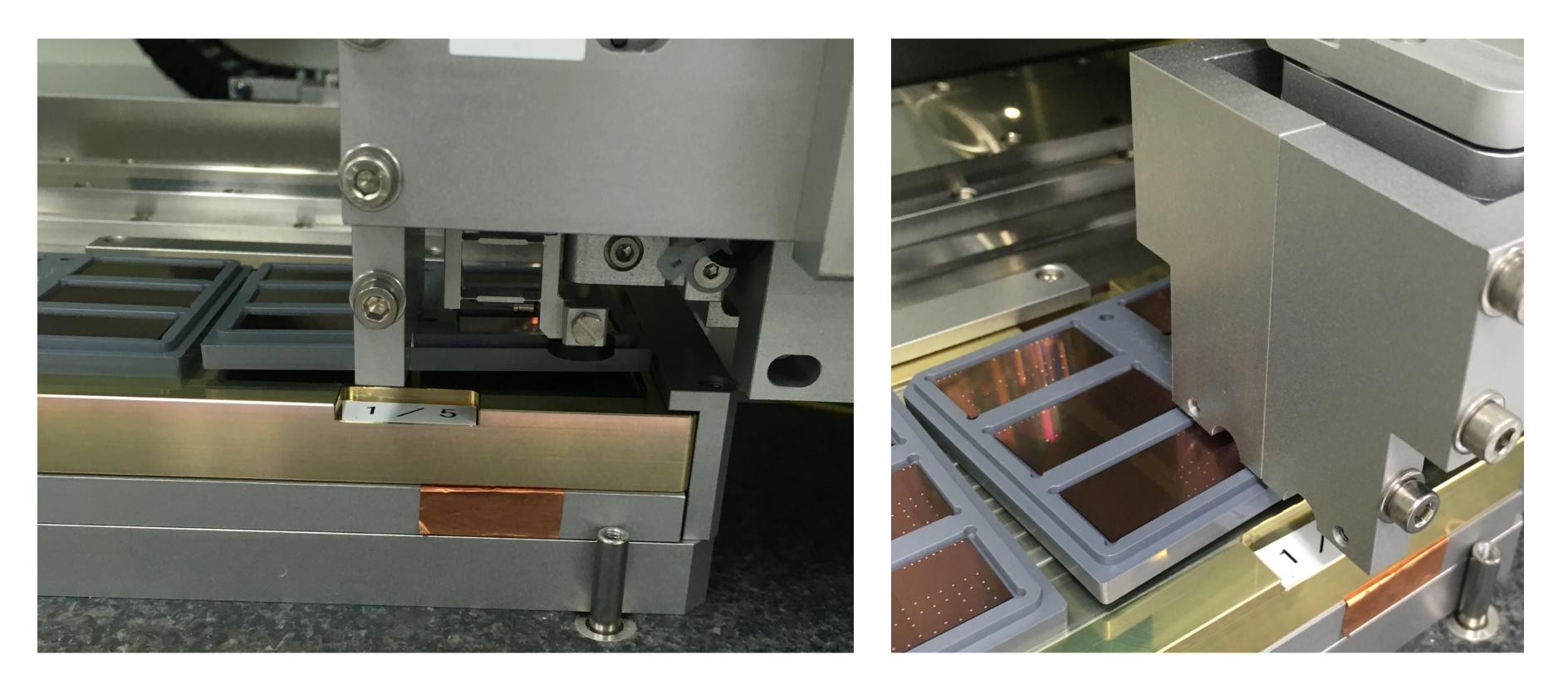


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Gripper incidents at CERN and Pusan/Ina



Aug 8+9 2017





- Production test starts in Yonsei
- This ends a long trouble-shooting period
- unreliable results were send to CERN
- was really due to bad luck

Feb 2018

Eventually the two probe cards that were used at Yonsei and produced

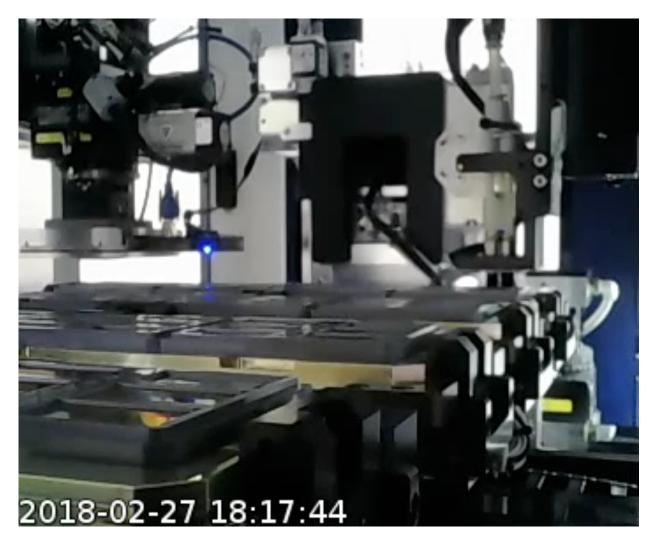
• They also behave badly at CERN, i.e. by now we know that the late start

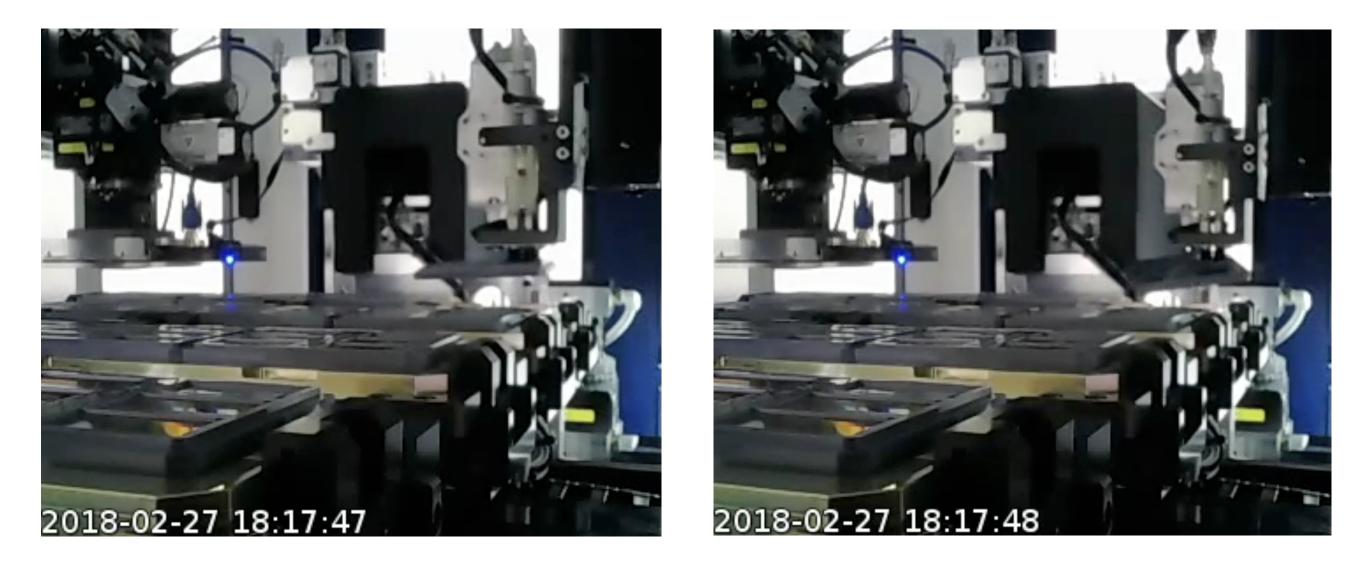
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Feb 27 2018

- Near-Incident at Yonsei
- into machine
- Luckily no damage



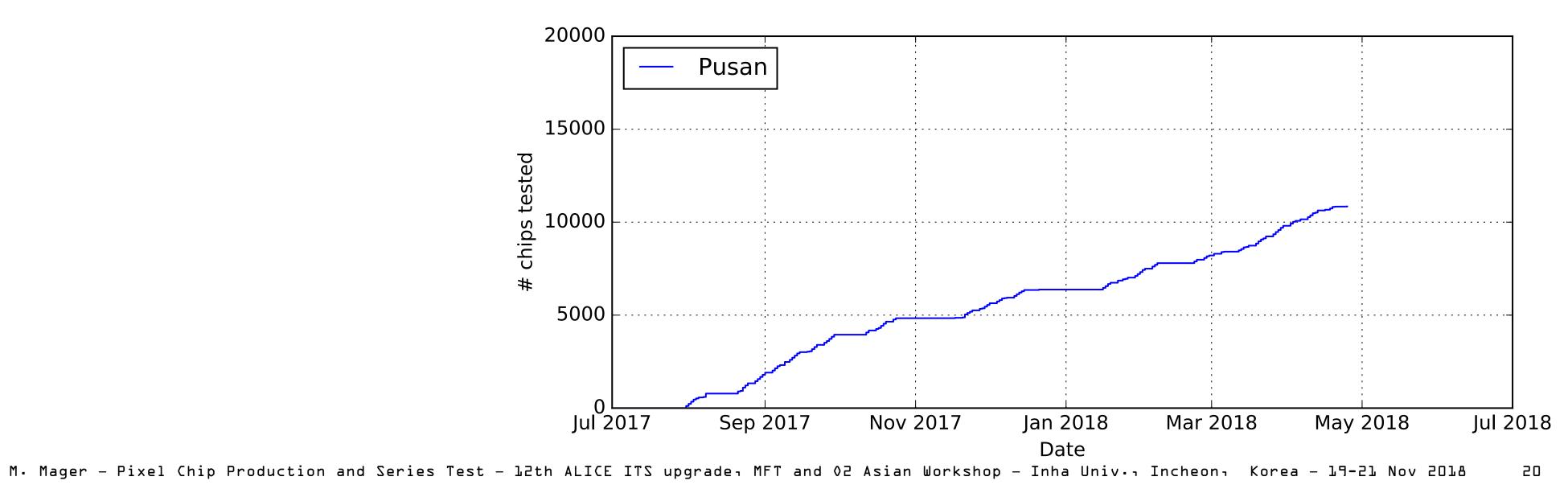


Database content for tray incorrect, chip-picker picks tray and crashes it



Apr 2018

- Planned stop of chip testing at Pusan/Inha
- Module construction largely relied on the chips tested by Pusan
- Meanwhile, verification of availability as back-up site completed
- Congratulations to the Pusan/Inha team!



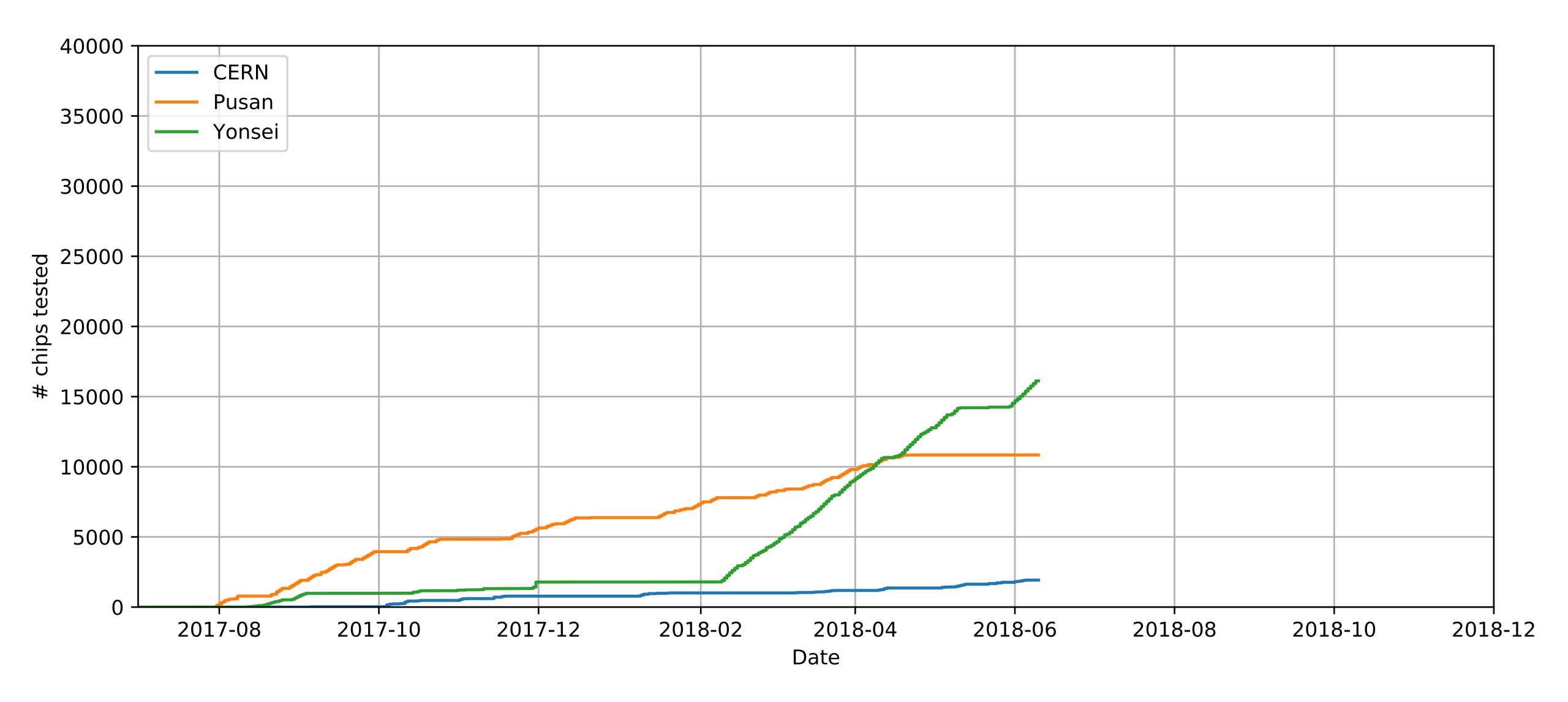


Oct 2018

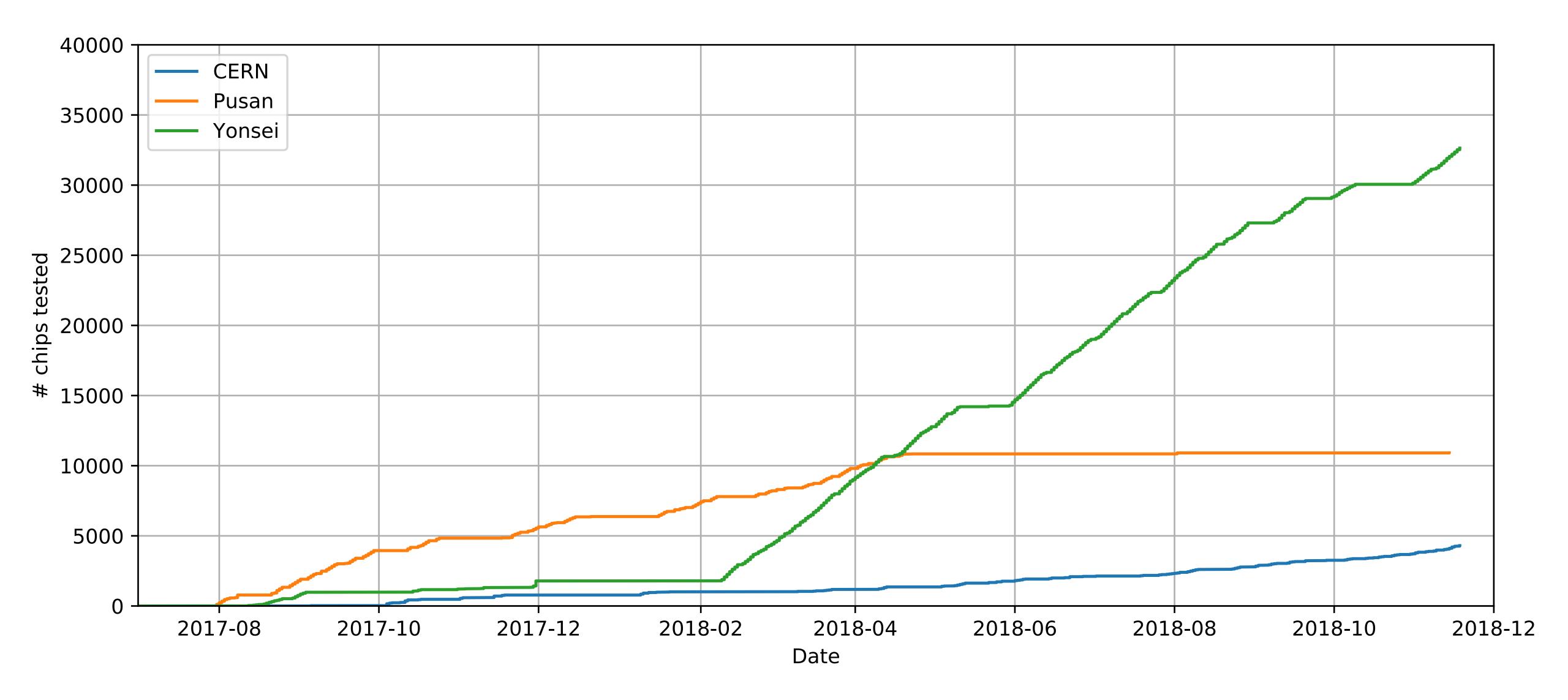
- MFT also joins chip testing
- smooth set-up of soft- and hardware
- Need to discuss spare probe card
 - currently 2 cards at CERN: ITS+MFT
 - Inha/Pusan card could become common spare



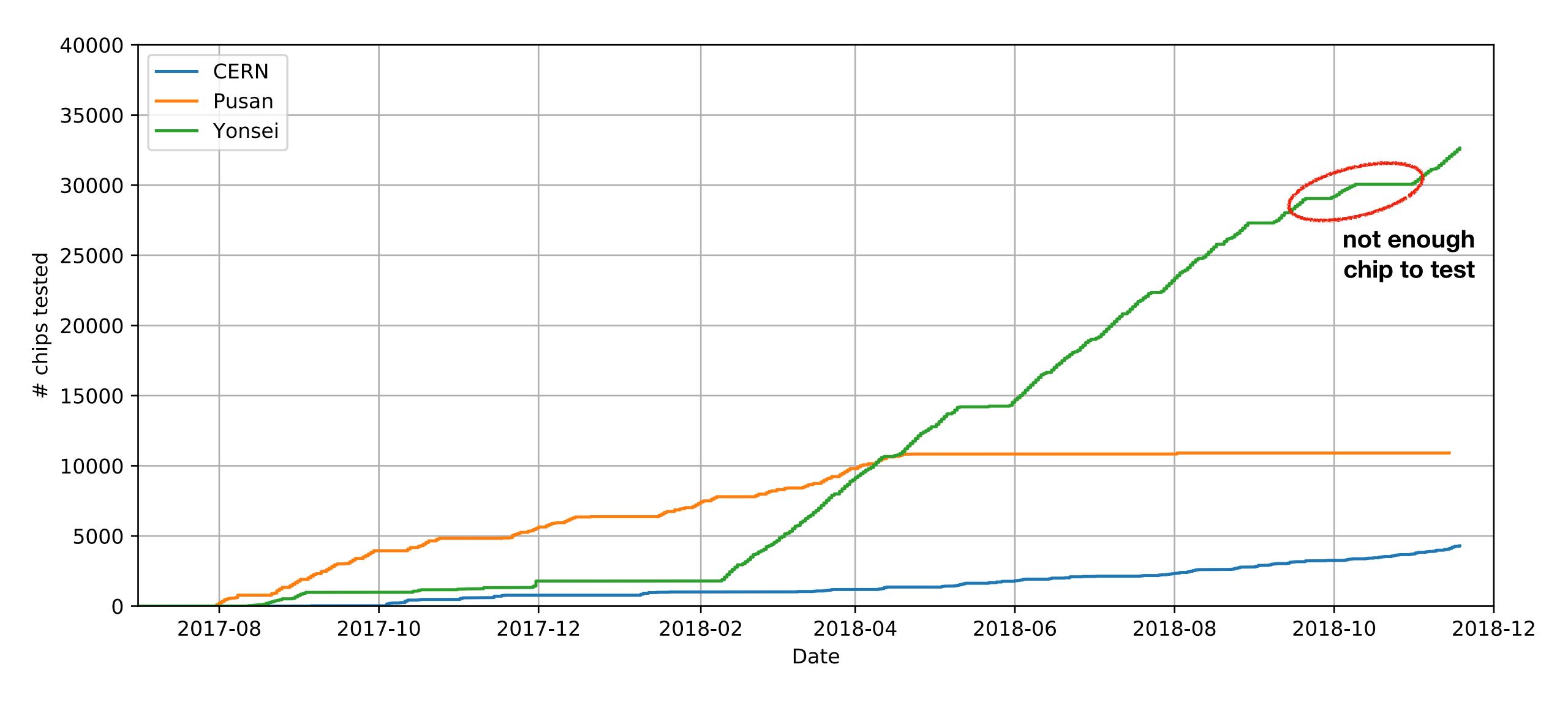














(Near) future

- ALPIDE production continues
- Rely on Yonsei for full test if 100-µm chips
 - Team is prepared for 24/7 operation (including shifter housing)

Congratulations to the Yonsei team for their smooth operation!

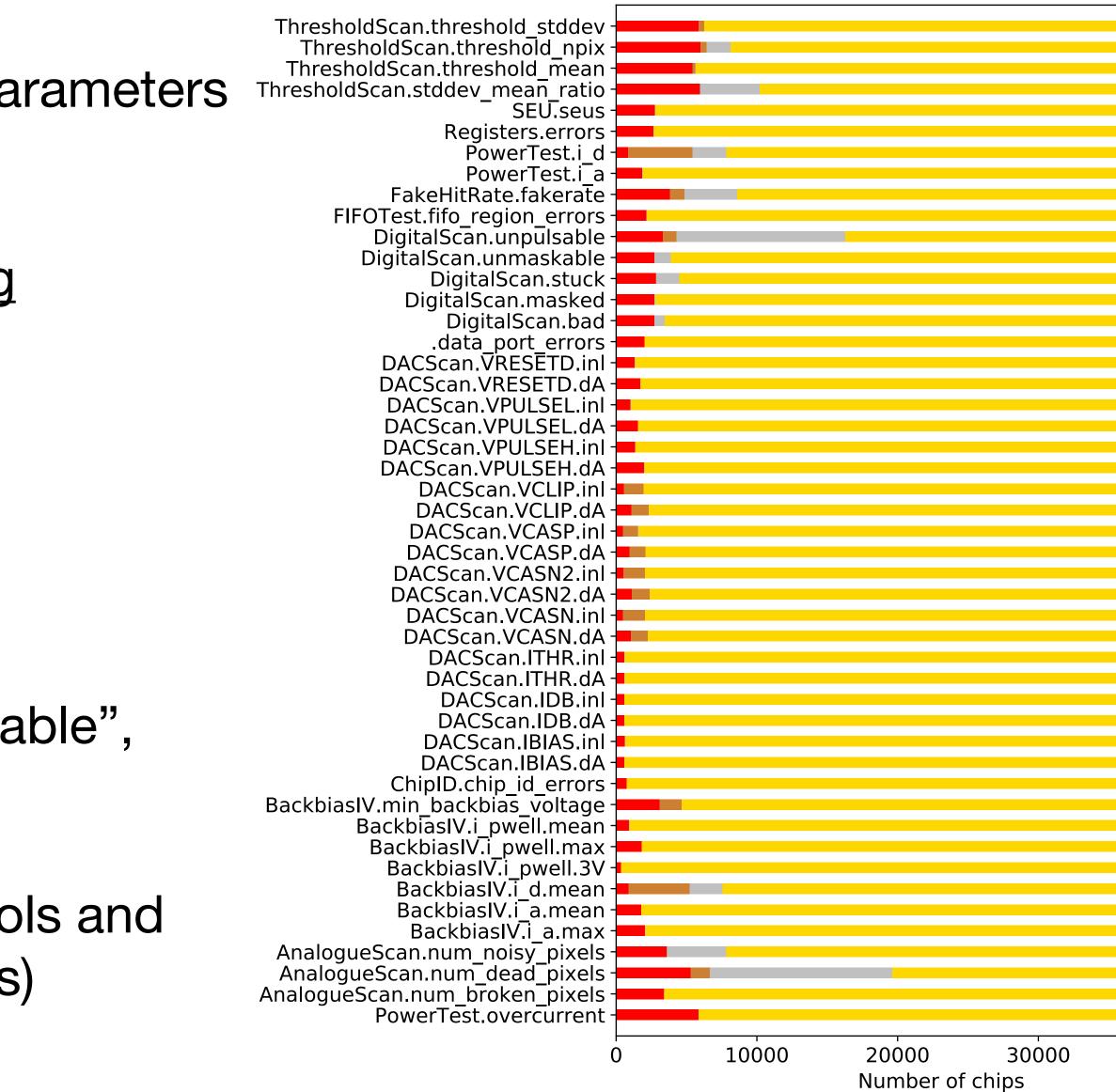
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- Comprehensive yield extraction, tuned cut parameters
- document, constantly updated: https://www.overleaf.com/read/wkmkcrjqtfsg
- Classifying chips as: **GOLD:** for IB SILVER: for OB (also uses GOLD) **BRONZE:** for OB spares **BRONZE-NOVBB:** for OB spares?) **BAD:** rest (could be further split: into "powerable", "short")
- NB: IB and OB chips come from different pools and are not interchangeable (different thicknesses)

Yields

Classification results

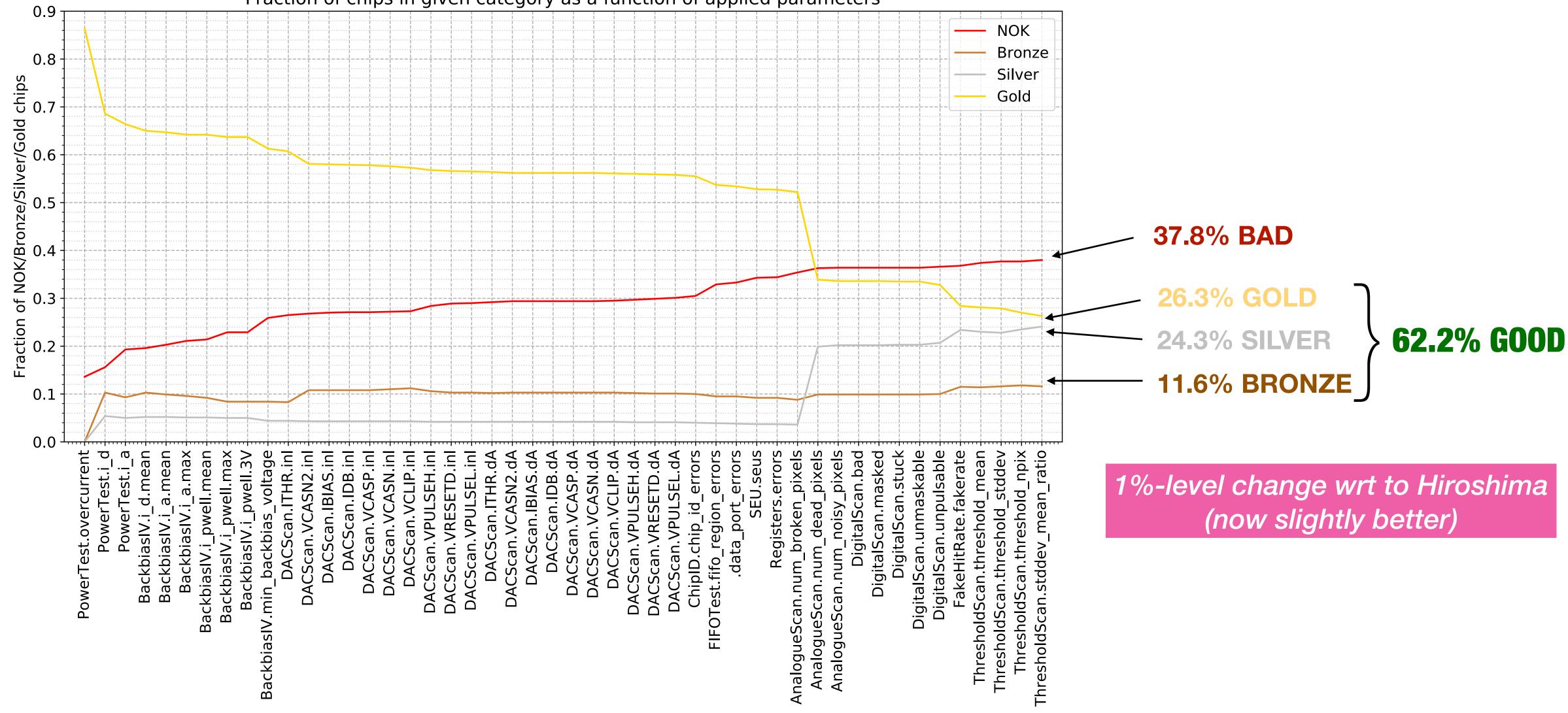




Yields summary



Fraction of chips in given category as a function of applied parameters





Smooth distribution to assembly sites

- After initial learning curve, packaging is done very well
- Delivery is in time and chips do not cause delays

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Distribution





Satus

- ✓ Wafer testing at CERN is completed
- ✓ 50 µm chip tests at CERN ongoing
 - **MFT has joined** testing on their machine (ALICIA-7)
- ✓ 100 µm chip tests in Pusan sopped end-April 2018
 - very productive period
 - now focus on module production
- ✓ 100 µm chip tests in Yonsei started in Feb 2018
 - smooth operation
 - faster than supply

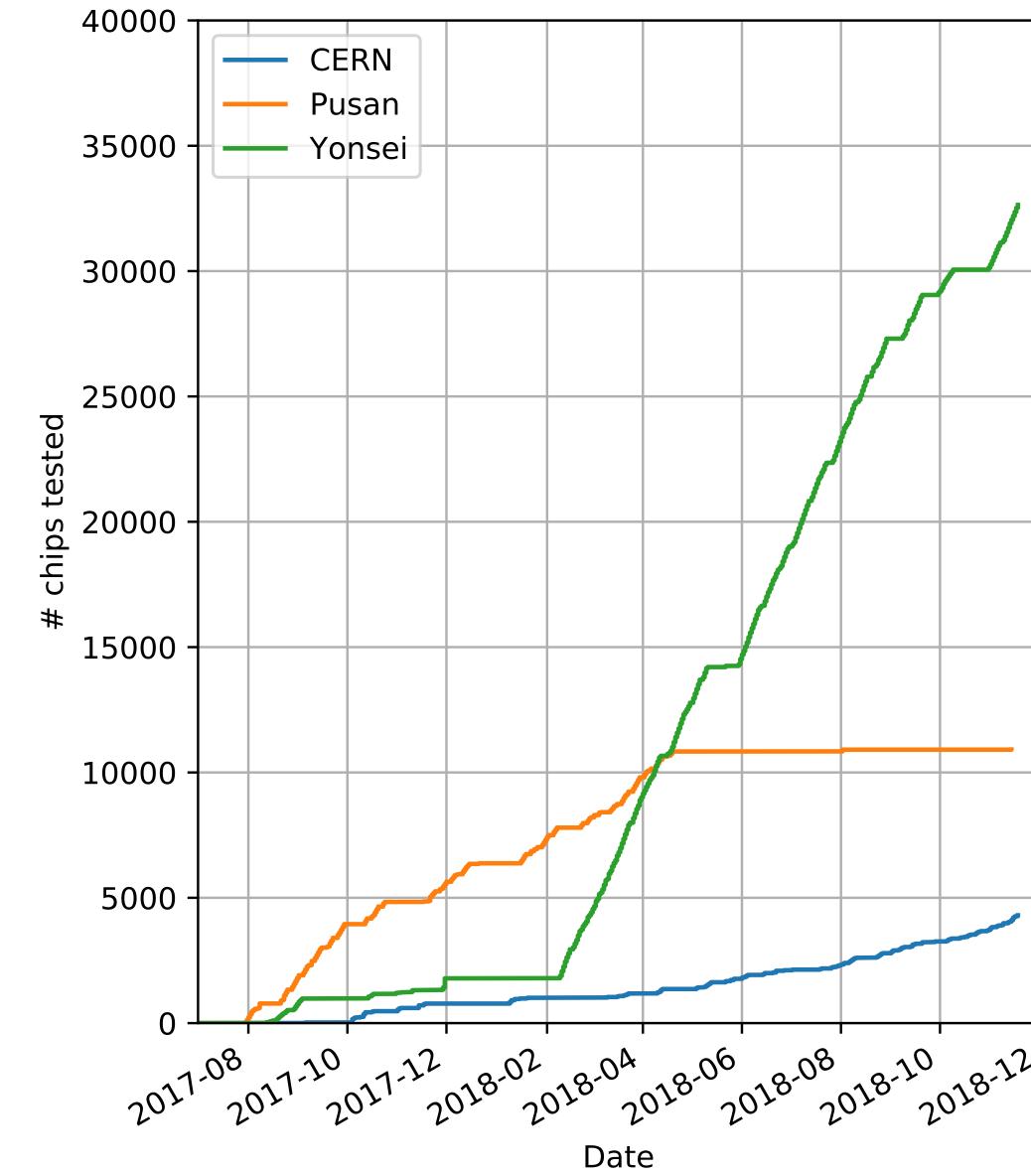
Summary

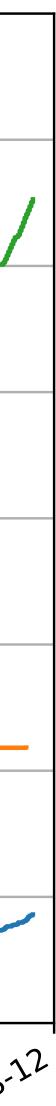
- \checkmark chip testing is a **very challenging** activity, involving
 - many people (shift crews, developers)
 - many custom made parts (hard-, firm-, software)
 - different institutes and companies
- ✓ we have already **produced** a lot of results
 - yield summary
 - distribution of chips for modules

Outlook

✓ Still a lot of work ahead of us. **Keep going!**

Summary & Outlook









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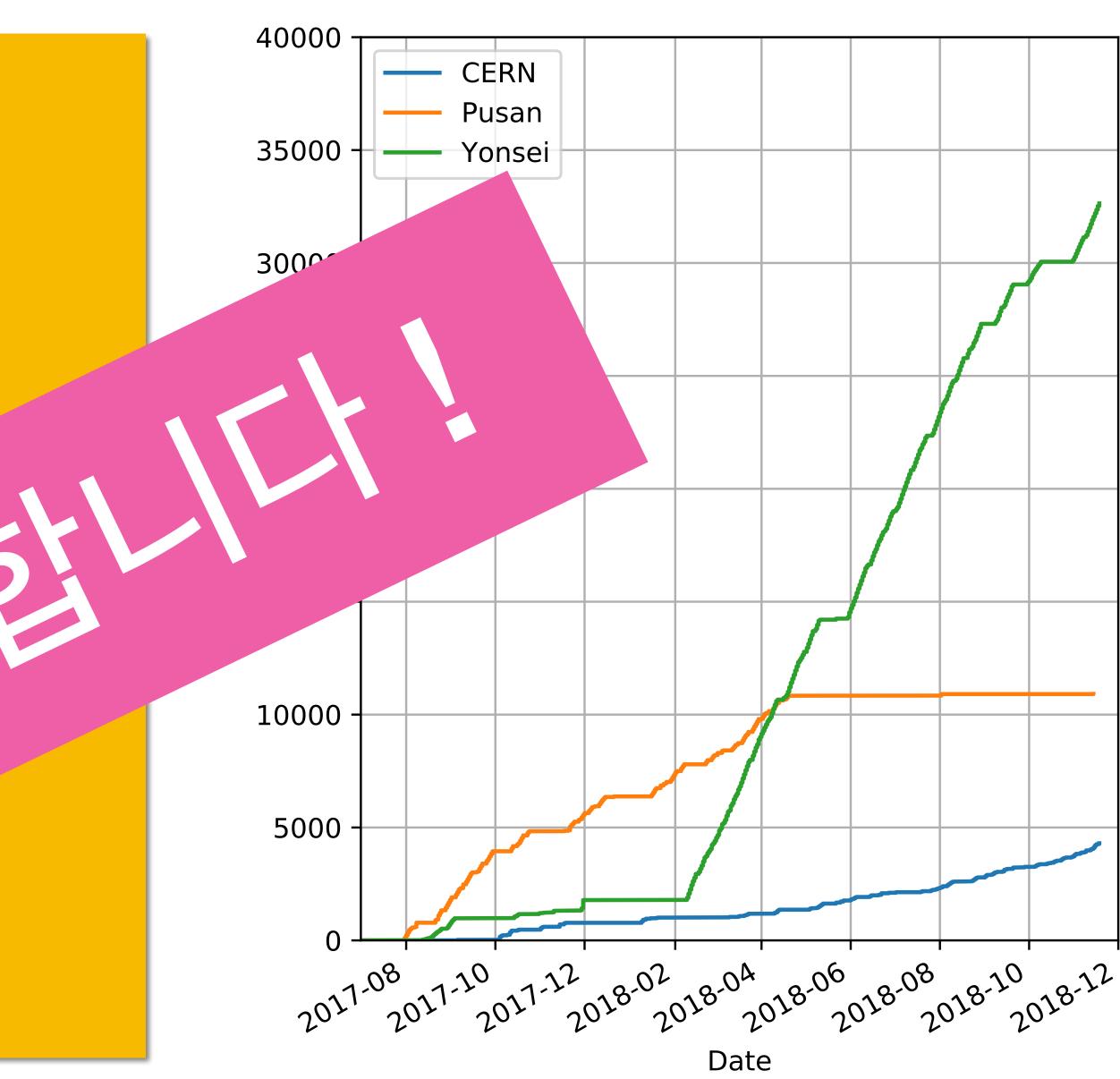
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Summary & Outlook

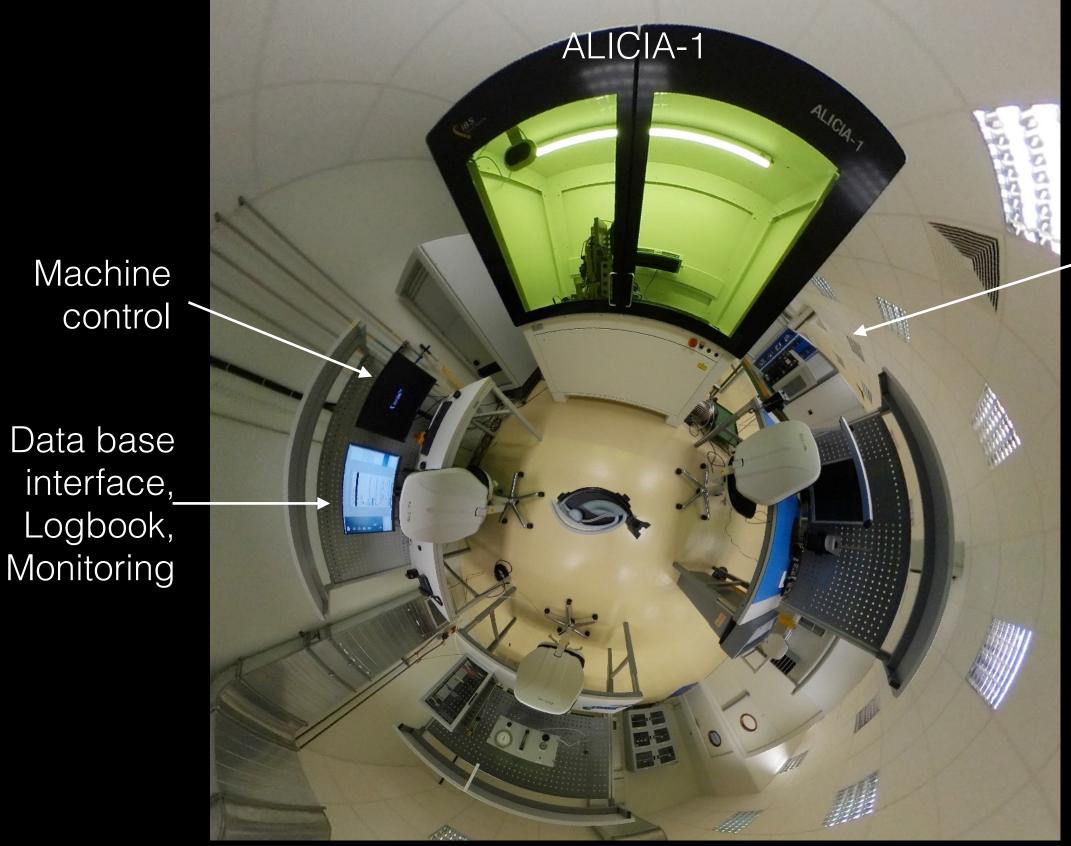








50 µm-thick chip testing





Wafer probe testing

Wafer storage

Chip storage



Wafer prober

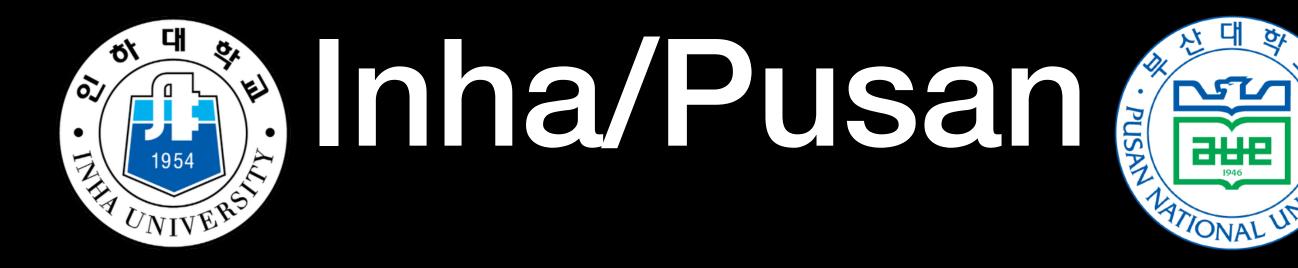
Data base interface, Logbook, Monitoring

Clean room tent (in clean room)











Machine control

Database interface

Logbook, Monitoring









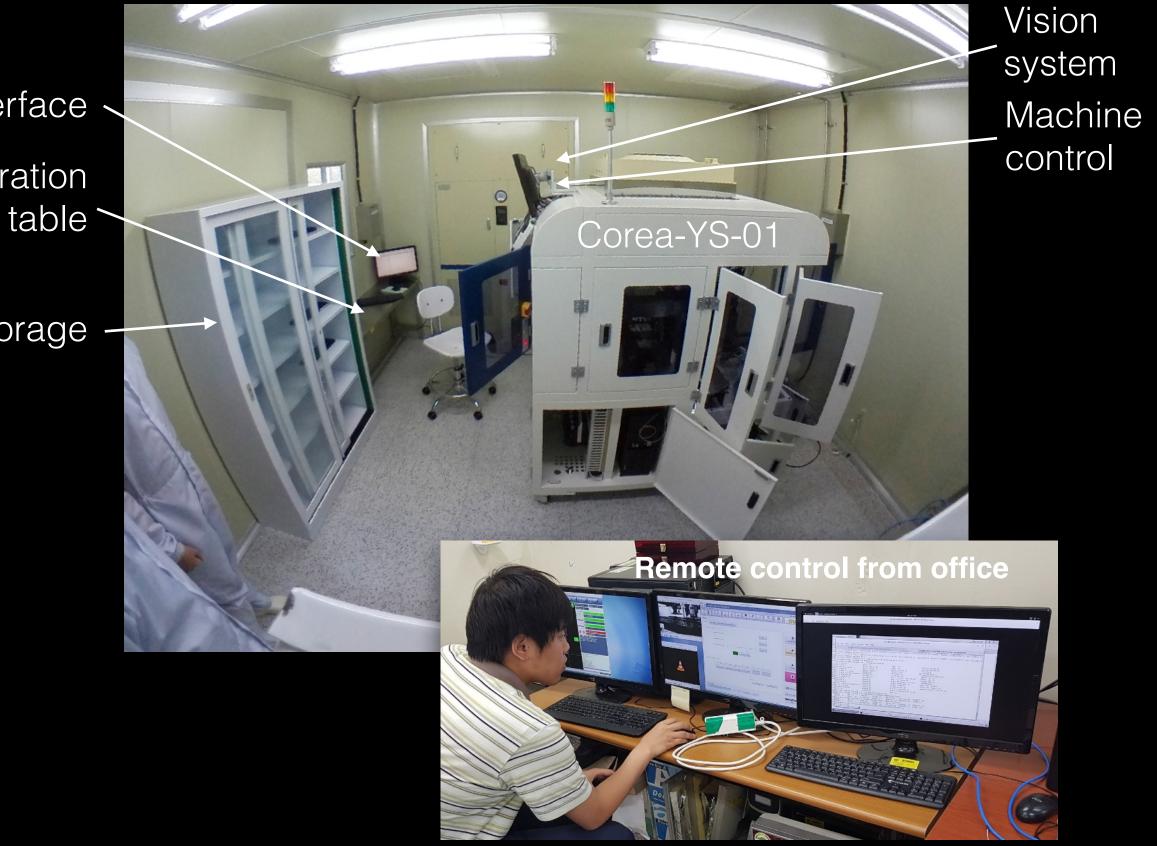


Database interface <

Tray prepa-ration

Chip storage

Yonse



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- Meetings: <u>https://indico.cern.ch/category/7312/</u>
- **Database:** <u>https://alucms.web.cern.ch</u> (website), \bullet https://alucmsapi.web.cern.ch/AlucmswebAPI.asmx (API)
- **EOS:** <u>https://cern.ch/alpide</u> \bullet
- Logbook: <u>https://alpide.cern.ch/logbook/</u>
- \bullet
- overleaf: https://www.overleaf.com/read/wkmkcrjqtfsg

Book keeping

TWiki: <u>https://twiki.cern.ch/twiki/bin/view/ALICE/ITSUpgradeProbeCard3</u>







Oct 2016

- Chip deliveries for machine commissioning
- Still using old foam trays

