LHCf:
new silicon read-out electronics

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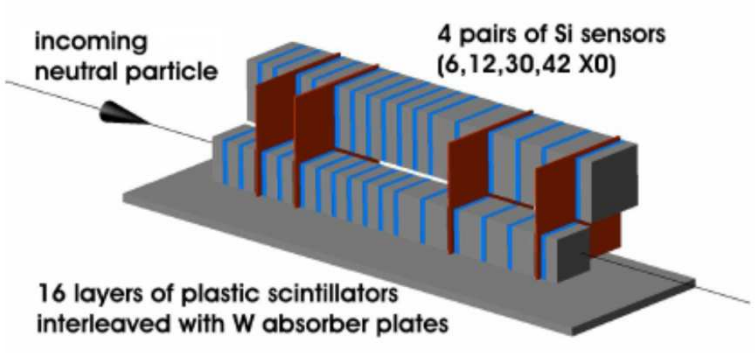
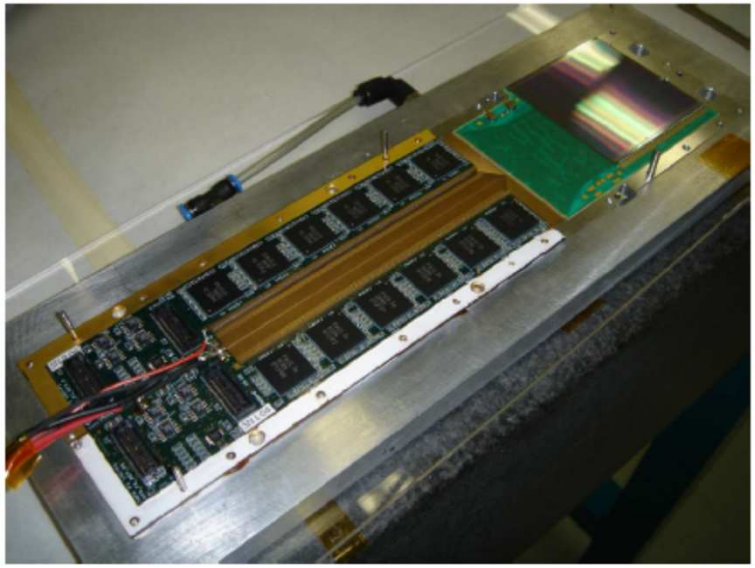
Summary

- Review of Arm2 silicon read-out electronics employed until now ("v1").
- Description of the new ("v2") read-out electronics.

LHCf Arm2 silicon detectors

Arm2 calorimeter: contains 4 pairs of Si microstrip sensor planes (1 pair = 1 Si detector module).

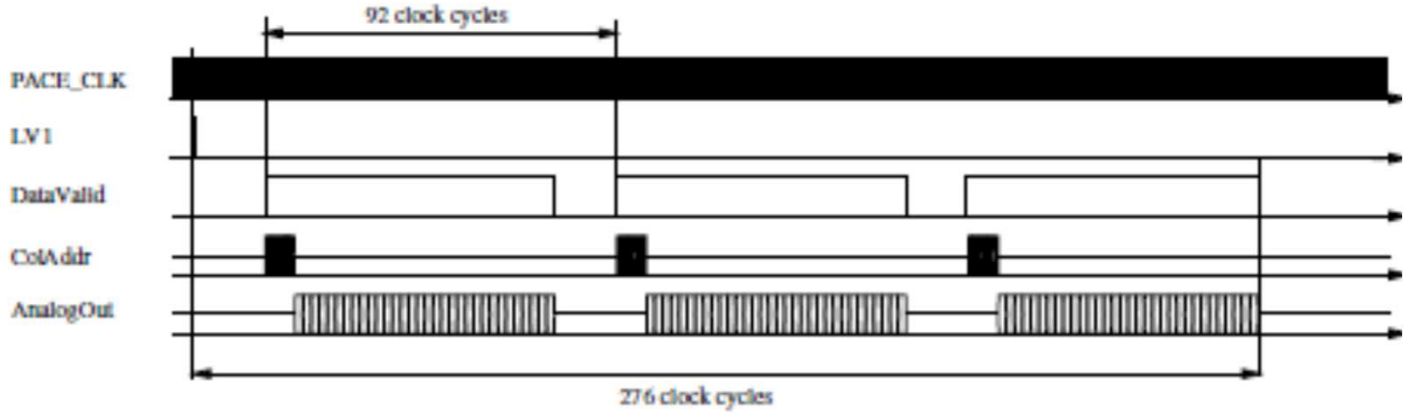




Top side of a Si detector module, showing one Si sensor plane and the corresponding 12 front-end PACE3 chips.

Si front-end chips

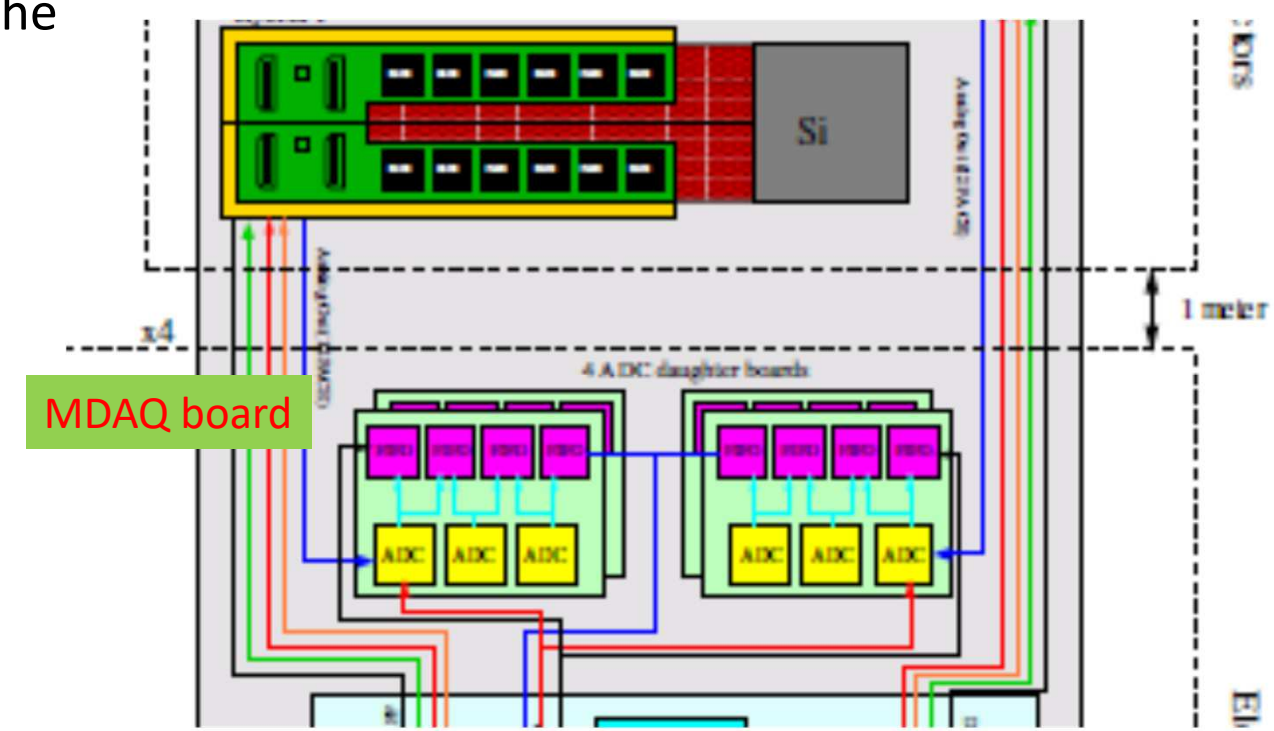
- The PACE3 chip features **32 read-out channels** with independent shaping circuit.
- The 32 shaped signals are continuosly sampled with LHC clock period (40.08 MHz frequency).
- Upon reception of L1 trigger (synchronous with LHC clock), PACE3 produces **3 analog data values per channel**, corresponding to 3 subsequent samplings.



- The latency and phase between L1 and selected samplings is set accordingly to the shaping time and line delays.

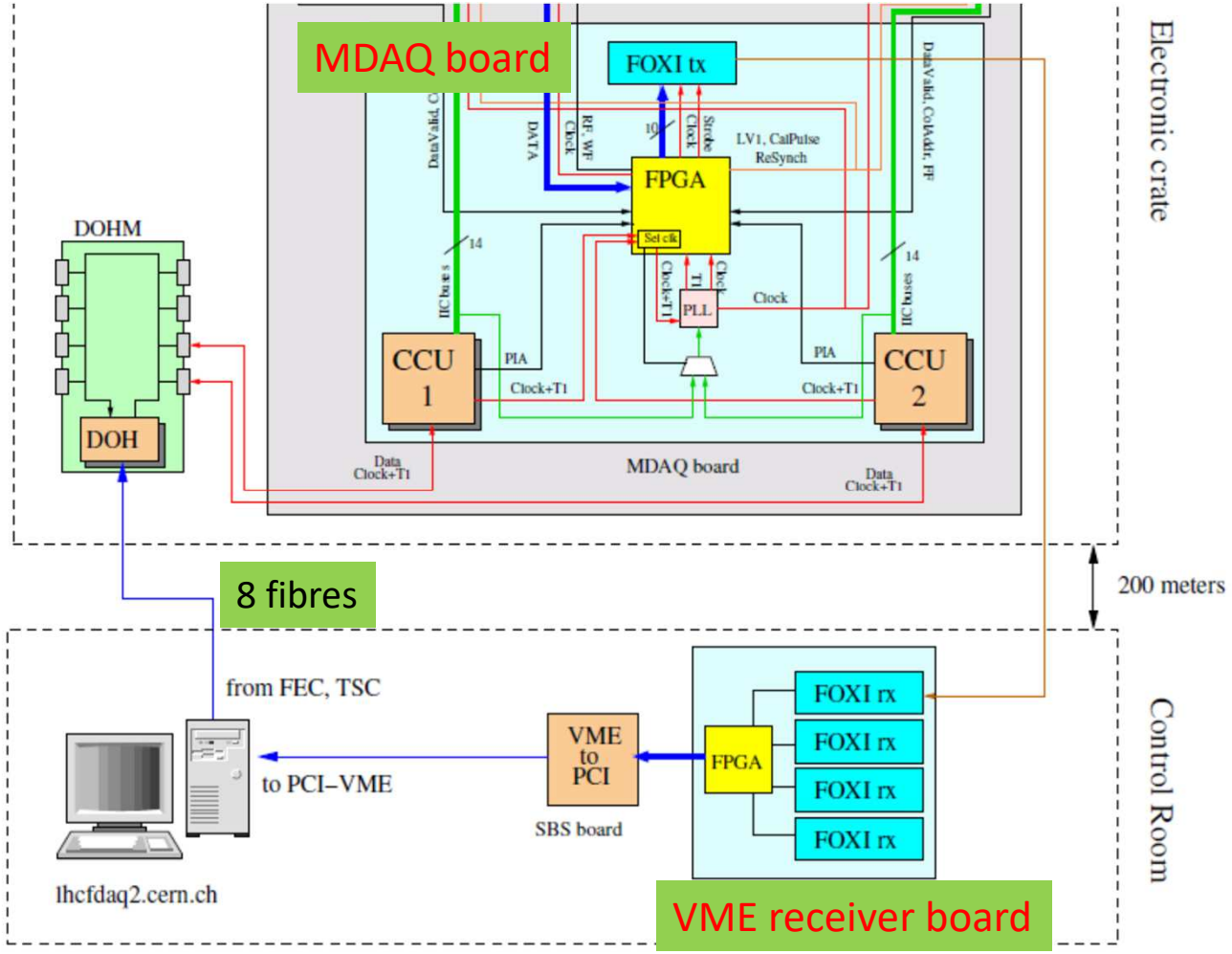
Si read-out v1: MDAQ boards

- Composed of **4 MDAQ boards** (one board for 2 Si planes) and a set of auxiliary boards.
- The MDAQ boards are installed in the "electronic crate" nearby the Arm2 detectors.
- The MDAQ board contains:
  - ADC's and FIFO's for digital conversion and temporary storage of PACE3 data;
  - FPGA with on-board logics.



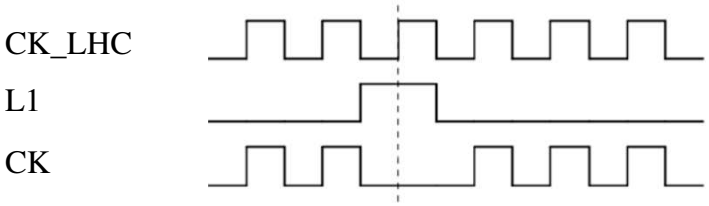
Si read-out v1: slow control

- **Slow control** is managed by the control PC located in the underground control room (USA15), 200 m apart from the detectors.
- Slow control employes a system of boards called **"control ring"** and originated from LHC CMS experiment:
  - FEC and TSC in the control PC;
  - DOH in the "electronic crate";
  - 2 CCU's (daughter boards) on each MDAQ board, with PIA interface with MDAQ logics;
  - 8 long-distance optical links (in+out CK/DATA pairs, with redundancy) between FEC and DOH;
  - local optical links between DOH and CCU's;
  - local I^2C links between CCU's and Si planes (PACE3 chips).

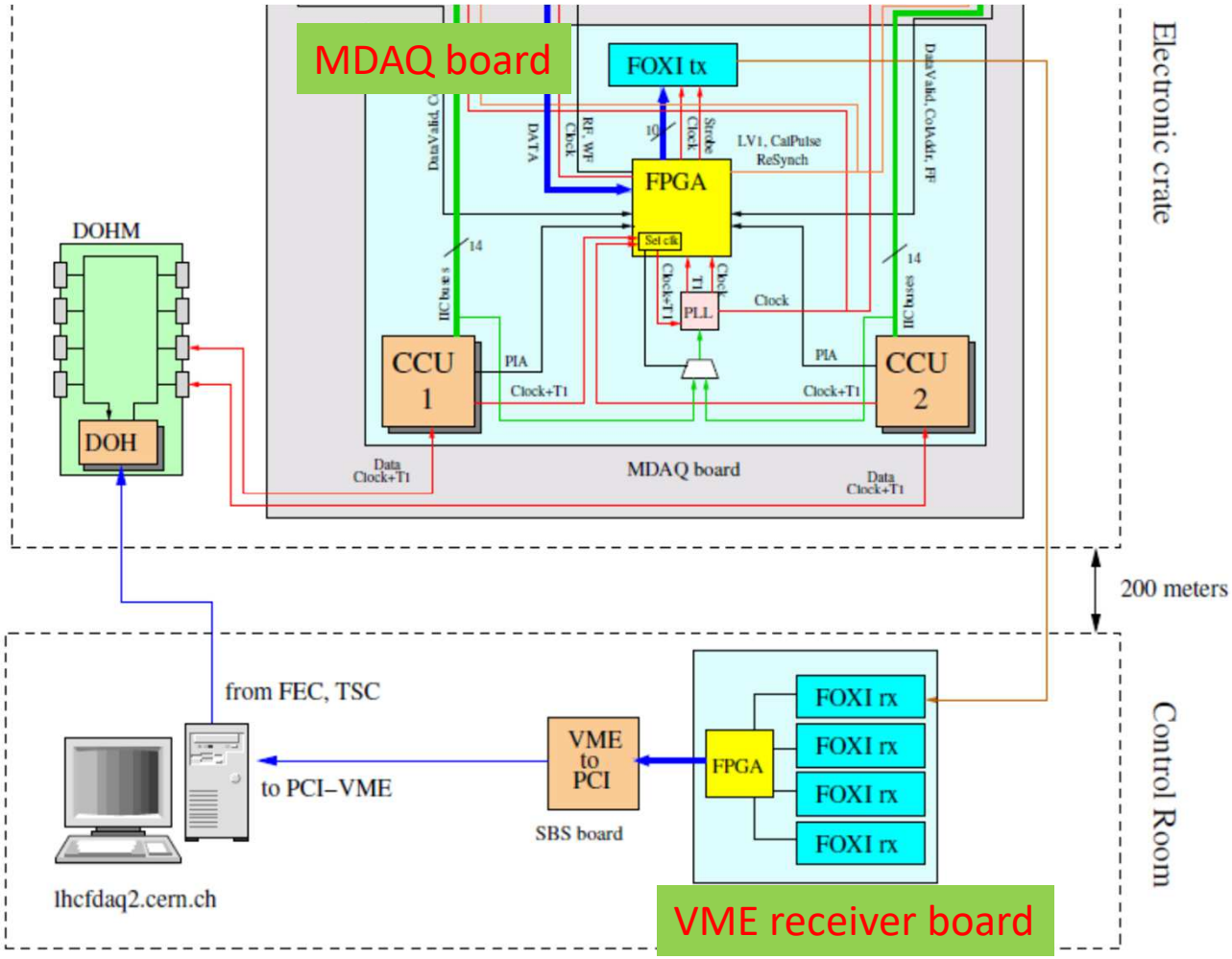


Si read-out v1: LHC clock and fast signals

- **LHC clock and synchronous fast signals** (L1 trigger, Cal, Resync) are distributed through the same DOH-CCU "control ring".
  - The fast signals are encoded as **missing clock cycles.**

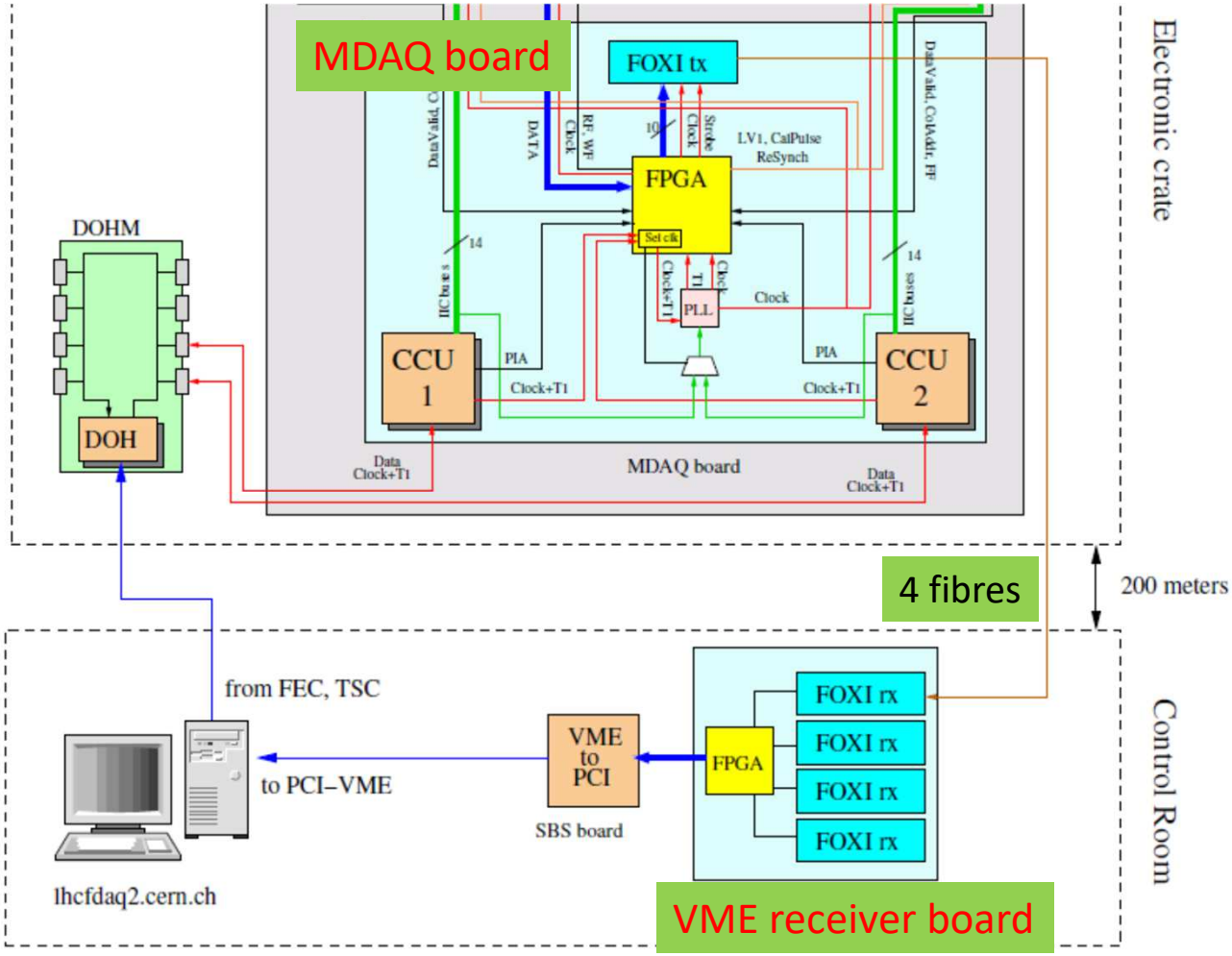


- The MDAQ boards distribute LHC clock and fast signals to the Si planes (PACE3 chips).



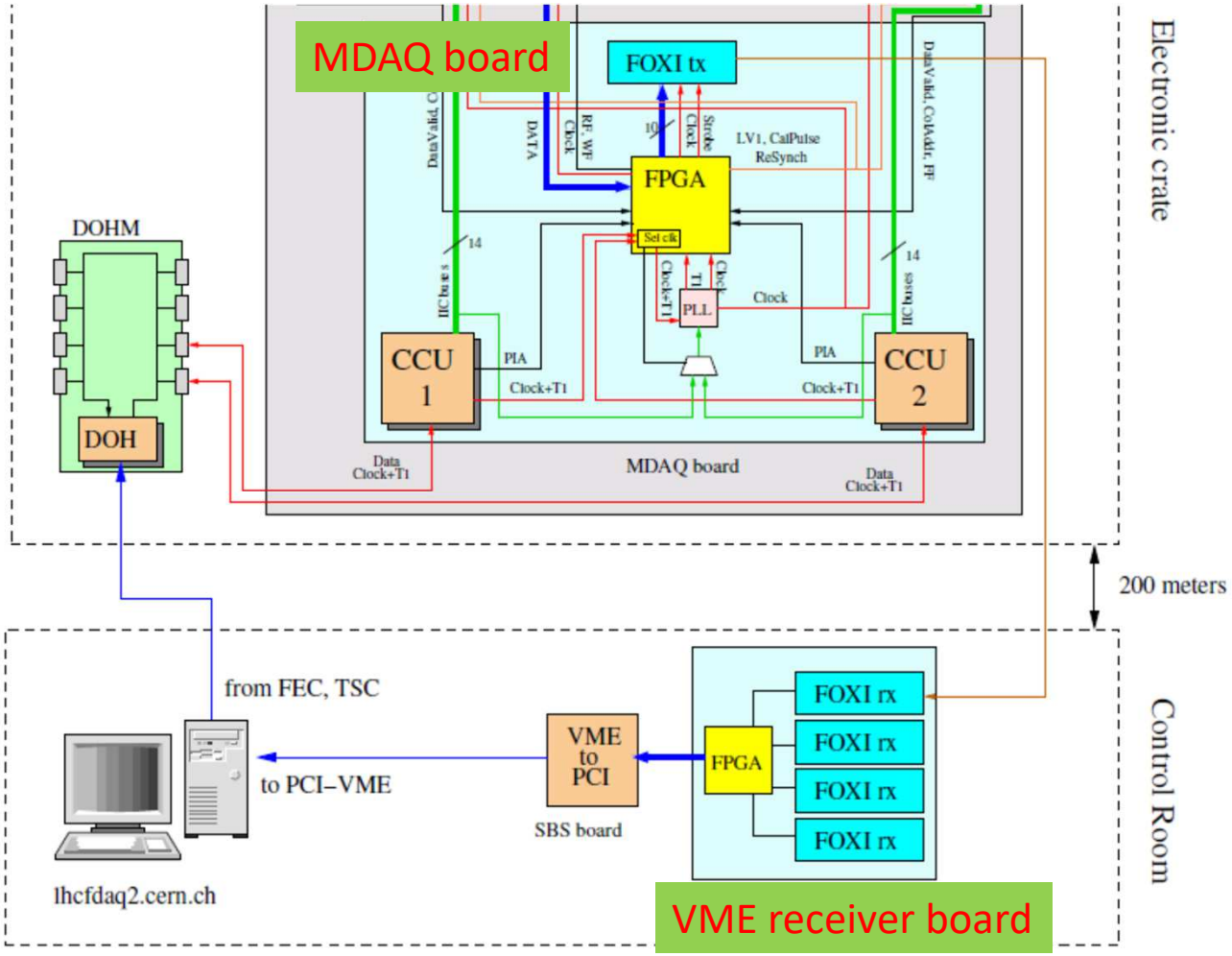
Si read-out v1: event data

- **Event data read-out** is automatically operated by MDAQ board upon reception of L1 trigger.
- Event data (28 kbit per MDAQ) are transmitted via optical link toward a custom **"VME receiver board"** in the control room.
  - The optical link is managed by AMD FOXIchips at **100 Mbps peek speed**.
- Each MDAQ board transmits data simultaneously with others.
- **Data transmission lasts 373 µs** since L1 trigger.



Si read-out v1: event data

- The VME system is interfaced with the control PC via SBS board.
- Event data transfer from the "VME receiver board" to the storage unit starts after L1, with a suitable delay to allow internal FIFO to be properly filled with event data.
- The whole event data packet (112 kbit) is then transferred **via VME bus** in 620 μs, at **184 Mbps effective speed.**



Description of the new ("v2") silicon read-out electronics.

Si read-out v2: motivations

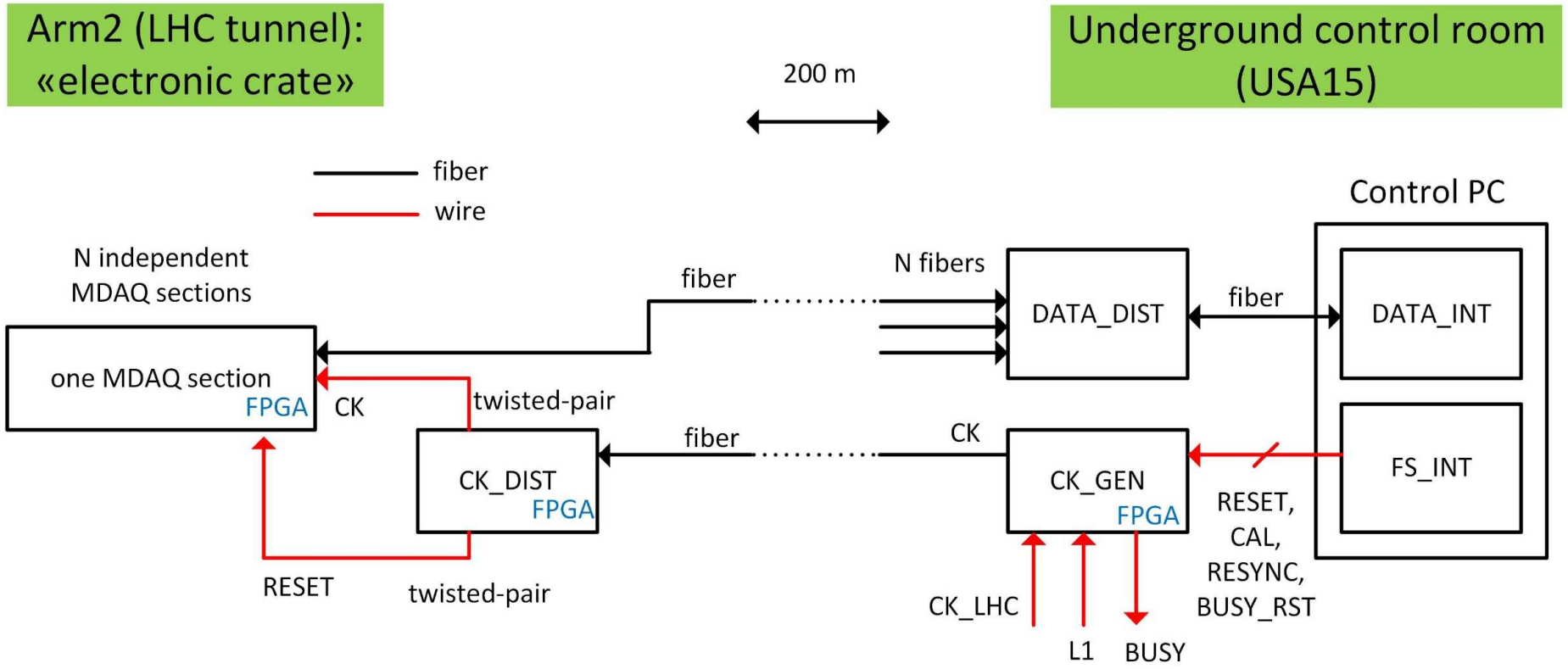
Motivations to develop new read-out electronics.

- **Substitute aged electronics**: the employed electronics is aged (> 10 years) with high irradiation sustained by the boards in the tunnel area.
- **Speed-up the read-out**, thus reducing contribution to overall dead-time.
- **Simplify and optimize the slow control system** (instead of adapting the complex CMS "control ring" architecture as in v1).
- **Employ standard and modern commercial devices** (instead of custom and old ones).

Notes.

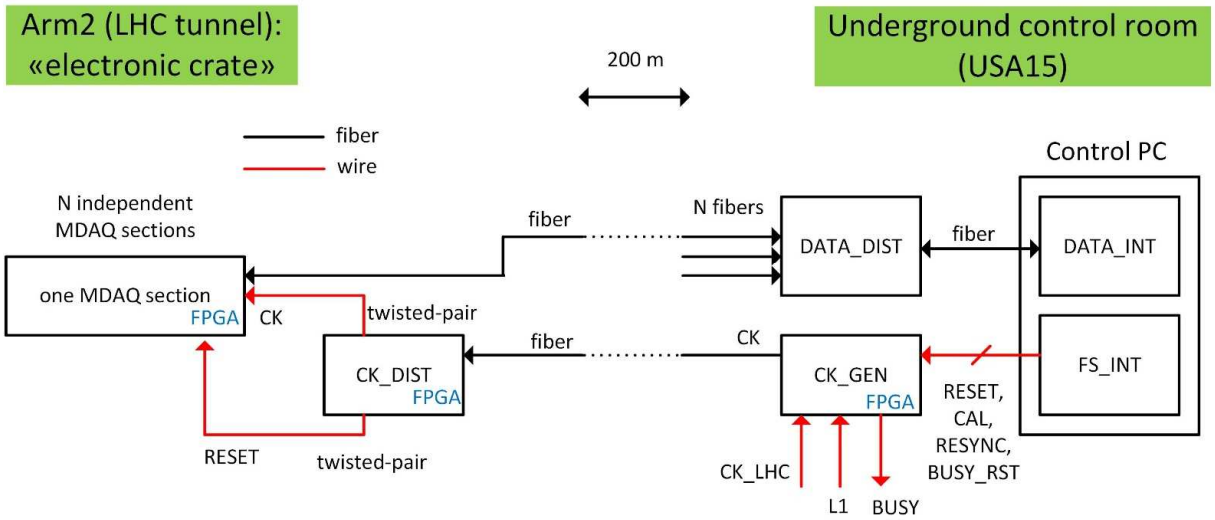
- The current Si detector modules will be retained (the original ones have been already replaced).
- The current power system will be retained, possibly increasing the output power if necessary, and substituting the power board in the "electronic crate" with a new identical one.

Si read-out v2: overall scheme



Si read-out v2: event data and slow control

1. **Event data transmission** will be operated with **standard 1 Gbps Ethernet protocol** (instead of FOXIchip protocol with 100 Mbps peak speed).
   - **The dead time contribution is thus reduced by a factor ~10.**
   - The custom "VME receiver board" on VME system is replaced by:
     - a standard **optical 1 Gbps Ethernet PCI express board,** DATA_INT;
     - a standard **optical 1 Gbps Ethernet switch,** DATA_DIST, directly interfaced with the control PC.

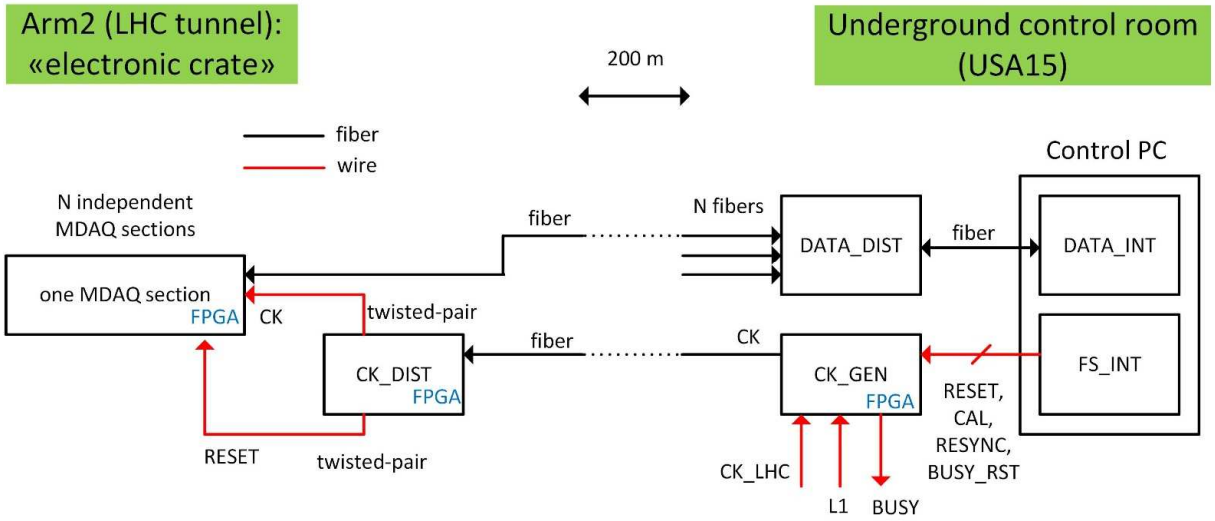


2. The **slow control system** (FEC, TSC, DOH and CCU boards) will be replaced by using the same (bidirectional) link.

Si read-out v2: LHC clock and fast signals

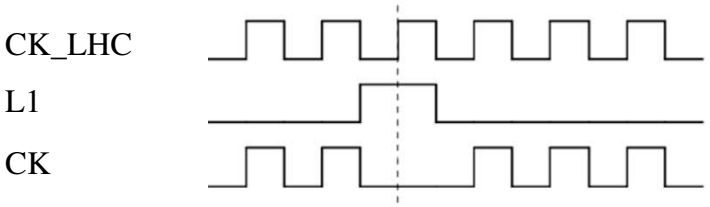
3. **Fast signal** generation and distribution will be implemented by a mix of standard and custom (simple) electronics:

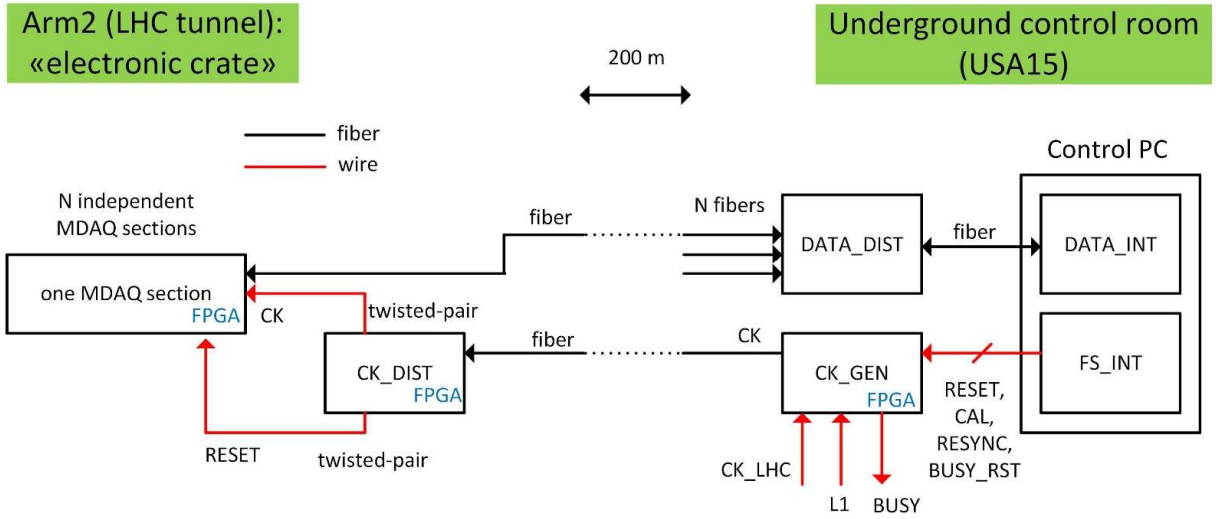
- **FS_INT**: standard PCI express board inside the control PC, with TTL output lines (RESET, CAL etc.);
- **CK_GEN**: custom board in the control room;
- single dedicated optical link;
- **CK_DIST**: custom board in the "electronic crate" nearby Arm2 detectors.



Si read-out v2: LHC clock and fast signals

- **CK_GEN**
  - As in v1, the fast signals (e.g. L1 trigger) are encoded as missing clock cycles, through internal PLL circuit.

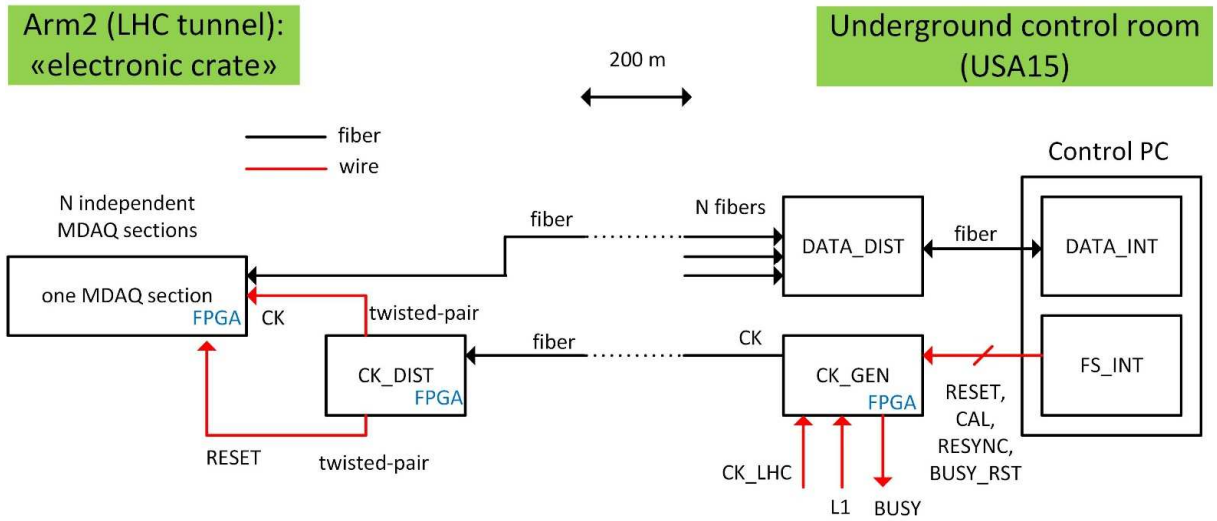




  - The BUSY output is set as soon as L1 pulse is received; it is then reset by the control PC (via BUSY_RST line).

Si read-out v2: LHC clock and fast signals

- **CK_DIST**
  - Dedicated outputs (twisted pair lines) for each MDAQ section.
    - CK (copy of input signal: LHC clock with encoded fast signals).
    - RESET decoded from input CK.
      New signal: allows for initialization in case of mulfunctioning
      (in v1, this was performed - only for a subset of cases - by DOH).

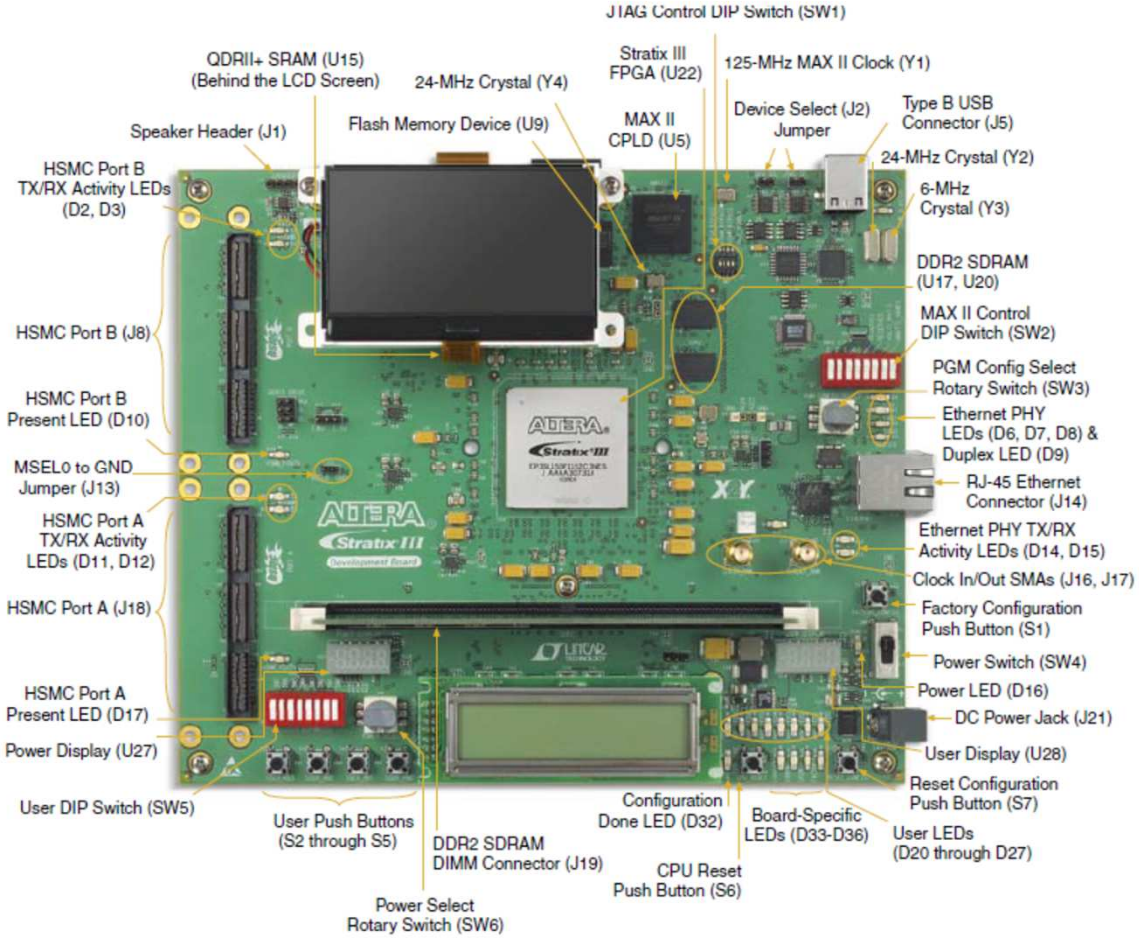


Si read-out v2: MDAQ board

4. The MDAQ board design will be simplified.
   - **Event data transmission and slow control** will be managed through **1 Gbps Ethernet** protocol, by a standard logic module implemented in the on-board FPGA.
   - **FOXIchip transmitters and CCU's are not used anymore.**
   - Slow control I^2C interface between MDAQ and PACE3 chips will be integrated in the FPGA (instead of using CCU's).
   - **Decoding of fast signals will be integrated in the FPGA** through internal PLL (instead of using the external CMS TPLL ASIC as in v1).
- If possible, the number of independent MDAQ sections will be set to 8 (one per Si plane), instead of 4 as in v1.
   - Increased segmentation, to balance loss the redundancy from "control ring" (v1).

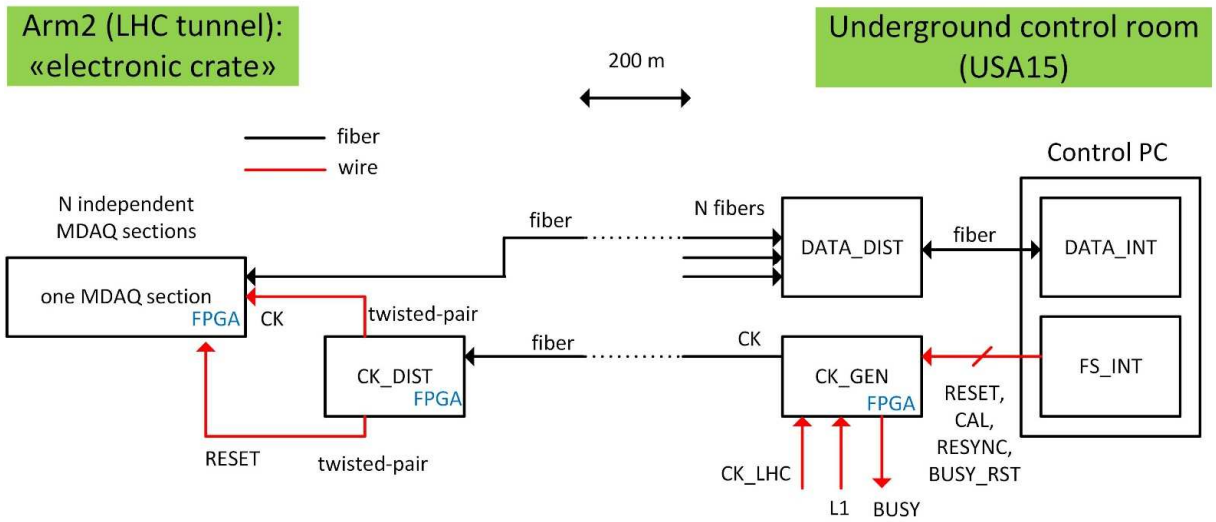
Si read-out v2: MDAQ board

- The new MDAQ board will contain a modern FPGA, **Intel/Altera Stratix III** (instead of Cyclone I of v1).
- Purchased **Stratix III development kit.**
  - Integrates 1 Gbps Ethernet.
  - Optical adapter module can be installed on the Ethernet RJ45 connector.
  - **This allows early testing of 1 Gbps Ethernet in our system.**



Si read-out v2: hardware development plan

- Selection and purchase of standard commercial boards (DATA_INT, DATA_DIST, FS_INT).
- Implementation of MDAQ board and CK_GEN functionalities on Stratix III development kit.
- **Assembly and test of system prototype with development kit** (no CK_DIST board).
  - 1 Gbps Ethernet for slow control and event data.
  - I^2C interface toward Si detector module.
  - LHC clock and fast signals.
- Implementation and test of real full system with MDAQ, CK_DIST, CK_GEN boards.
  - CK_DIST and CK_GEN are much simpler boards than MDAQ.



Si read-out v2: software development plan

- Modify the control PC software:
  - to manage slow control via **standard PCI Express board** DATA_INT, instead of custom FEC board;
  - to manage event data via DATA_INT instead of VME system (same as above!);
  - to generate fast signals via **standard PCI Express board** FS_INT, instead of custom FEC board (simple task).
- Overall, **the software structure will be simplified** with respect to v1.

Conclusions

- We presented the new read-out electronics for LHCf Arm2 silicon detectors.
- The new read-out will be **faster and simpler** than the previous one.
- It will employ a mix of:
  - standard and modern commercial devices;
  - custom electronics, optimized for this application.