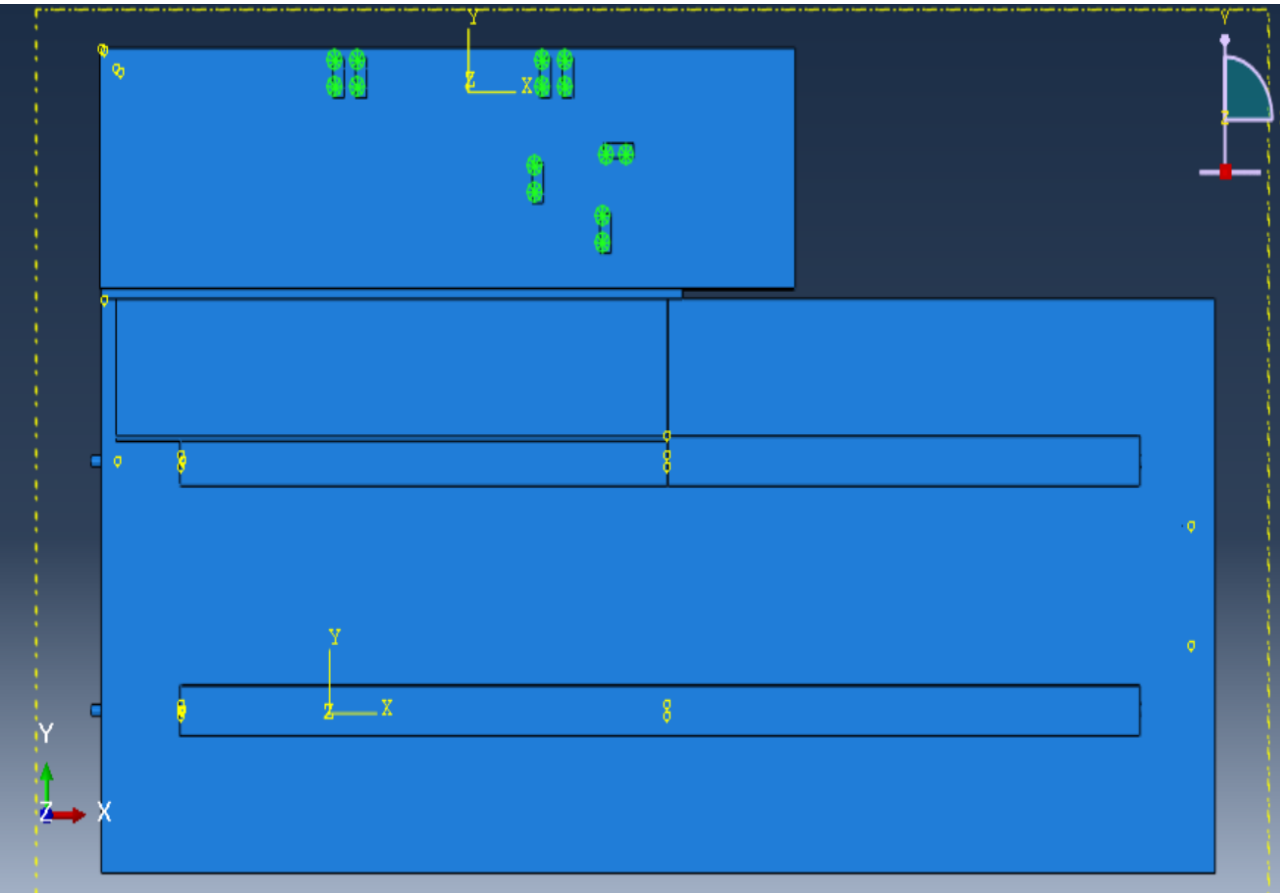


# Thermal FEA Update

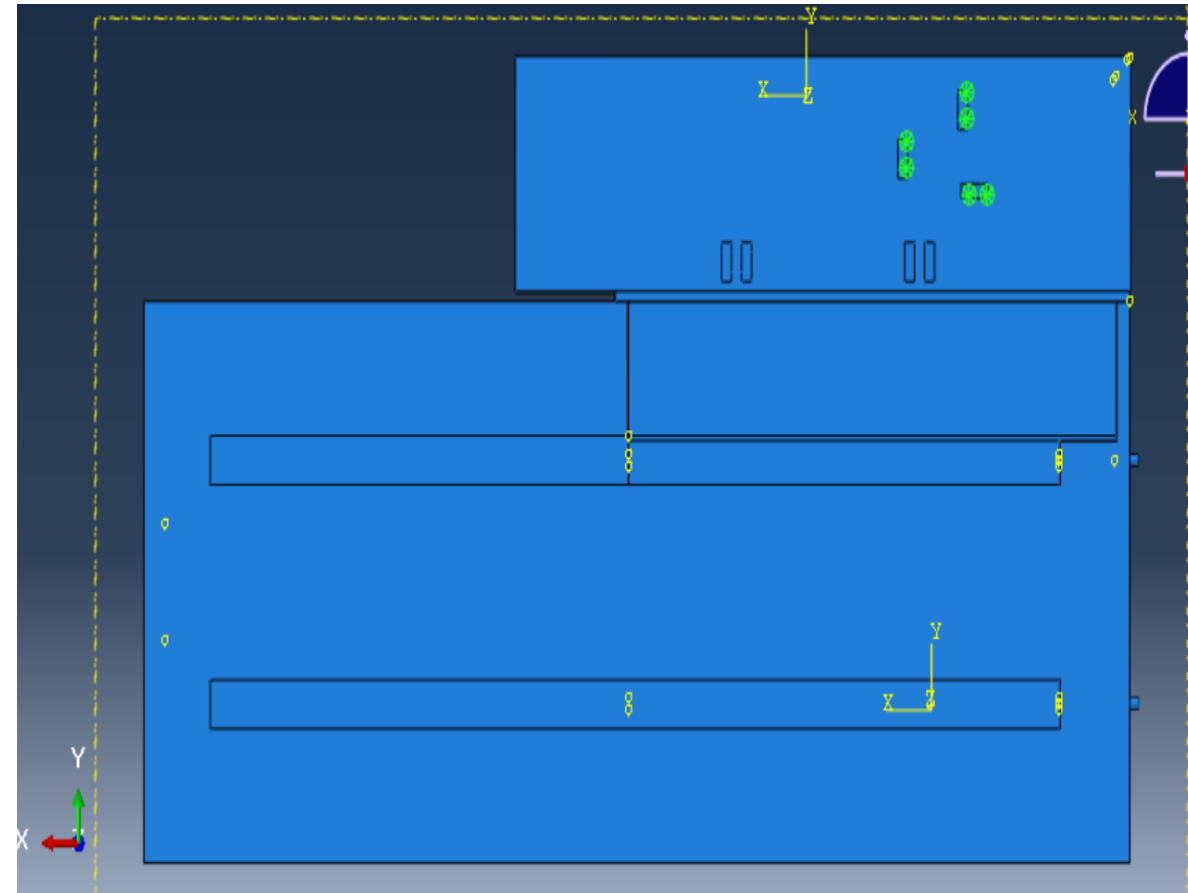
2018/11/15

Shuaiyan

# Mini Stave Model

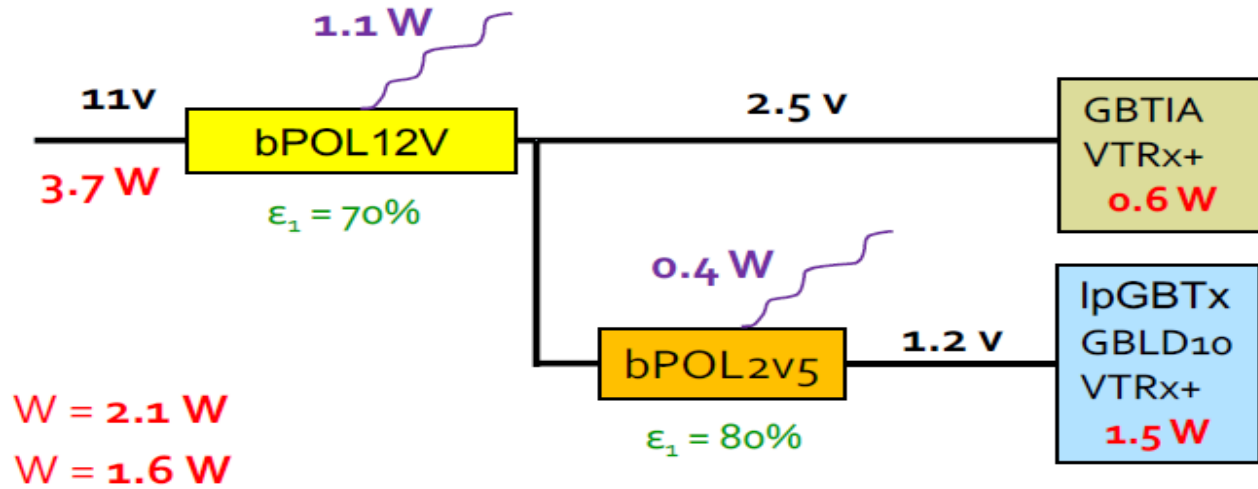


Master

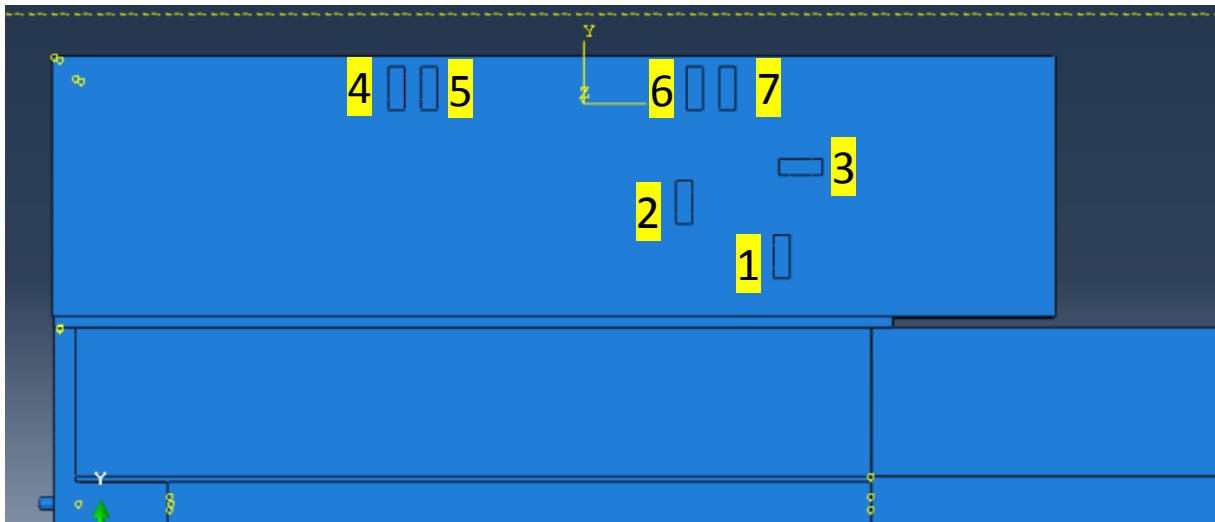


Slave

# Power dissipation estimate



PCB power distribution diagram made by Mogens Dam



Dummy PCB model

EoS	Voltage	Current (A)
IpGBT	1.2	0.625
GBTIA	2.5	5.30E-02
IpGBLD	2.5	1.80E-02
IpGBLD	1.2	9.50E-03 (per channel)

Voltage/current estimates for chips on PCB (two channels of IpGBLD @1.2V)

resister area  $3 \times 8\text{ mm}^2$  (with soldering area)

Power dissipation calculated by Graham:

R1 & R2 simulates IpGBTx , each gives about

$$\frac{0.75}{24} = 0.03125\text{ W/mm}^2$$

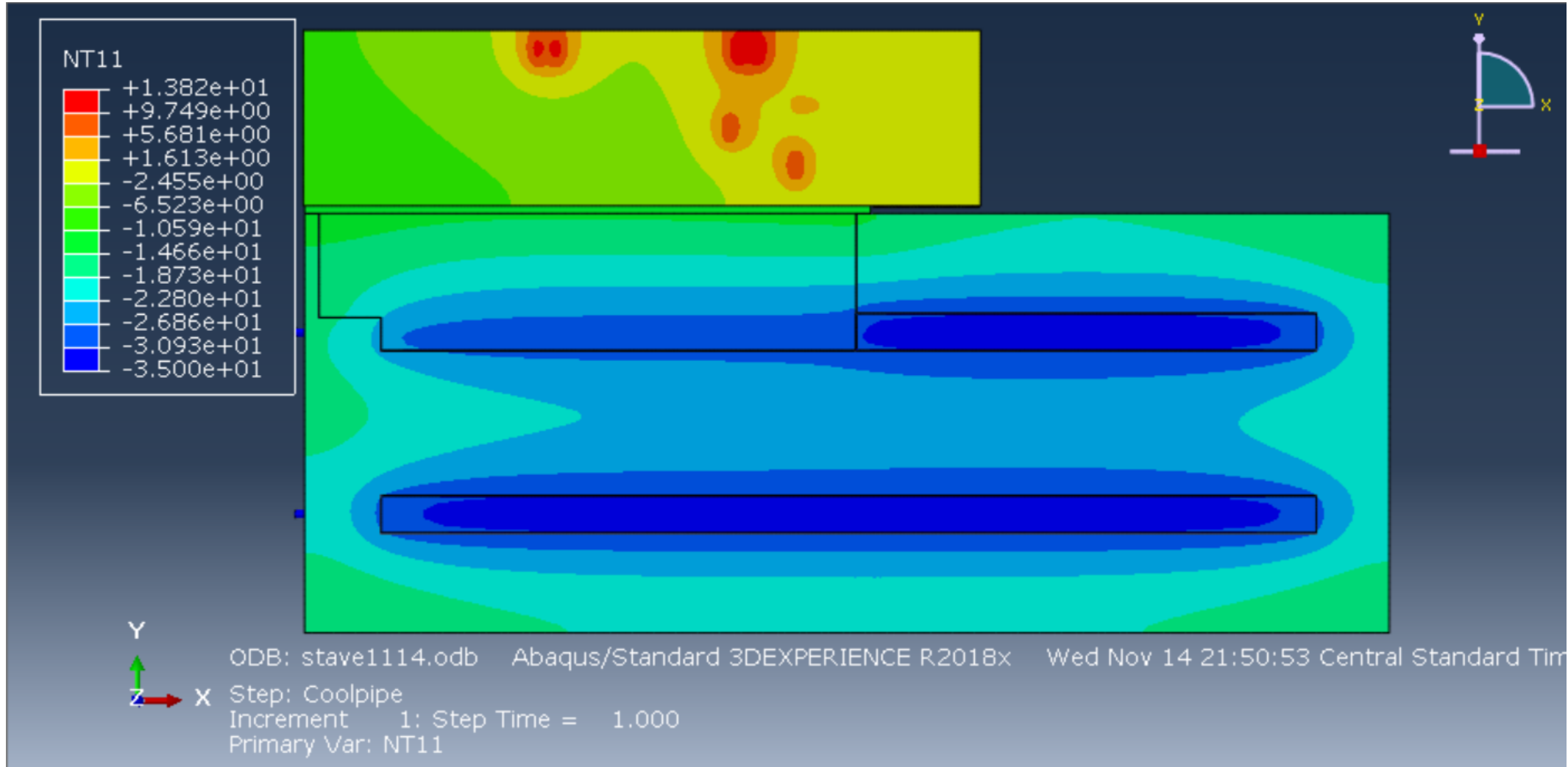
R3 simulates VTRx  $\frac{0.2}{24} = 0.00833\text{ W/mm}^2$

R4 & R5 simulates Master DCDC

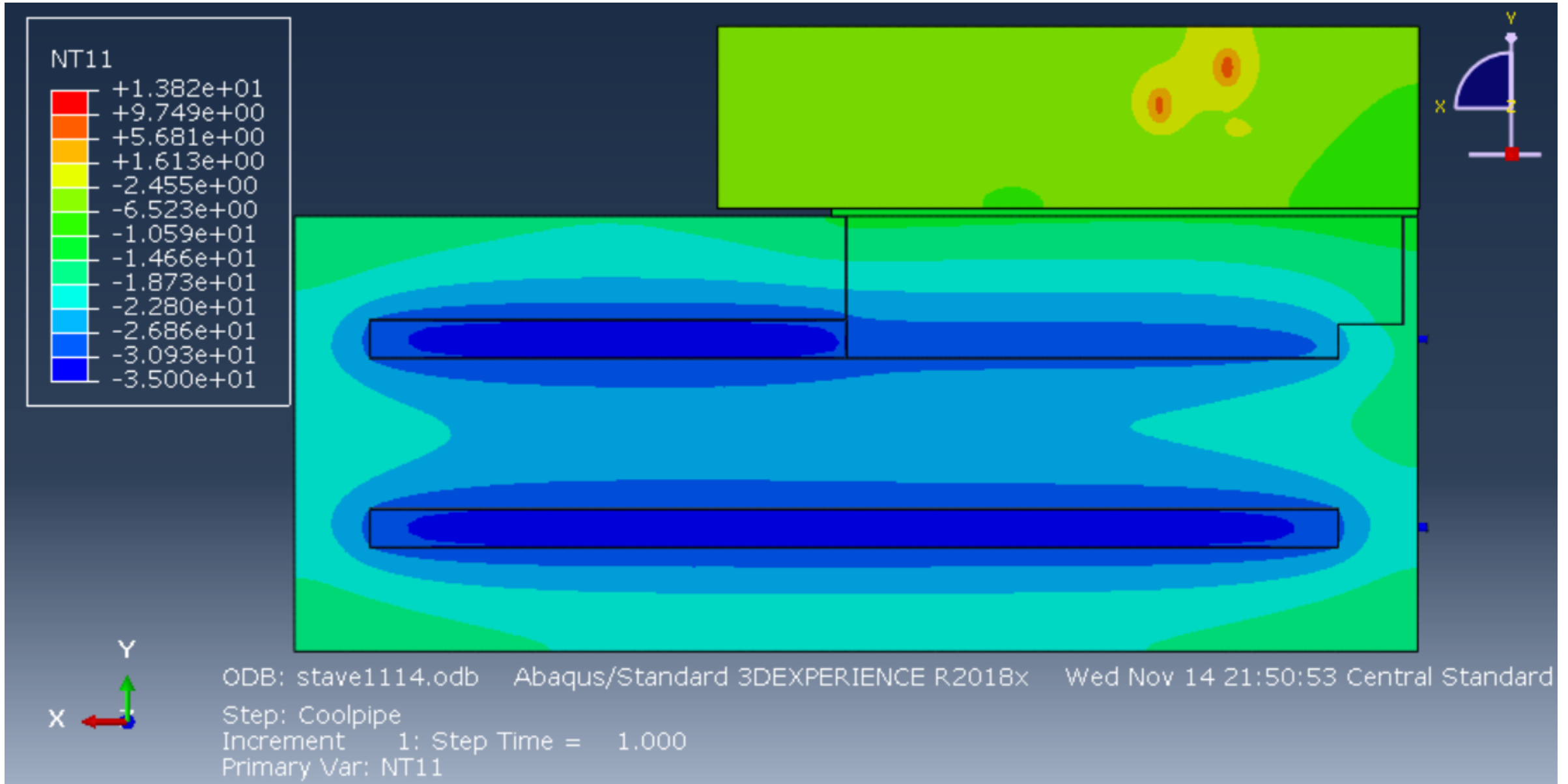
R6 & R7 simulates Slave DCDC

Each gives about  $\frac{0.635}{24} = 0.02646\text{ W/mm}^2$

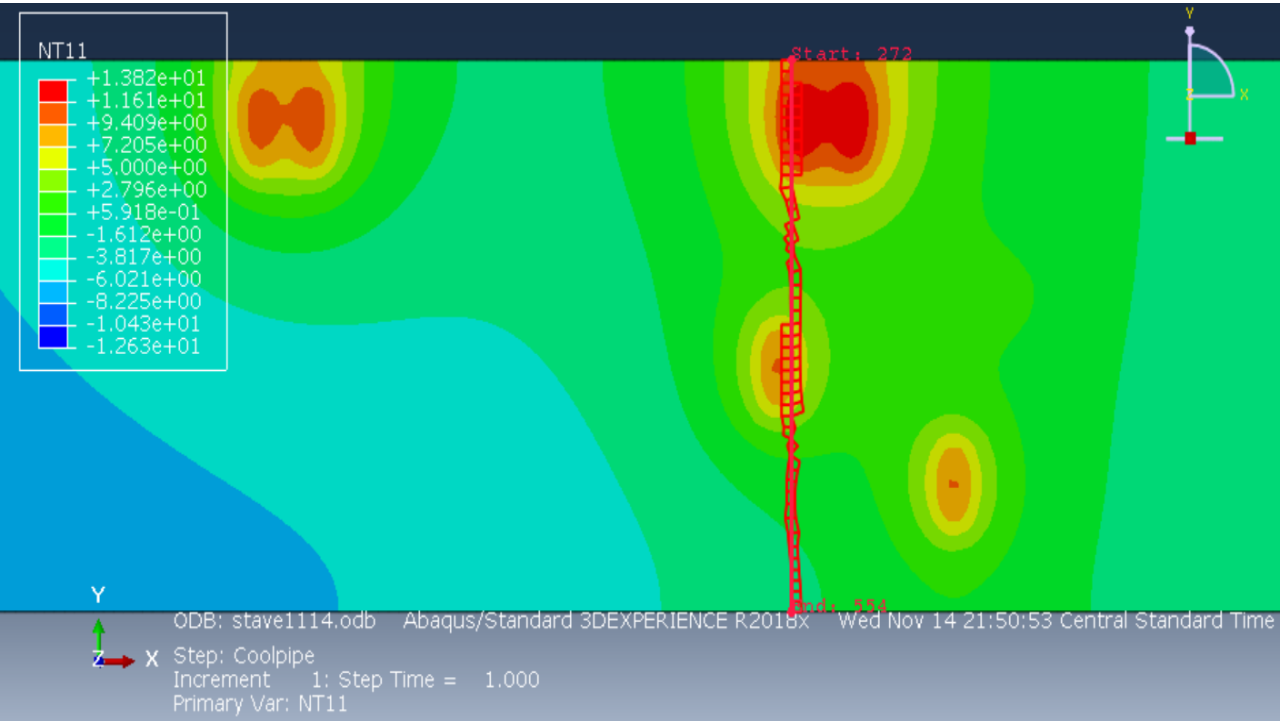
# Stave temperature distribution (master)



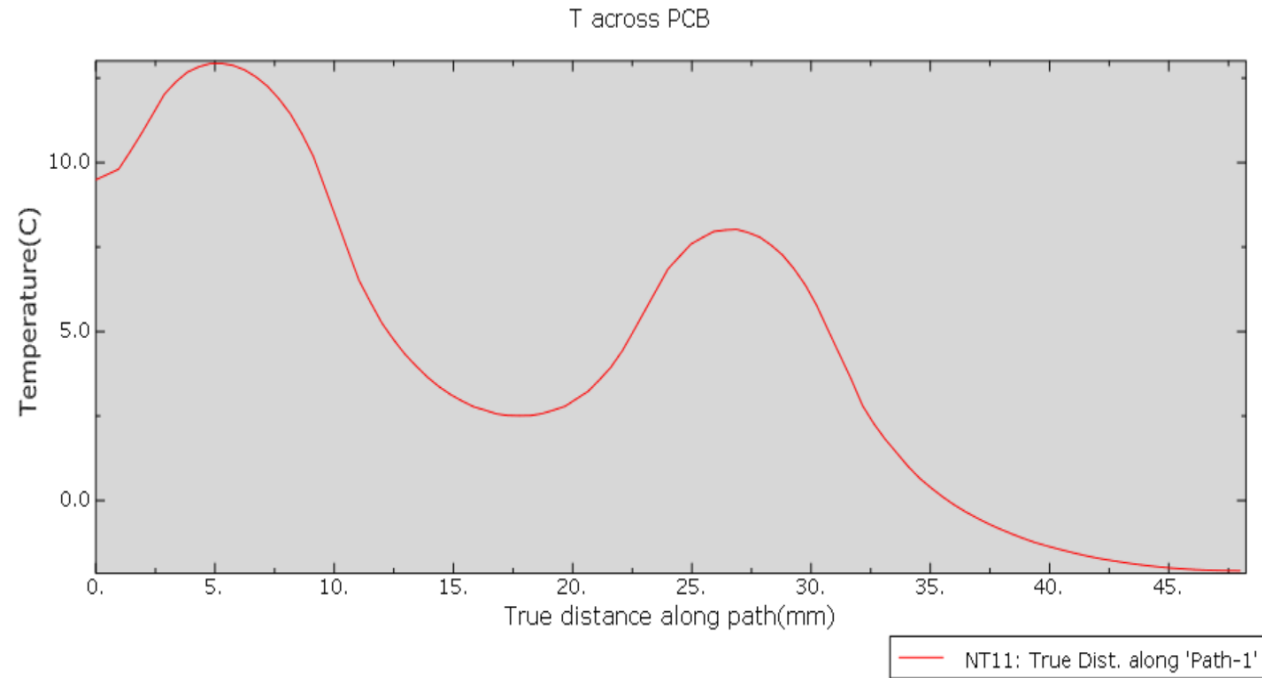
# Stave temperature distribution (slave)



# Temperature distribution across master PCB

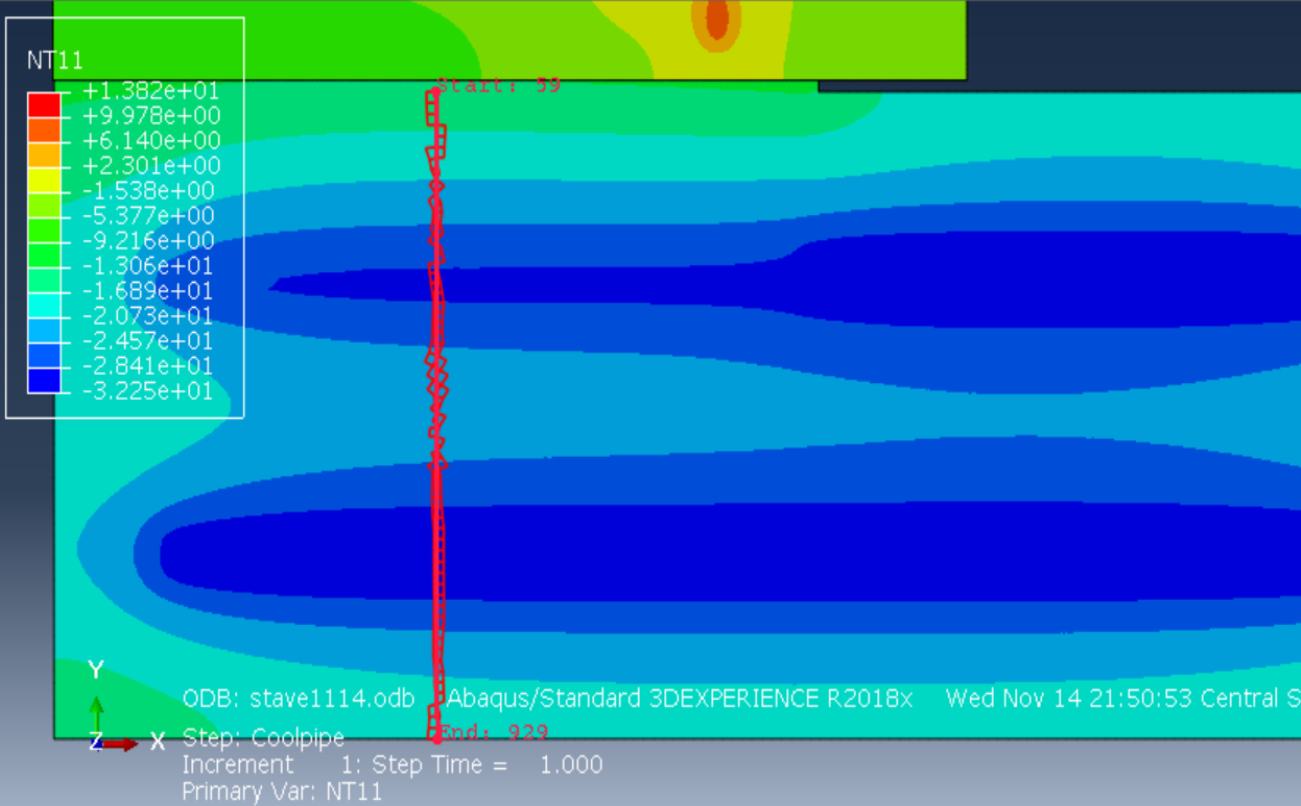


Path across master PCB

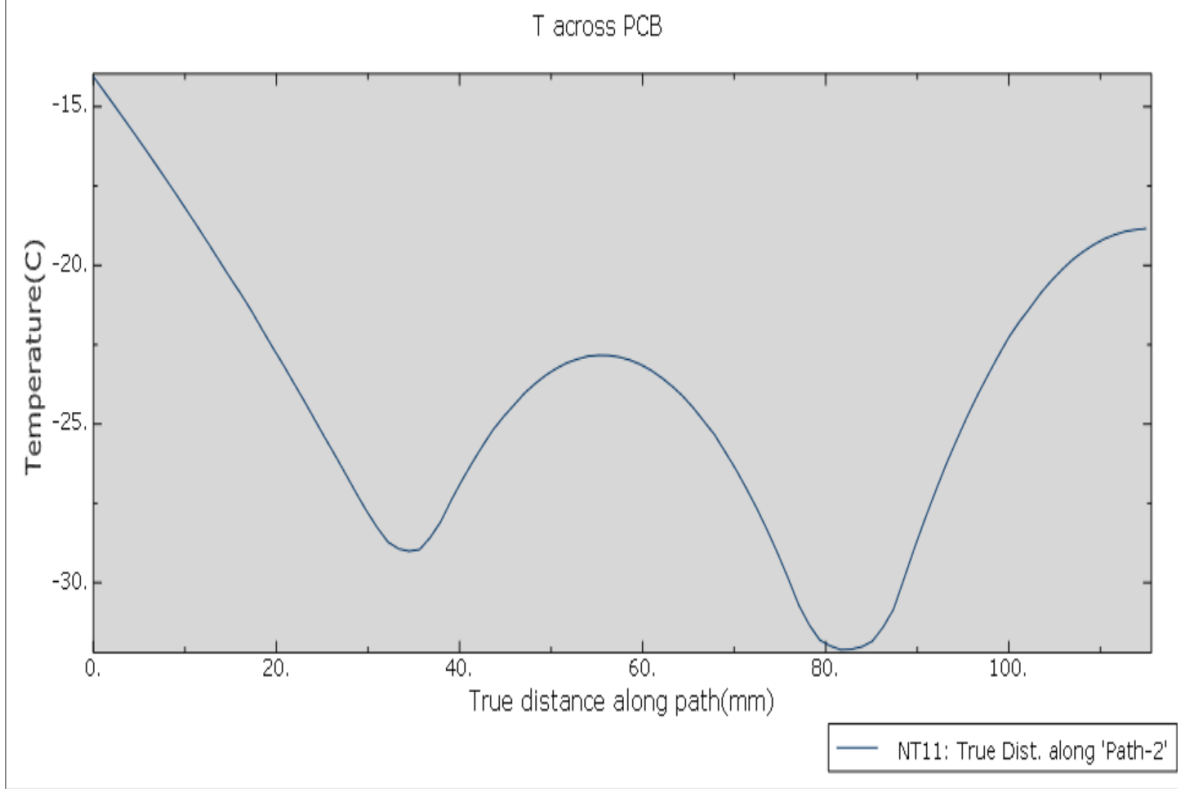


Temperature across master PCB

# Temperature distribution across stave (master)



Path across stave



Temperature across stave