VMM ASIC

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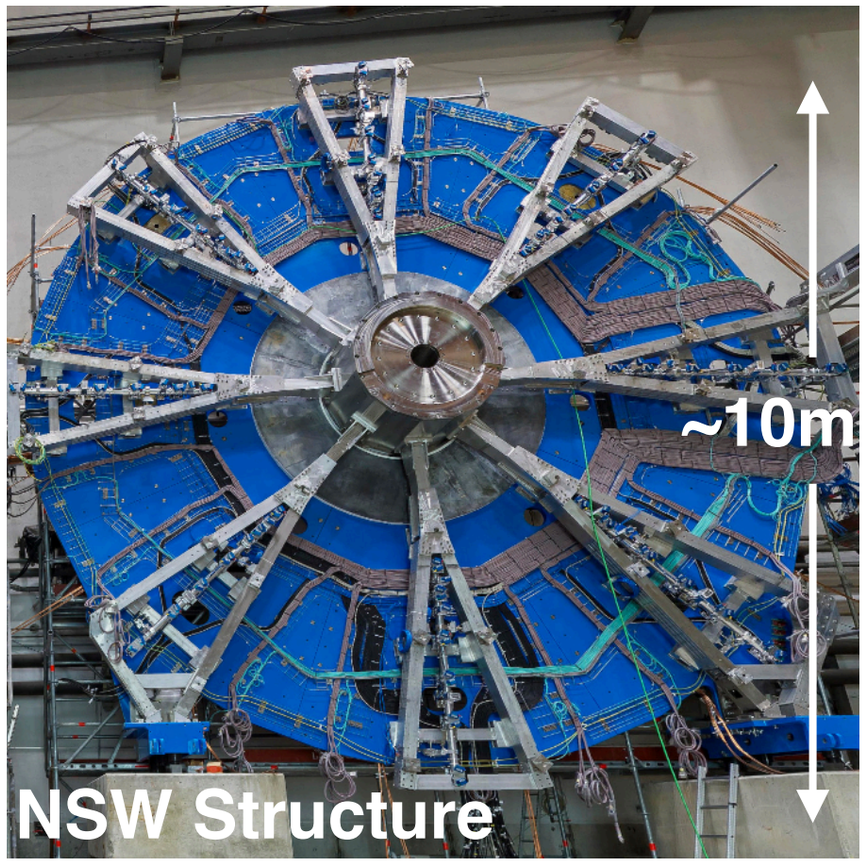
Introduction & talk outline

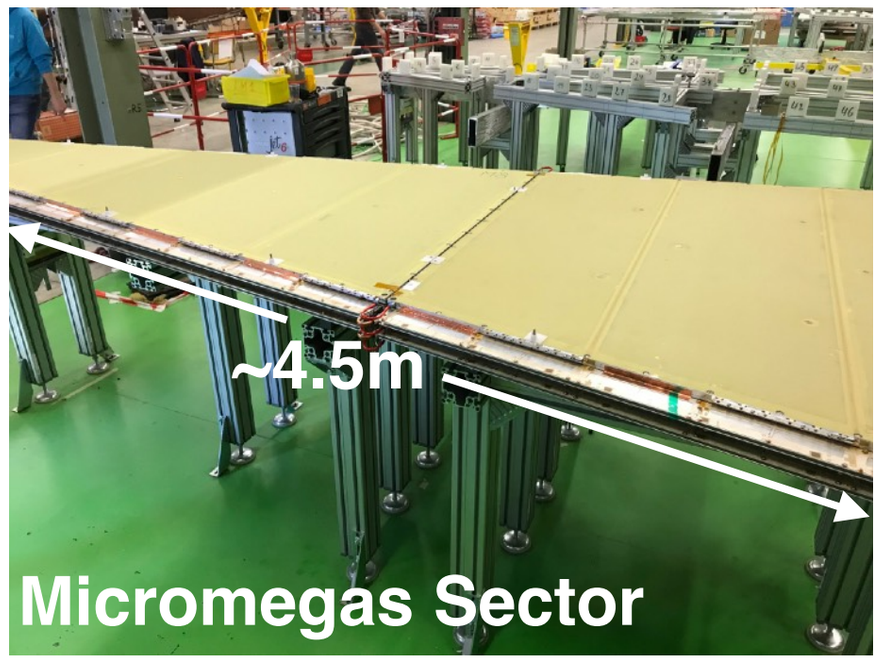
✳**VMM** development was performed in the context of the **ATLAS New Small Wheel Upgrade**

- Two detector technologies, Resistive Micromegas & sTGC - **Largest MPGD development !**
- Highly complex upgrade, **2.4 M channels**

✳Included in that talk:

- **VMM evolution** and the **production version**
- Functionality, **architecture** and readout
- **Performance** highlights
  - Bench measurements
  - Resistive Micromegas test beams
- Integration **highlights** on high channel density Micromegas detectors
- **Production**, reticle layout of the **wafer**
- Closing **remarks**

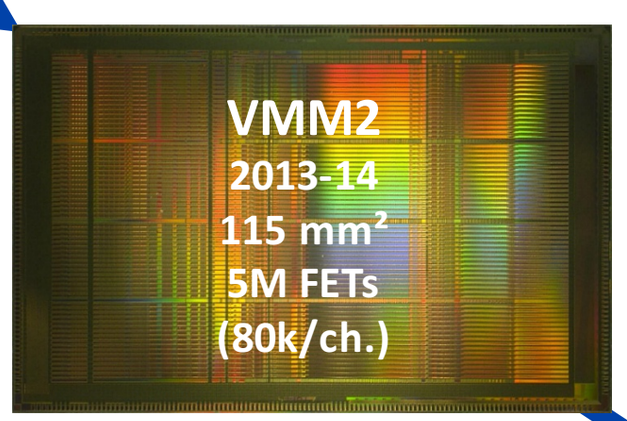




The VMM front-end ASIC - **Evolution**

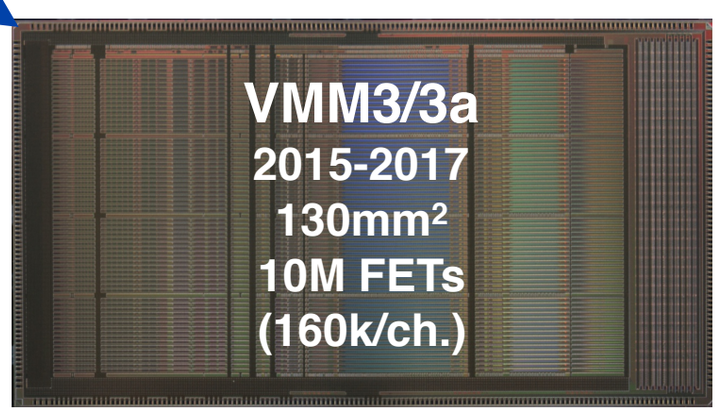
- **Mixed-signal**
- 2-phase readout with external ADC
- **peak** and **timing** information
- neighbouring readout
- sub-hysteresis **discrimination**
- few timing outputs

- Mixed-signal
- **Continuous** readout
- Current-output peak detector
- **Increased** range of **gains**
- **Three ADCs** per channel
- FIFOs, **serialised data with DDR**



- Serialised ART with DDR
- Additional timing modes
- **64 timing outputs**
- Additional functions and fixes

- **LVL0 pipeline** and buffering for ATLAS
- **SEU-tolerant logic**
- **Revised front-end** for high charge and capacitance (2nF, 50pC, fast recovery)
- SLVS signals
- Reset controls
- **Timing at threshold**
- Timing ramp optimisation
- Ion **tail suppressor** (fast recovery)
- Int. Pulser range extension
- ART synchronisation to BC clock
- additional functions and fixes
- **VMM3a fixed open bugs** from VMM3 and introduce some stability fixes on the ADCs and Front-end

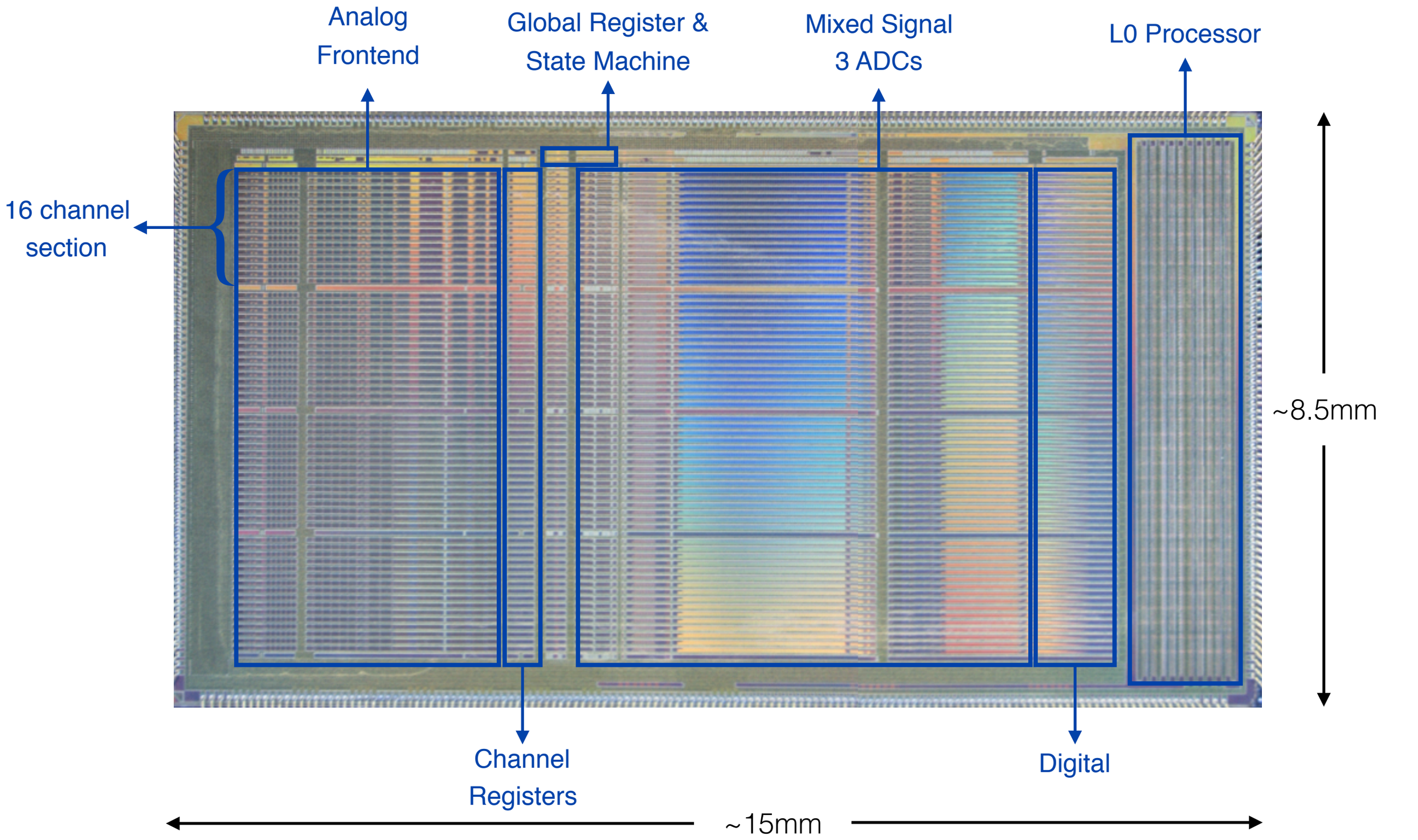


VMM3a - Production Version !

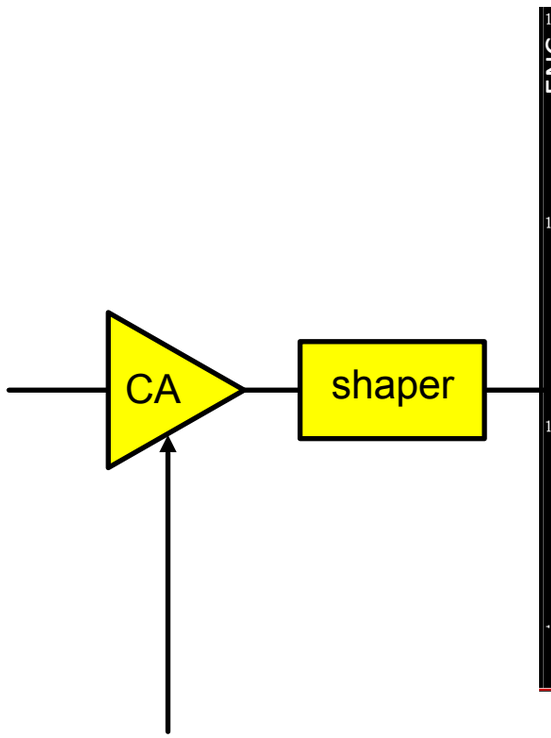
- ***The VMM was designed at BNL in collaboration with IFIN-HH***
- ***It is fabricated in the 130nm Global Foundries 8RF-DM process (former IBM 8RF-DM)***

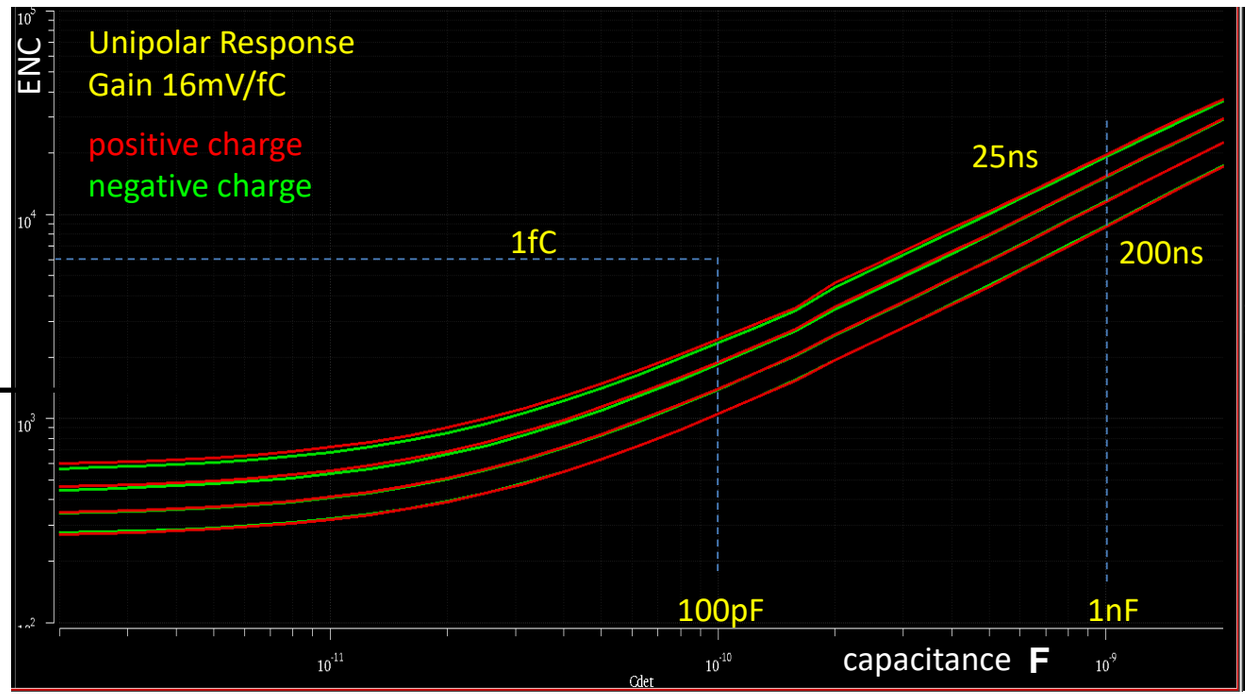
An actual photo of the ASIC

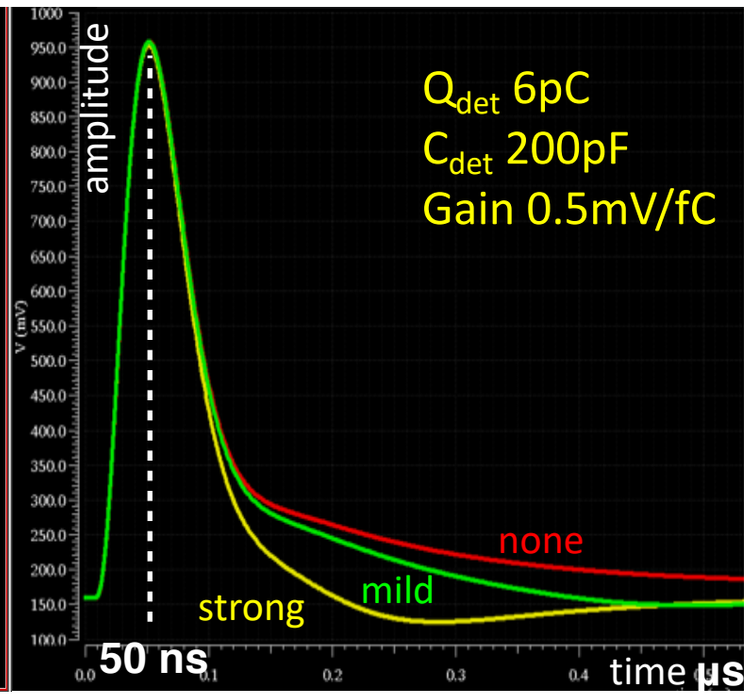
- The ASIC features **64 channels** that extend along the size of the die. At the end the L0 section (explained in later slides) is separated to isolate the noise from the digital activity



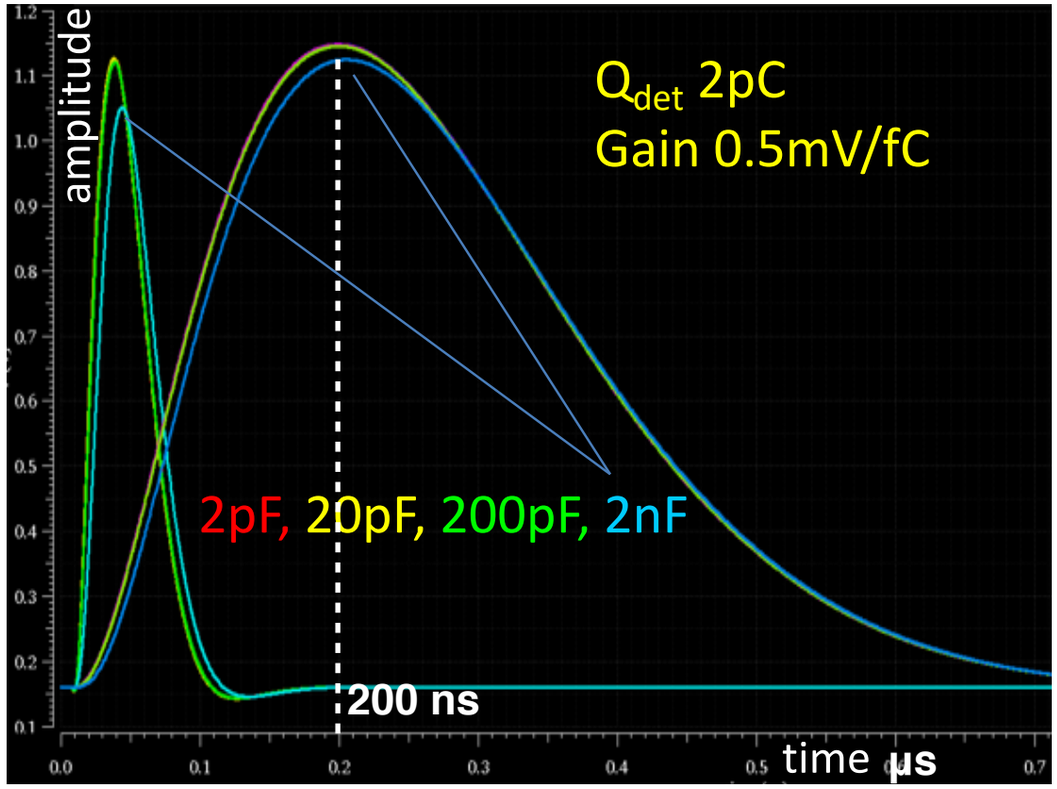
VMM **Amplifier & Shaper**



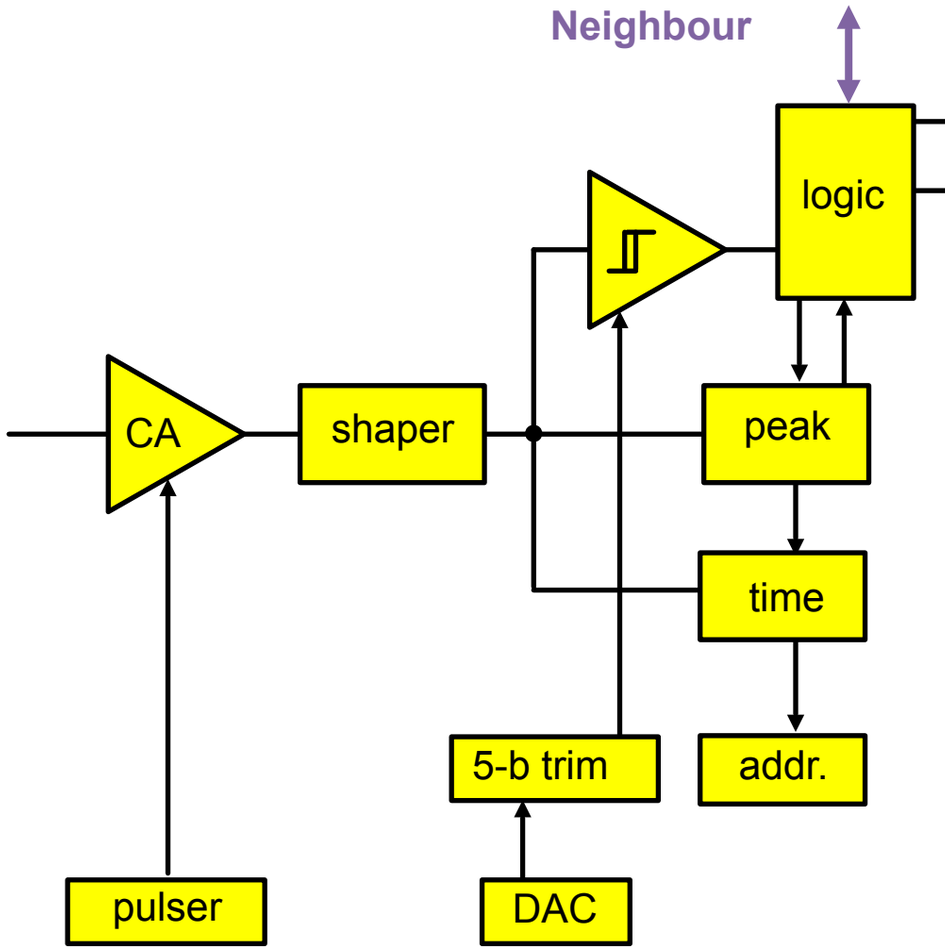


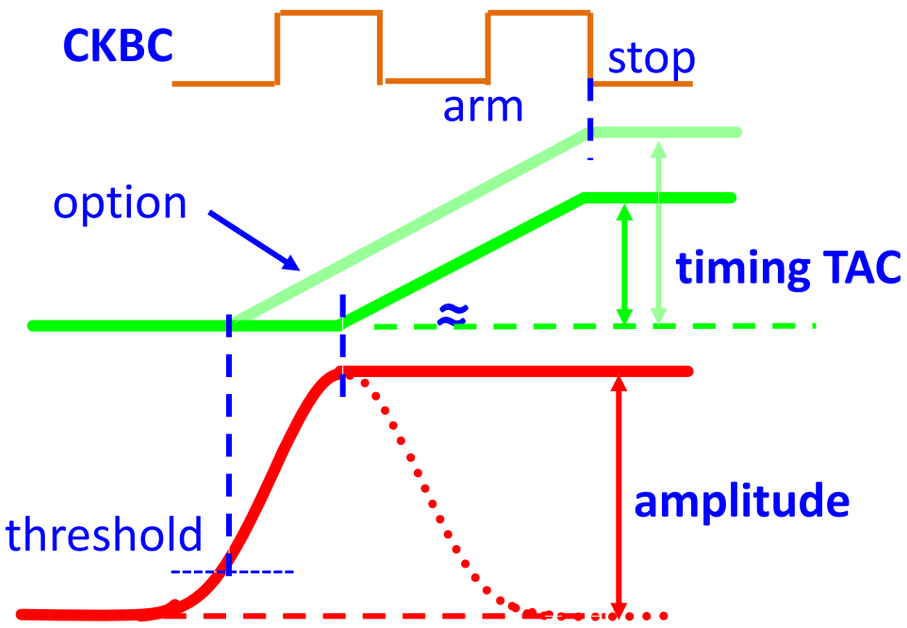


- Input transistor: **PMOS** 180 nm x 20 mm, 3 stage amplifier,
  - 2 stages used for **adjustable gain**: 0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC
  - 1 for **adjustable charge polarity**: positive or negative
- Input **capacitance**: can operate from sub-pF to several nF
- Maximum **charge**: 2 pC in linear range, fast recovery from 50 pC
- Semi gaussian **shaper 3rd order**
  - **Configurable** ion tail **suppression**: none, mild or strong
  - **Adjustable peaking** time: 25, 50, 100, 200 ns
  - Leakage-adaptive, DDF shaper, **BGR-stabilised baseline**



VMM3a **Discrimination, Charge and Time**

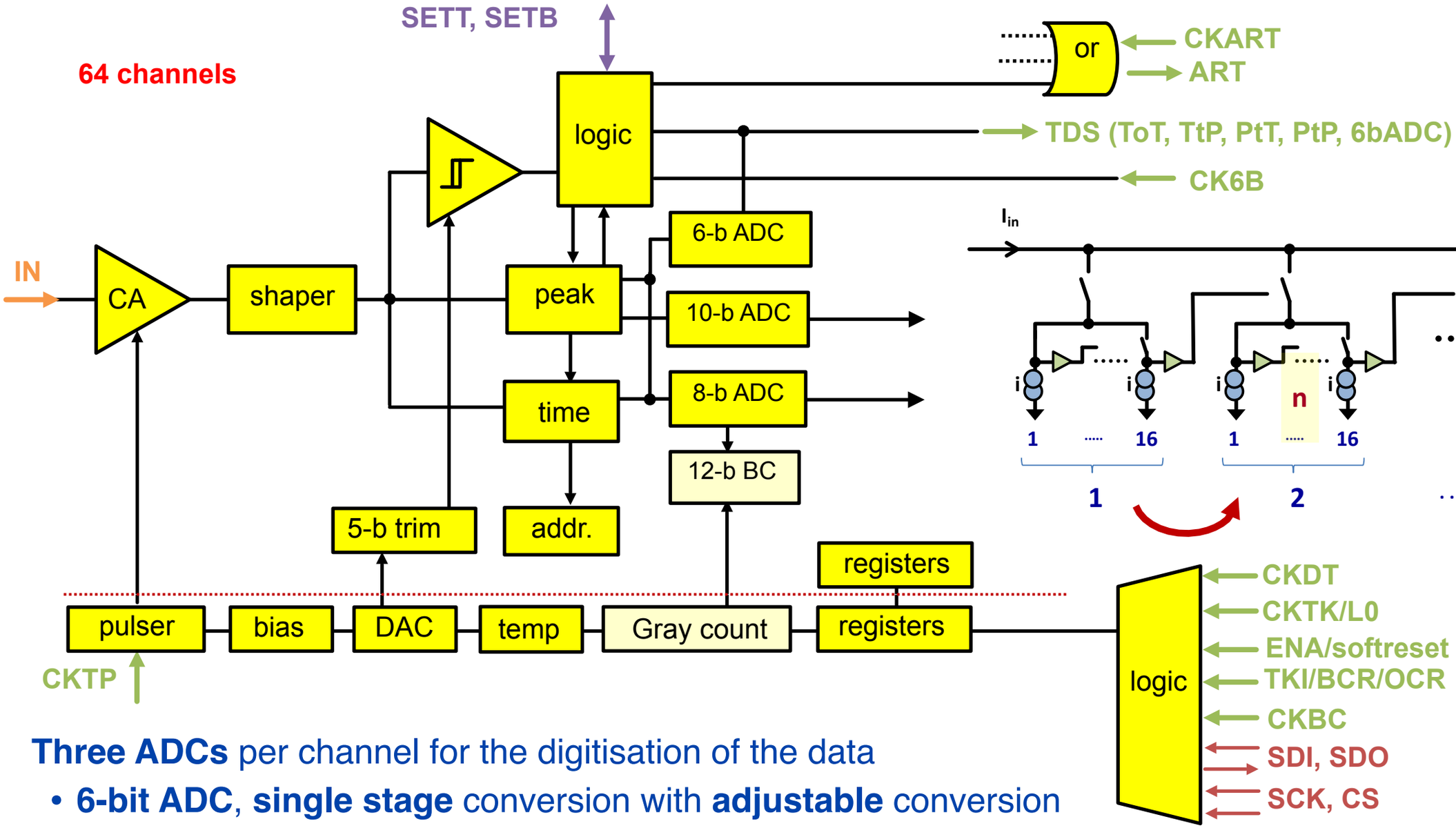




Configurable direct output
- time over threshold (ToT)
- threshold to Peak (TtP)
- peak to threshold (PtT)
- pulse at peak (PtP)

- Global 10-bit DAC for adjusting the **threshold** - **Discrimination** with sub-hysterisis (effective 2mV)
- Adjustable **5-bit discrimination** threshold **per channel** to adjust at ~mV level
- **Neighbour** logic to trigger sub-threshold channels with inter-chip communication
- Configurable **direct output** per channel and serial fast output of address as an OR of all channels
- **Peak detection**: measurement of peak **amplitude** and storage in analog memory
- **Time detection**: measurement of **peak/threshold** timing through a configurable time to amplitude converter (**TAC**: 60, 100, 350, 650 ns) and storage in analog memory
  - Clock working mode on **synchronous** machines but also as strobe for **asynchronous** operations

VMM3a **ADCs**

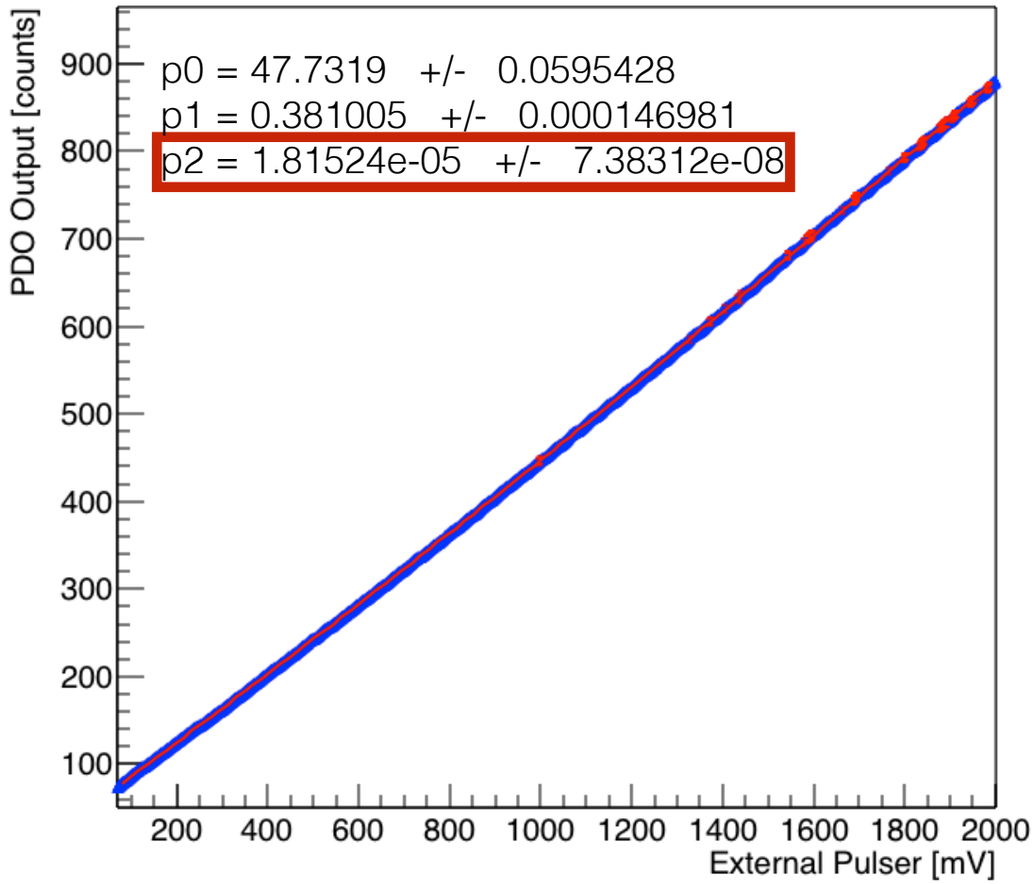


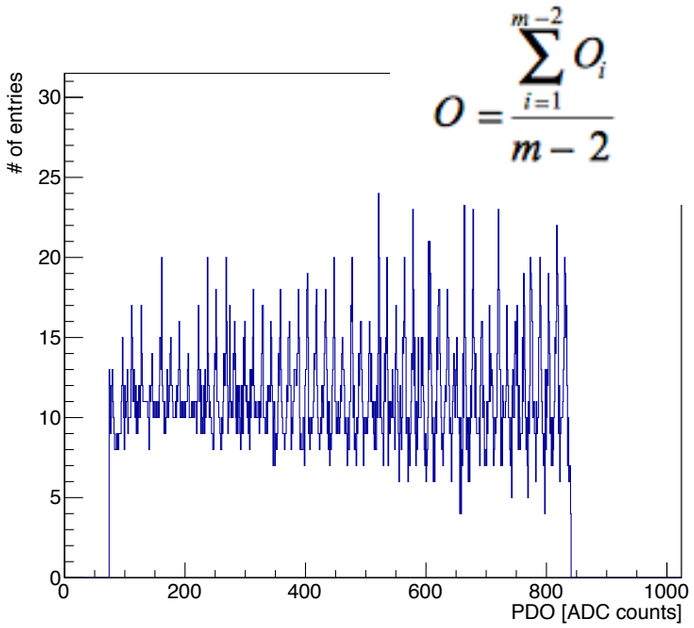
Three ADCs per channel for the digitisation of the data

- **6-bit ADC**, **single stage** conversion with **adjustable** conversion **time** and **offset**, completes within **25 ns from peak**
- **10-bit ADC**, **200 ns adjustable** conversion time/offset, for peak **amplitude** conversion
- **20-bit timing information** with 8-bit ADC, **100 ns** conversion time + 12-bit Gray-code counter, BC clock
- **2 step mode conversion for 10-bit & 8-bit ADCs** - First stage the comparison identifies one of the macro-cells and at the second stage the micro-cell is identified, possibility to jump through macro-cells

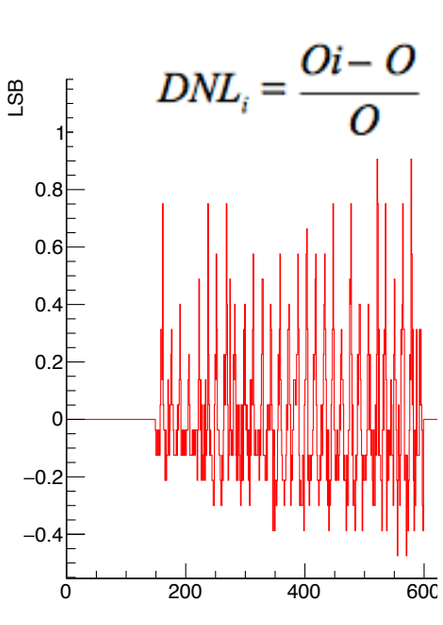
ADC Performance - 10bit example

- In order to evaluate the ADC performance, **a full scan** with fine step was performed
- The ADC cannot be driven with a sinusoidal waveform for accurate estimation of its “noise” from the FFT
- In that sense the **DNL** and **INL** is calculated and used to estimate the **ENOB** of the 10-bit ADC
- The non-linearity introduced by the ADC is of the order of **2×10^{-5}**
- **Equivalent number of bits ~8 (noise free)** for the 10-bit ADC

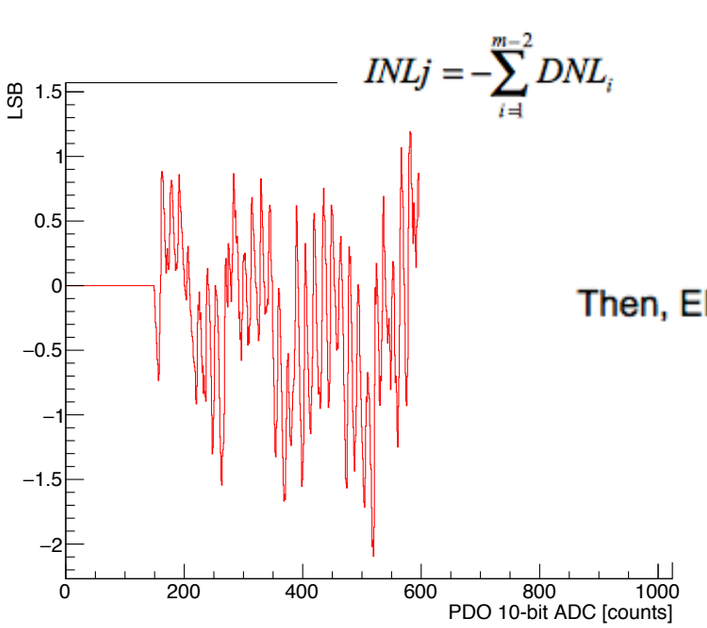




$$O = \frac{\sum_{i=1}^{m-2} O_i}{m-2}$$



$$DNL_i = \frac{Oi - O}{O}$$



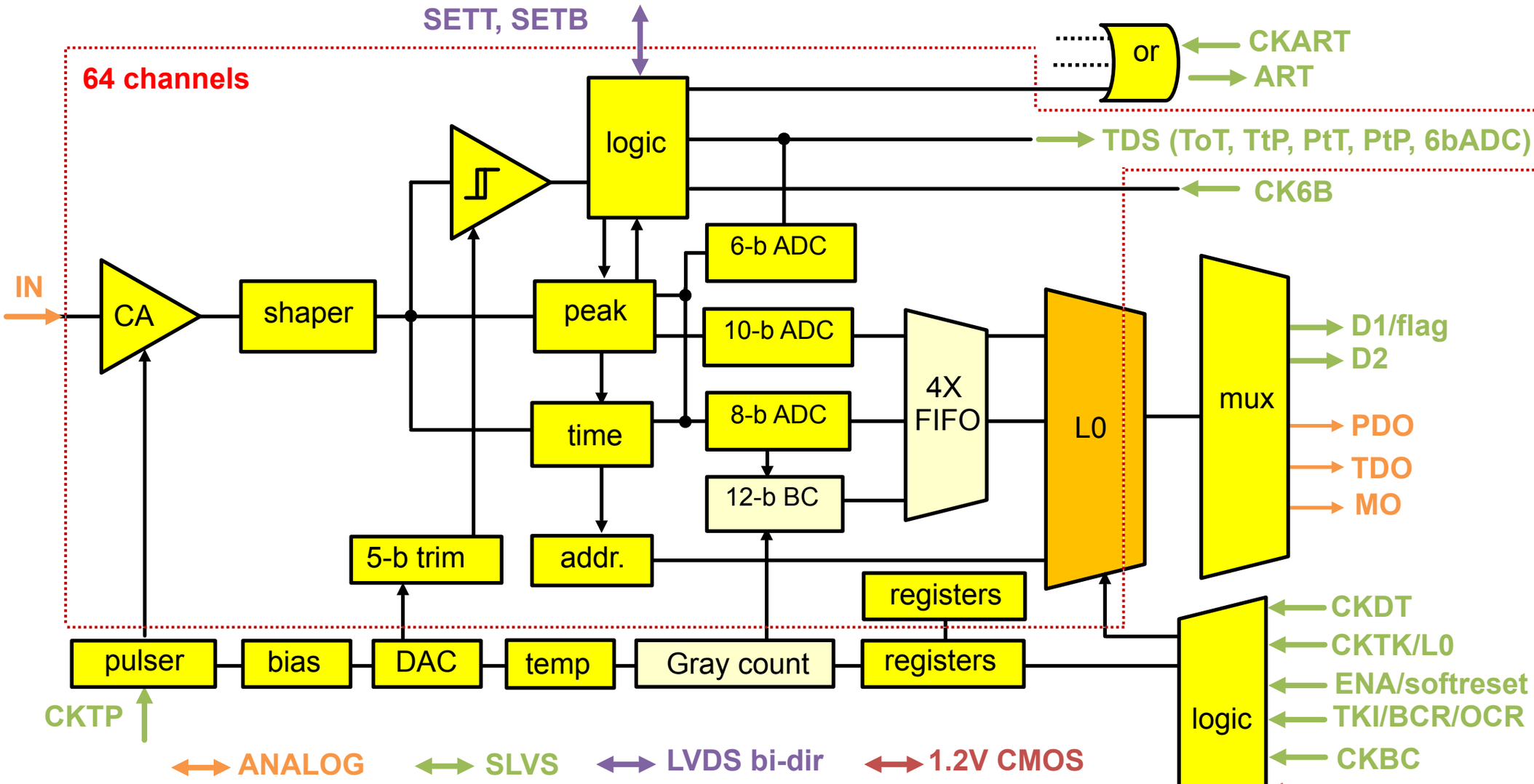
$$INLj = -\sum_{i=1}^{m-2} DNL_i$$

$$\sigma_c = \sqrt{\frac{1}{12} + \frac{1}{m-2}\sum_{i=1}^{m-2} INL_i^2}$$

Then, ENOB can be calculated as

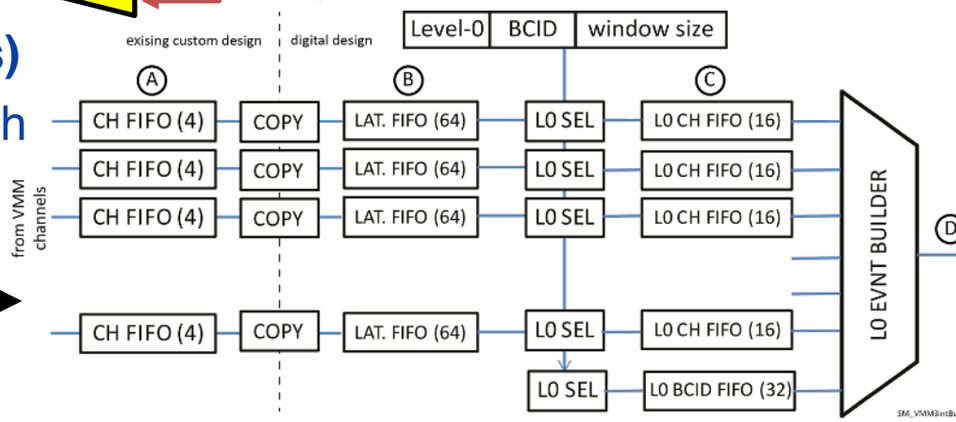
$$ENOB = \log_2 \frac{m}{\sigma_c \sqrt{12}}$$

VMM3a Readout & Overall **Architecture**



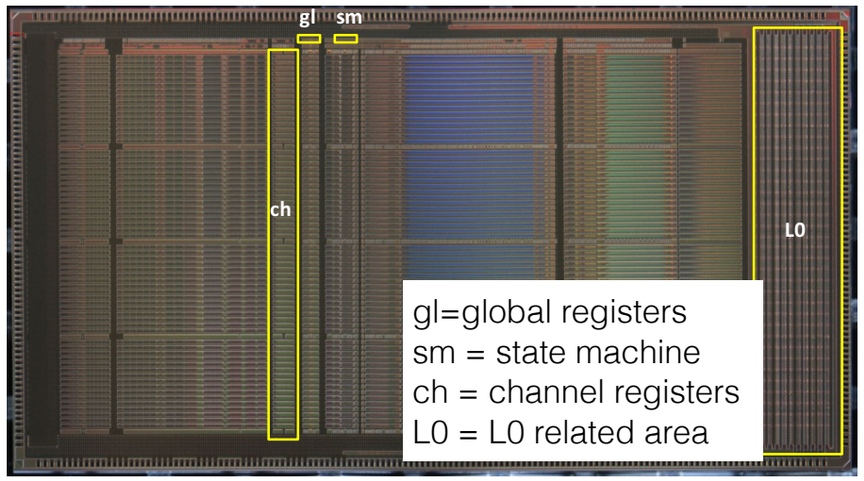
Three readout modes

- **Mixed** mode with peak & time analog output + address **(external ADCs)**
- **Digital continuous** with **internal ADCs** and 38-bit data at 2 outputs with 200MHz DDR, **trigger-less** or with **external trigger** and auto reset
- **Level-0** processor **external trigger mode** with 64-deep latency FIFO programmable acceptance windows with 8b/10b encoding



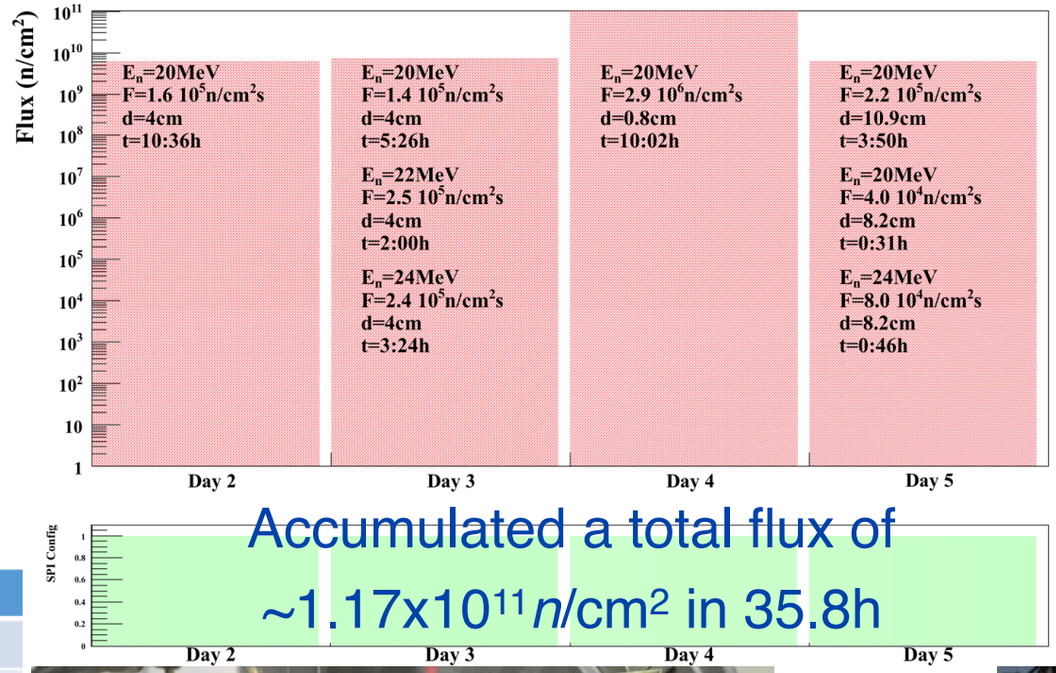
Single Event Upset & Total Ionisation Dose

- In the VMM3a there are **three types of storage elements** that require SEU protection, the **configuration registers**, the **state machine** control logic and the **L0 logic**
- To mitigate for SEU two techniques are used:
  - **Dual Interlocked Cells** (DICE) for the protection of the configuration registers
  - **Triple Modular Redundancy** (TMR) for the state machines and the L0 Logic blocks
- L0 Data
  - Single-bit faults on data are flagged by a **parity bit**
  - The parity is registered in the FIFOs and transmitted outside

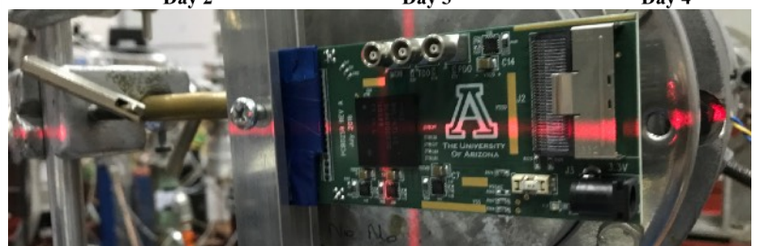


L0 block protection

Block	Method
BC counter	TMR
Latency FIFO CTRL	Parity on FIFO pointer, FIFO resets if parity error
L0 FIFOs Control	TMR
Event Builder	TMR
L0A register/Nskip circuit	TMR



Accumulated a total flux of ~1.17x10¹¹ *n*/cm² in 35.8h

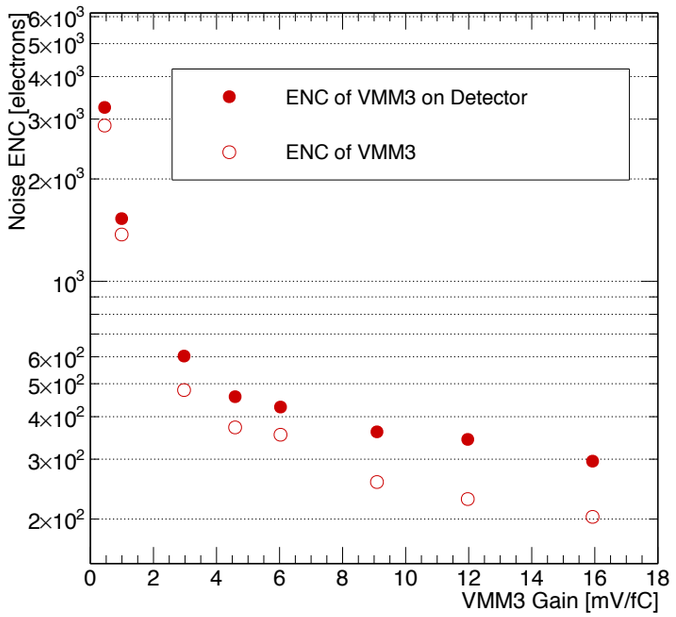


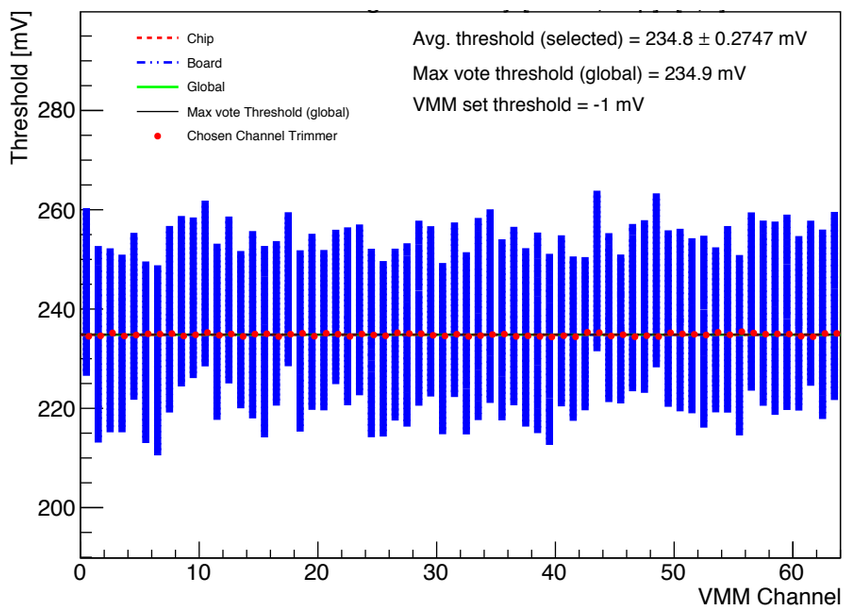
4 VMM3a were irradiated at the ^{60}Co source at BNL working fine for the 300kRad needed for ATLAS

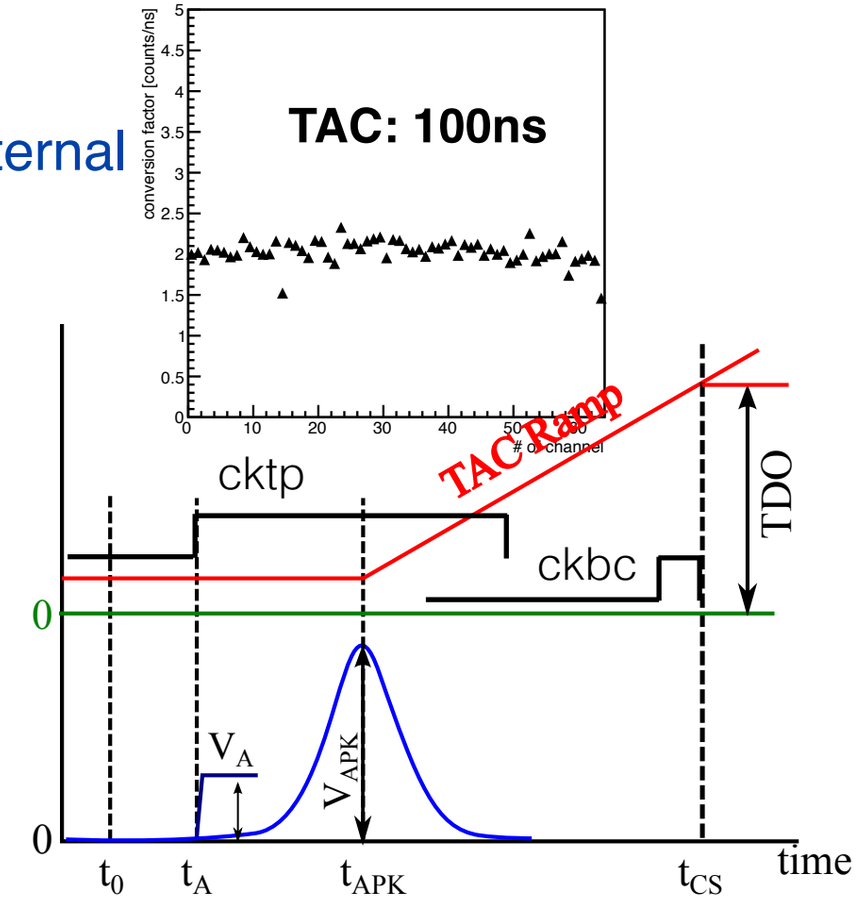
Test Beams with **Resistive - Micromegas** prototypes

- **Setup** of of 2x MMFE1s on 2x Resistive Micromegas chambers (Ar+7%CO_2 400µm pitch, 5mm drift)
- Custom made **firmware** and **software** was developed allowing to **trigger** with scintillator system
  - Mode to control the CKBC externally
- **High** data **rate** ~20KHz/channel (VMM can reach 4MHz), arrived at the limit of Gbps UDP connection
- **Noise** levels of 300 e^- ENC at gain 9mV/fC, 200ns

- Detailed **calibration** was performed to align the channel **discriminators** and also to measure the time with respect to external trigger for **precise timing** measurements needed for the µTPC

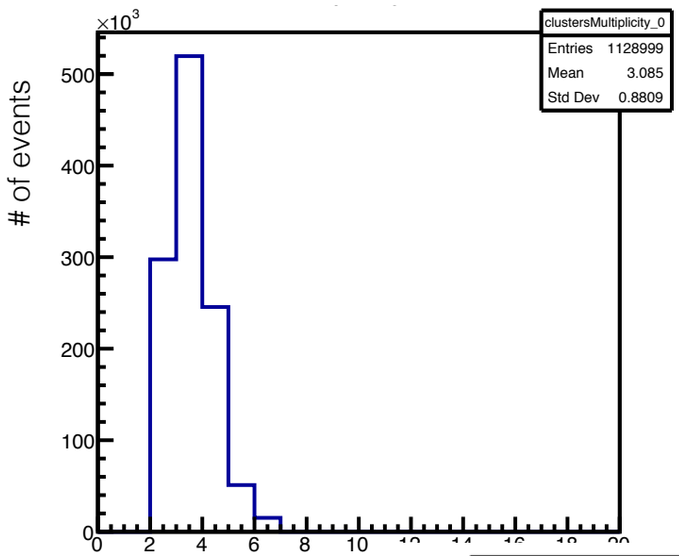


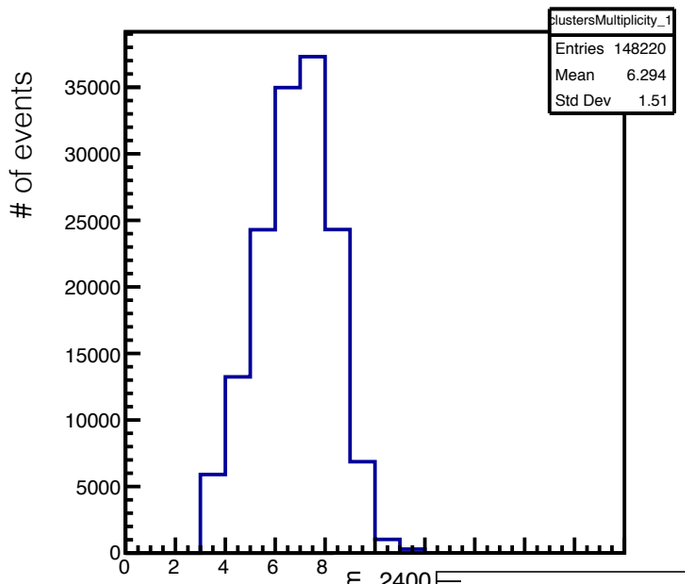


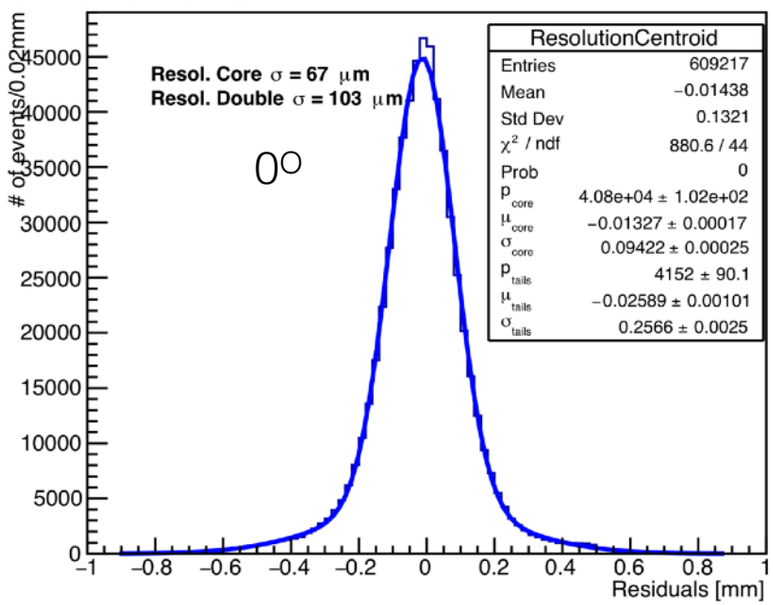


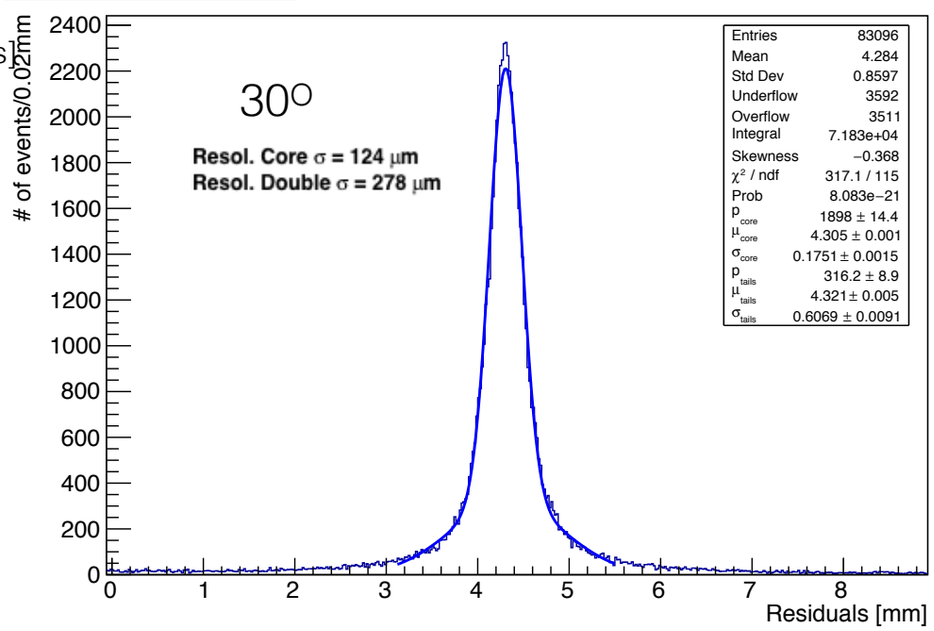
Test Beams with Micromegas prototypes

- To form **clusters** of strips per particle hit **charge centroid** was used for perpendicular tracks and **μTPC** for tracks under an angle with a pattern recognition filter
- After **forming the clusters** the position **resolution** is measured by **subtracting** the space point reconstructed in different layers (identical layers)
- The spatial performance of the detectors is **satisfactory** for the NSW application



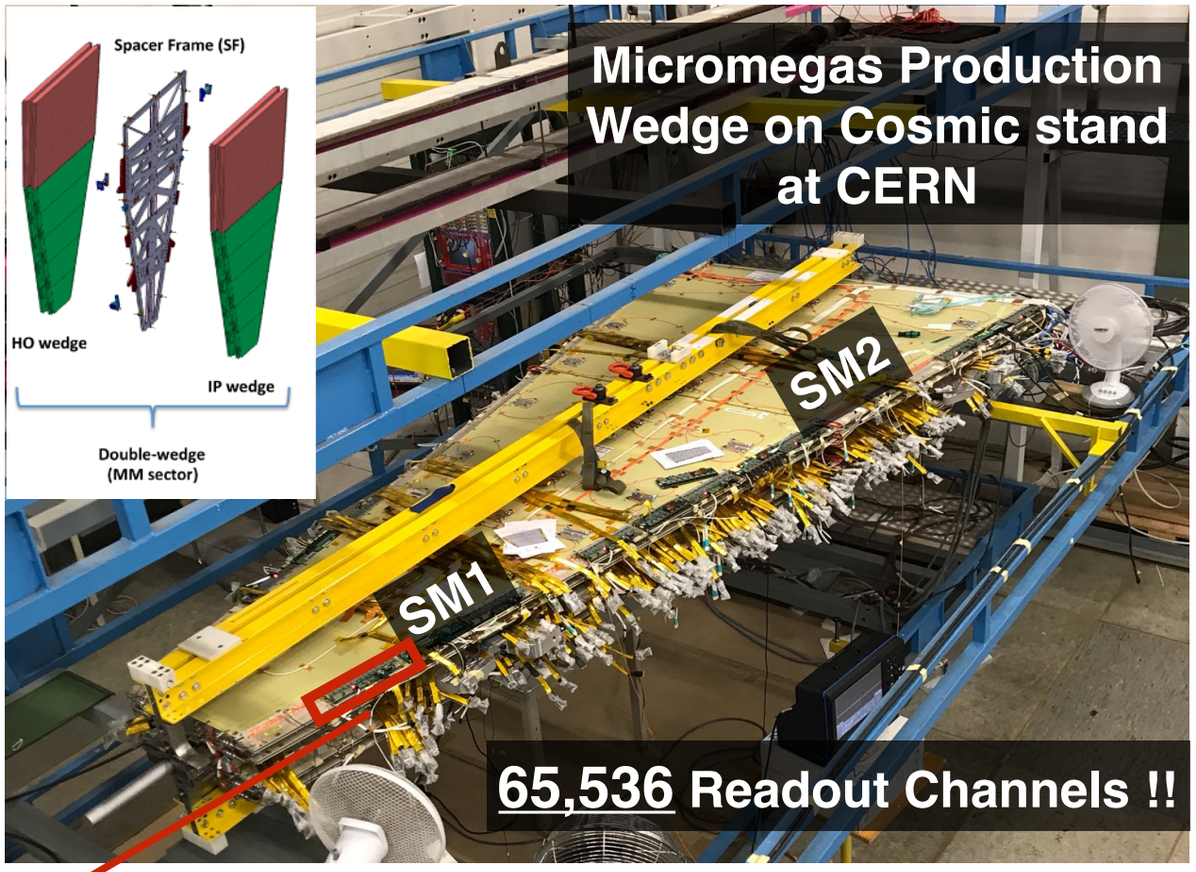




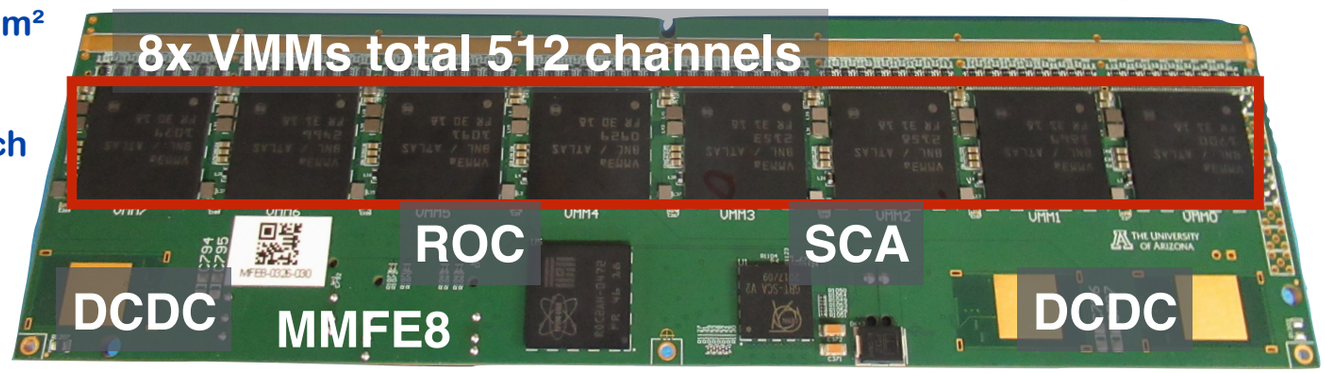


Integration with Micromegas **Production** modules

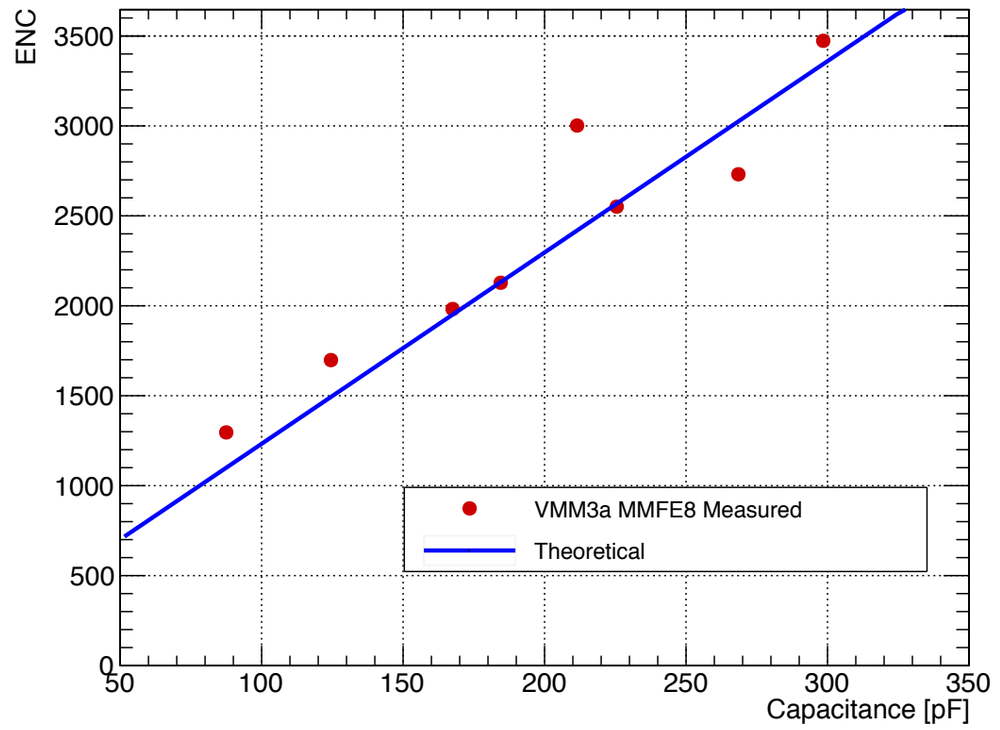
- **Micromegas** Production modules are arriving at CERN BB5 **integration** facility
- They are **assembled** on either side of a stiffening panel
- On either side of the wedge, **32x MMFE8** frontend boards are installed (128x total/sect)
- **Alignment** platforms are glued on the surface
- All the FE boards are readout through custom made 4.8Gbit serialiser boards with fibres
- **Highly complex** services routing (electronics readout, fibres, LV, HV, cooling, gas)



400-pin
21 x 21 mm²
BGA
1mm pitch

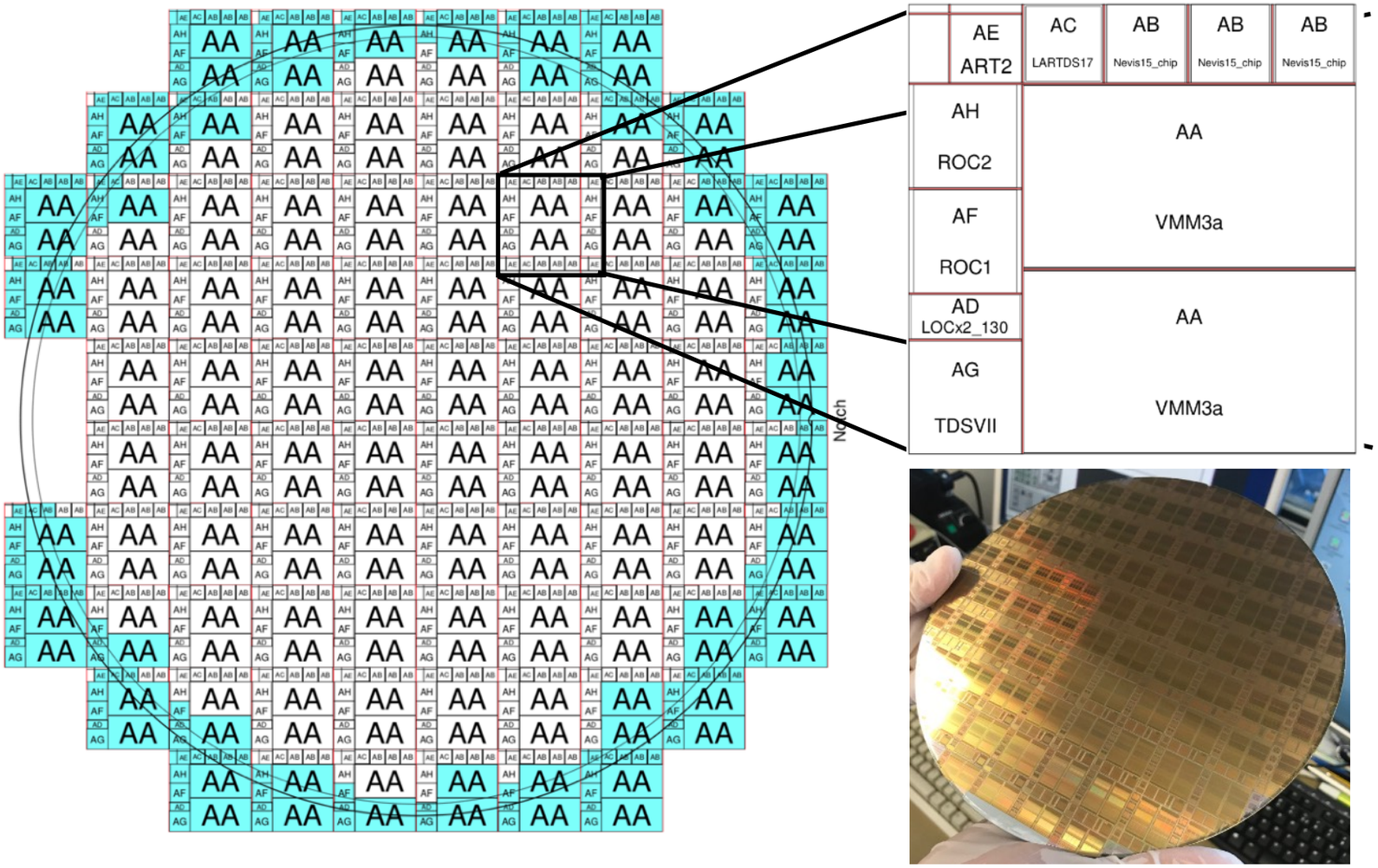


- **Noise** measurements with the production electronics and chambers show good performance and **matches the theoretical expectations**



VMM Production & Other Applications

- The **VMM** is **produced** in a 8” **wafer** with 2 copies of the chip in a reticle, **total 113 chips per wafer**. In the same floor-plan other ATLAS ASICs are included
- ATLAS has submitted a **production order of 70,000 Chips** - delivery starts on mid-May 2019
- Many iterations with experts from Global Foundries to improve the yield (currently ~72% due to damage on the Baseline stabiliser circuit). Already got indications on issues in their processes, but not clear on how to improve the yield.



VMM has been as well **proposed** and in some cases **accepted already** in the following other than NSW applications:

- Focal Plane Detector for NUMEN
- n_TOF at CERN
- Mu2e at Fermilab
- DUNE Near Detector at Fermilab
- CERN RD51 SRS system (replace APV hybrids) which is a hub for **many other applications**

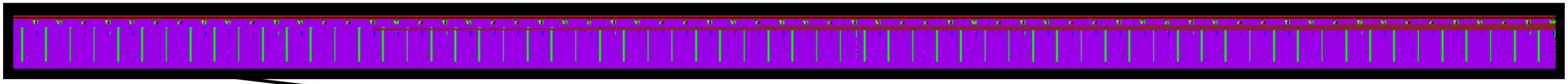
Closing remarks

- **VMM developments** for the last 7 years **concluded** with a **successful production** version for ATLAS, **VMM3a** (fourth iterations from the beginning)
- **VMM3a** was **tested** thoroughly on bench, prototype and production detectors achieving the needed performance
- **Already a success** being **proposed** for multiple **systems** and **experiments**
- **New Small Wheels** are the first and the **biggest MPGD upgrade** in high energy physics and **VMM** was **validated** after multiple reviews to **fulfil the requirements**
  - ATLAS entered the **production of 70,000 chips**.
  - CERN RD51 joined the production with 2,800 chips

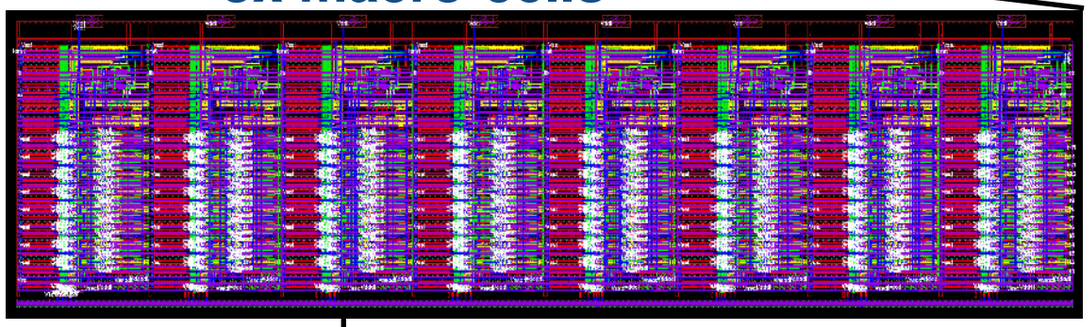
Thank you for your attention

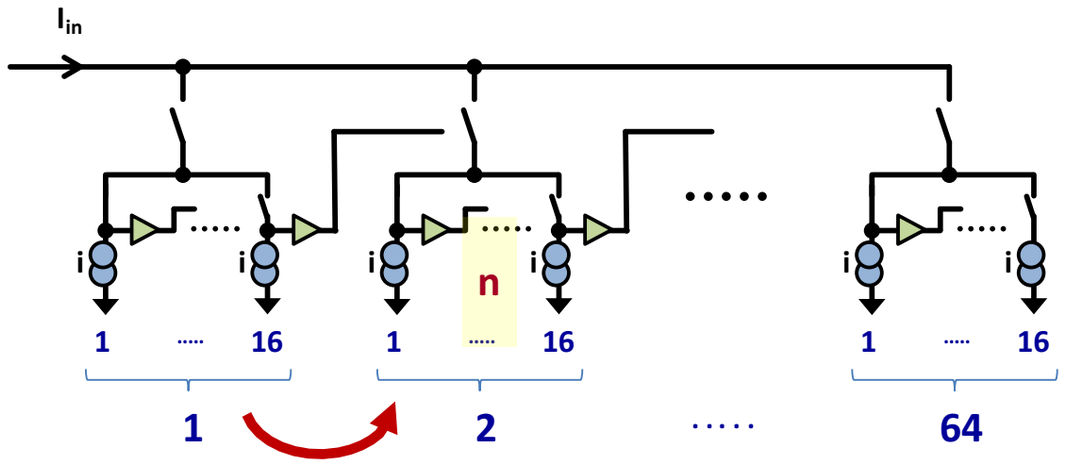
10-bit Current-Mode Domino **ADC** - Functionality

ADC Cells

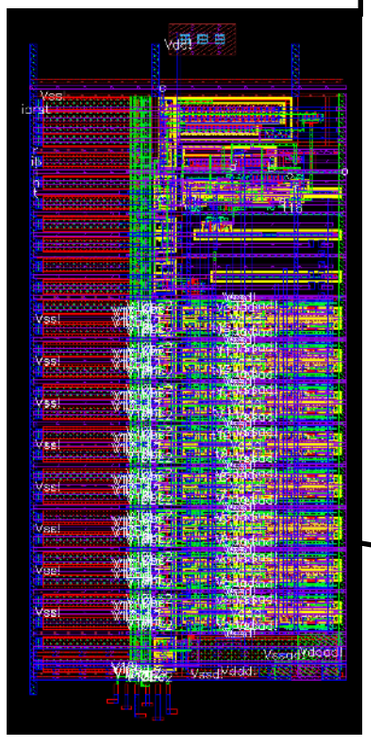


8x macro-cells





1 macro-cell

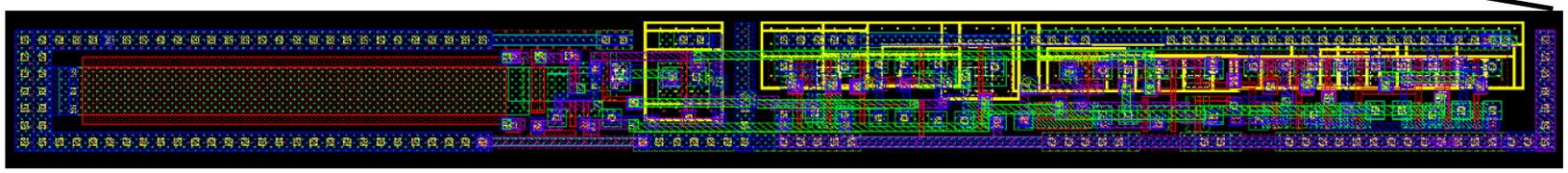


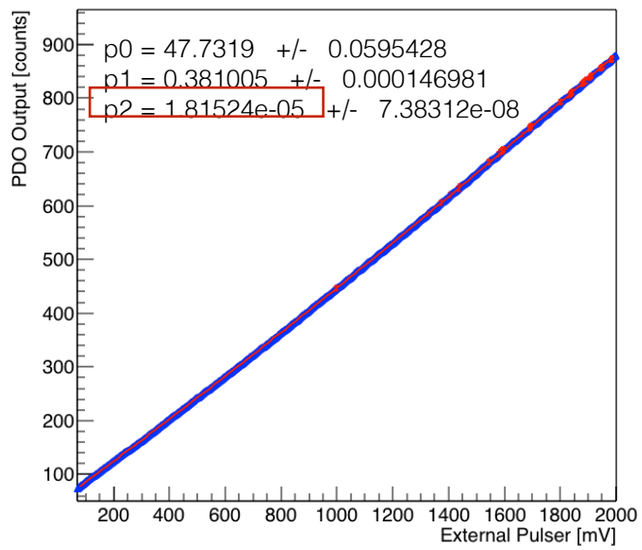
16x micro-cells

ADC Core (per channel)

- **1024** current sources (similar to a digital thermometer)
- **64** macro-shells (6 upper bits xxxxxx0000), **16** micro-shells (4 lower bits 000000xxxx)
- **2 step mode** - First the comparison identifies one of the 64 macro-cells Then on second step the lower 4 bits are identified (200ns conversion time)
- **8 bit ADC** is build in the similar way
- **6 bit ADC** is a **single stage conversion** similar to the 64 macro shells with fast digitisation (50ns)

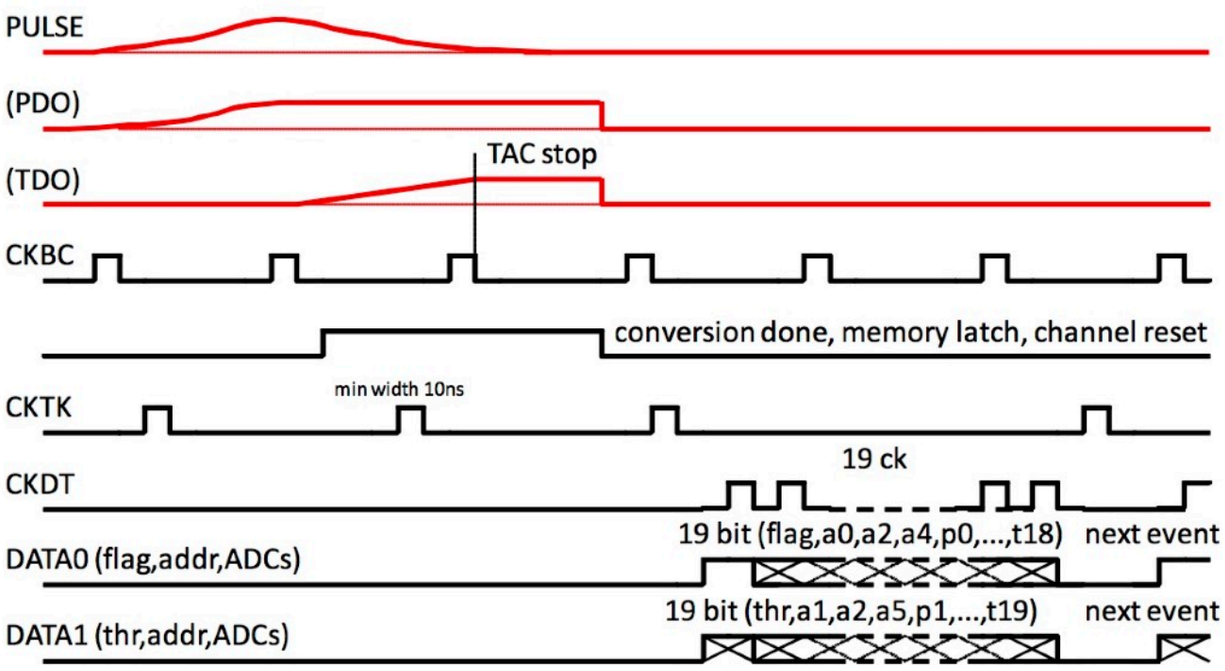
1x micro-cell

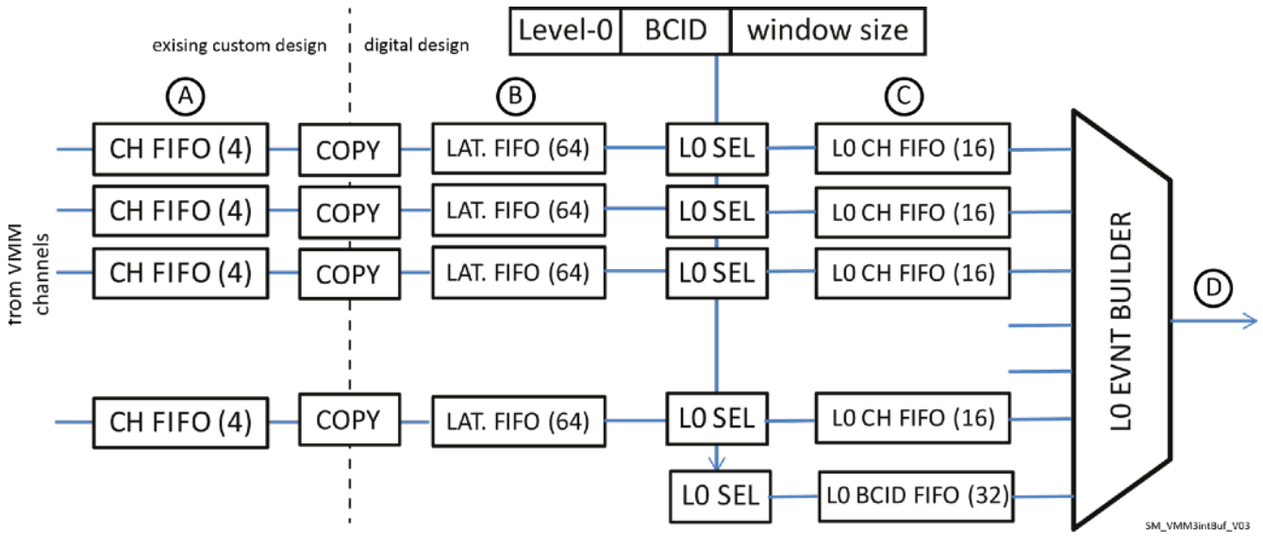




Multiple **Readout** modes

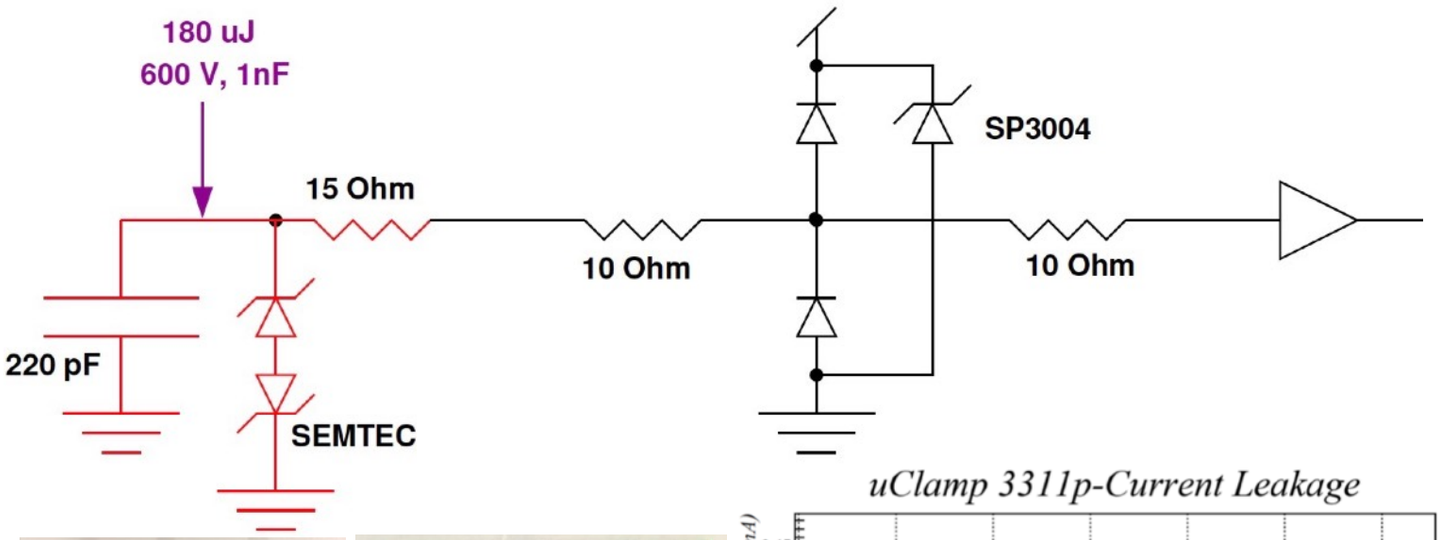
- Most of the **chip developments** for high energy physics are built for **synchronous machines** which makes measurements difficult once at **environment like test-beams.**
- **VMM** implements several **three readout modes**.
  - Two-Phase Analog Mode (external ADC) which uses the **analogue** features of the ASIC.
  - **Continuous** (Digital) Mode (internal ADCs) which is mostly used in **test-beams** and someone can perform **accurate timing measurements** (clock uses as a **strobe** controlled by trigger)
  - **LVL0 Mode** (**ATLAS** Readout mode) - The event processing is done in the same way like the continuous but the readout is different. Each channel has a **Level-0 Selector** circuit which is connected to the output of the channel's **latency FIFO**. The selector finds **events** within the BCID **window** (maximum size of 8 BCs) of a Level-0 Accept and copies them to the L0 Ch FIFO. The **data are available in the output** which to be readout.

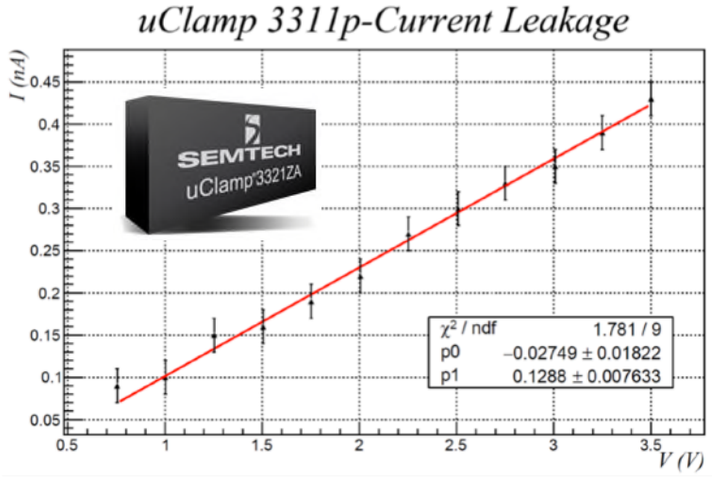


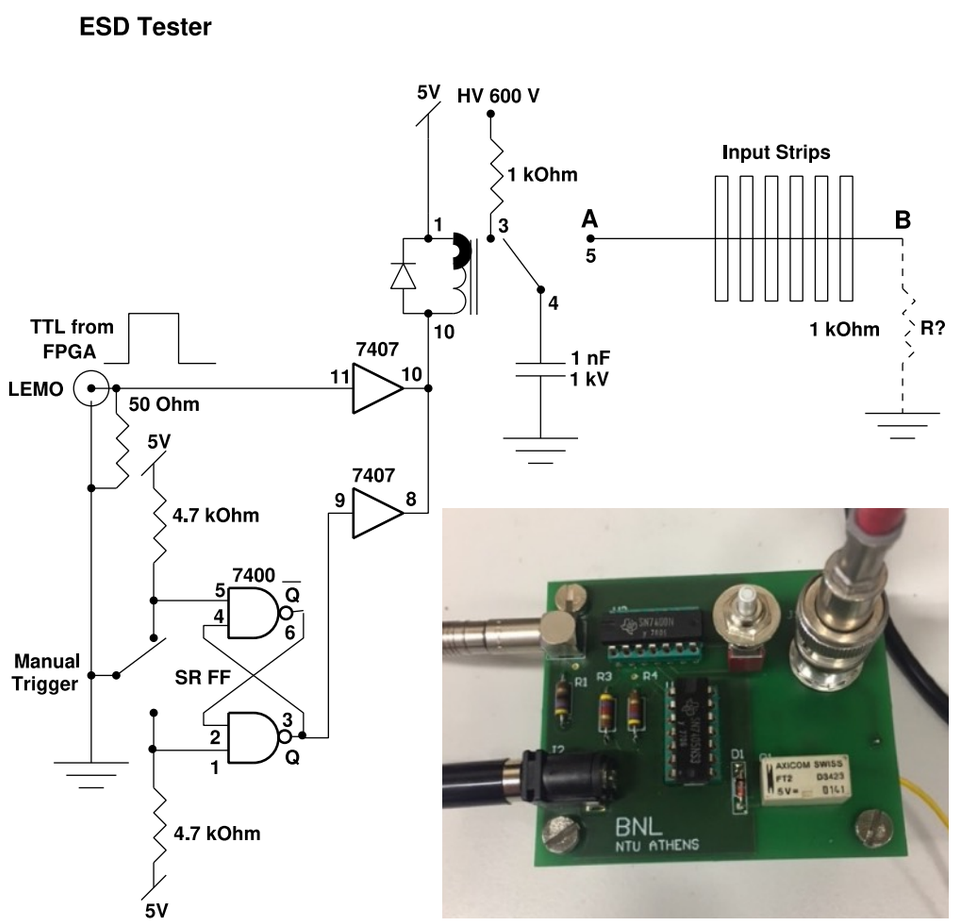


Input protection schema

- Since the VMM2, we have experience major channel (initial NUP4114 issue). Moving to 130nm technology made the requirements on input protection higher. Current protection scheme based on the SP3004 seems inadequate to protect the VMM front ends
- A dedicated ESD testing procedure was lunched allowing a systematic test of the VMM input.
- A VMM board (MMFE1) with Panasonic connector and a VMM socket was developed to perform systematic tests. On top a Panasonic based connector daughter-board was built to test different protection schemes and different footprints.
- 220 pF capacitor emulates typical MM strip capacitance, a channel like this survived repeated discharges while without protection is dead after a single discharge. Then survived zapping overnight (>30,000 discharges)

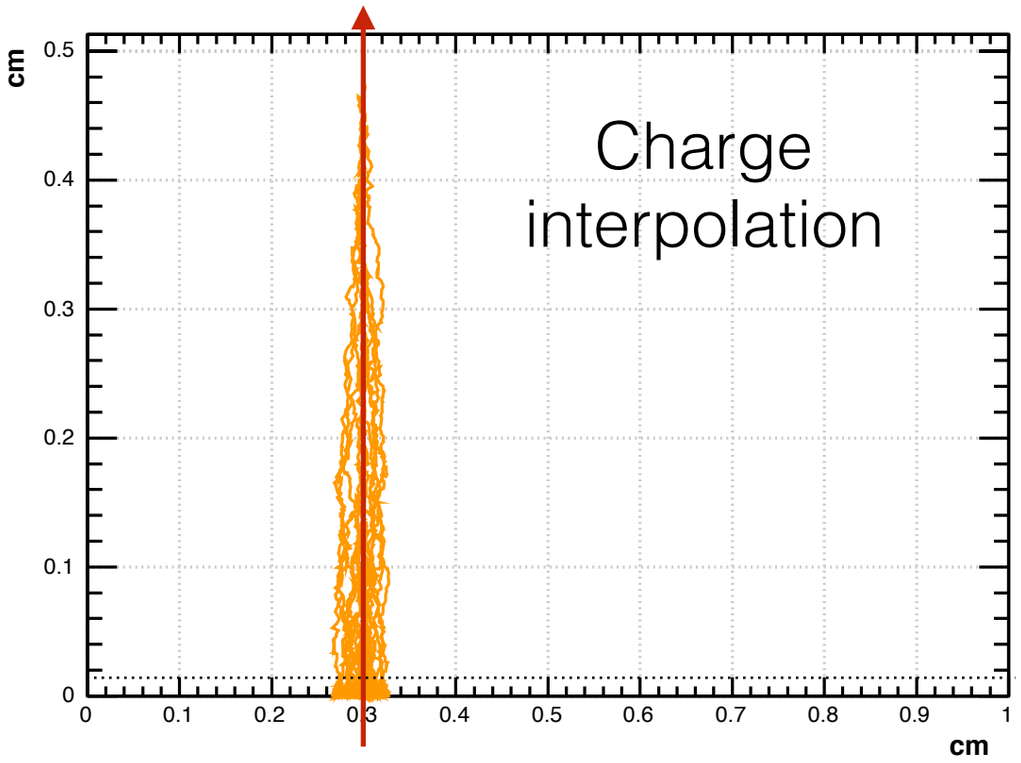


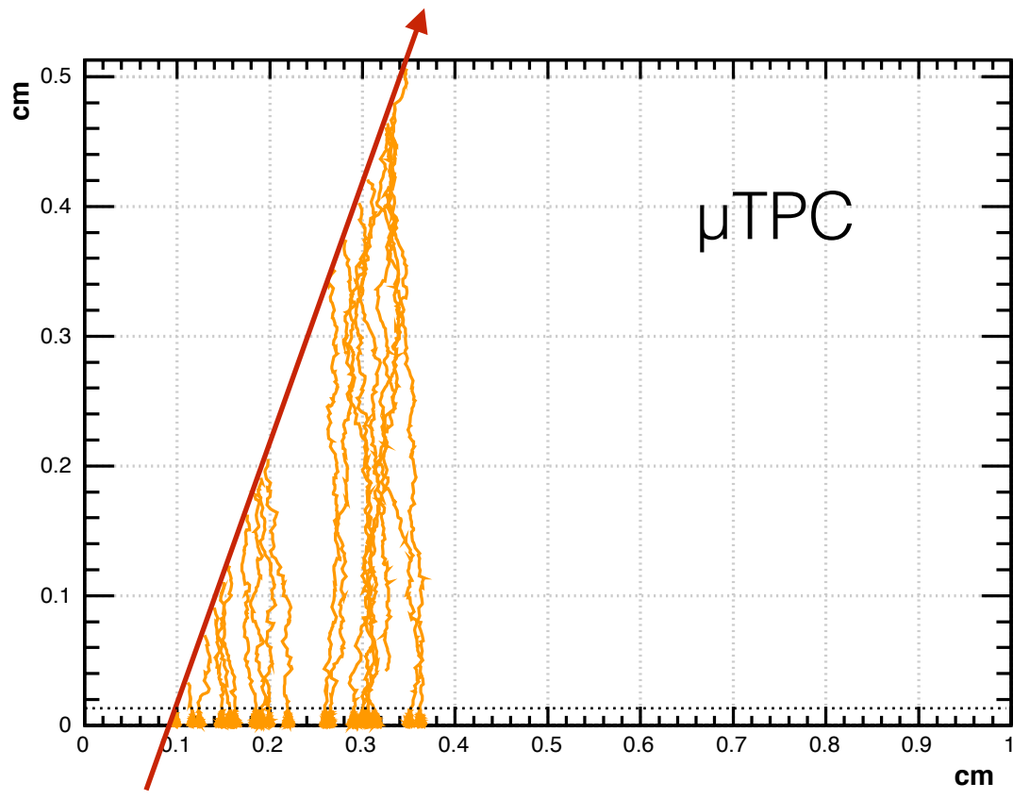




µTPC - The concept

- In the NSW the **track range** is 5º-28º for the tracks originated from the IP
- It is mandatory to be able to **reconstruct the position** of a particle that transversed the detector under an angle **with high resolution**
- The **charge centroid method** is proven **not to be able to provide** good resolution for tracks over 5º.
- Instead a **new method** was implemented in the Micromegas called the **µTPC**
- This method implies on **measuring with high accuracy** (<3ns) **the arrival time** of the primary ionisation above a strip.

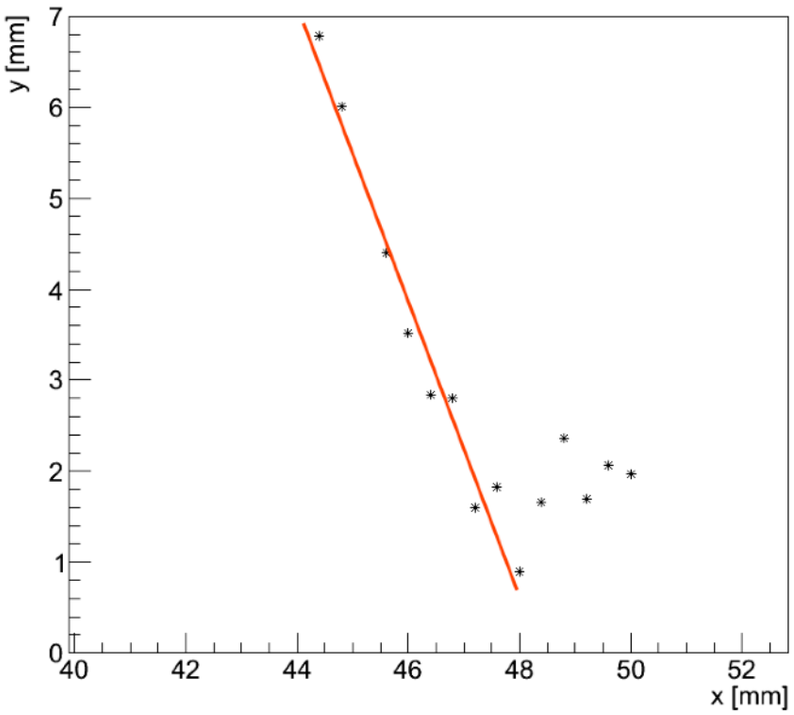




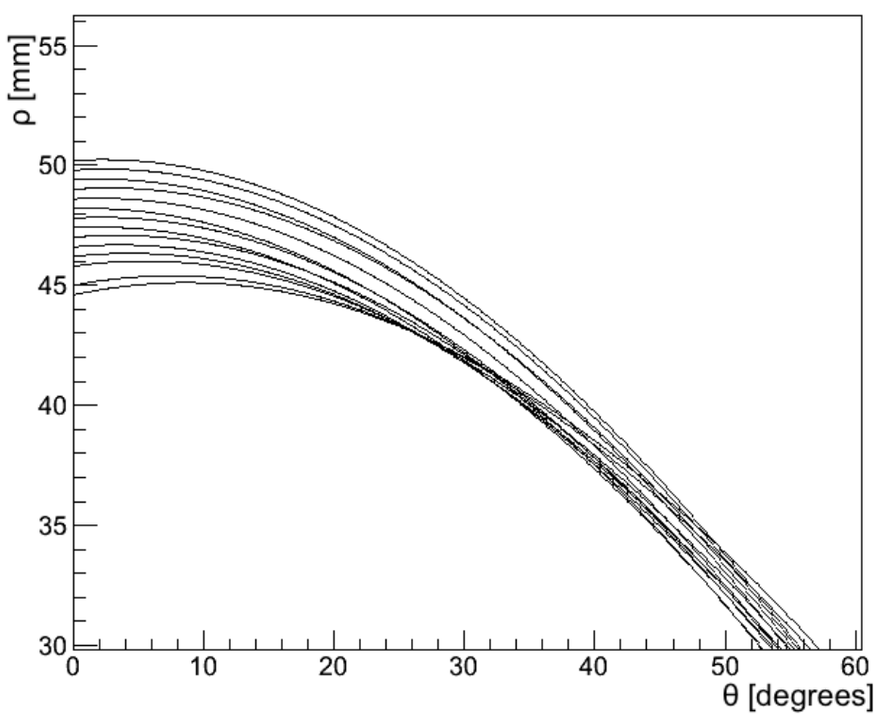
µTPC - **Clustering** under an angle

- **Clustering** strips for **inclined tracks** is a challenging task due to:
  - Ionisation statistics, there are **fluctuations** on **primary** cluster generation that can give "holes" in between a cluster of strips **depending on the incident track angle**
  - Generation of **delta electrons**
  - **Multiple** track events
  - **Noise** in the system
- For this reason, a **pattern recognition technique** including the **Hough** Transform is used as a **filter** efficiently removing noise, delta electrons, separating double track events

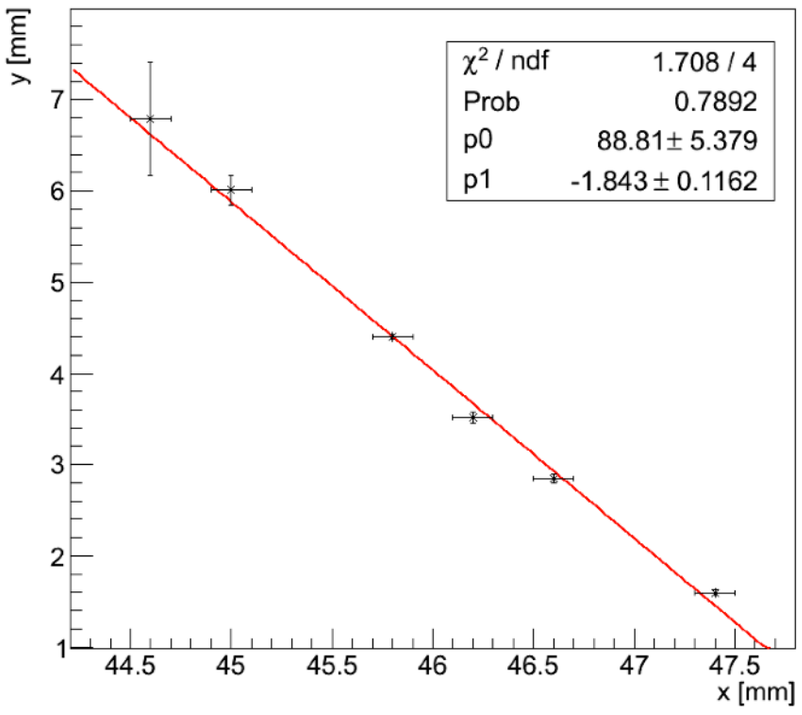
Hough line



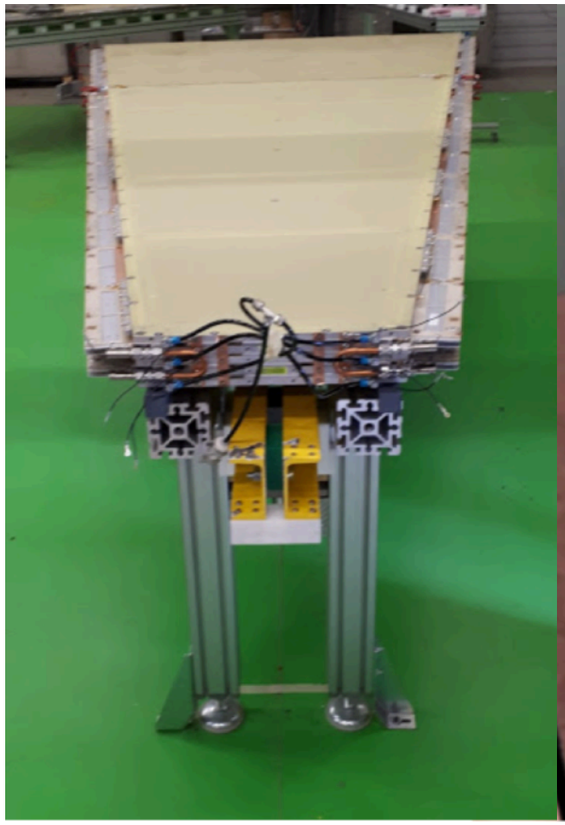
Hough Space

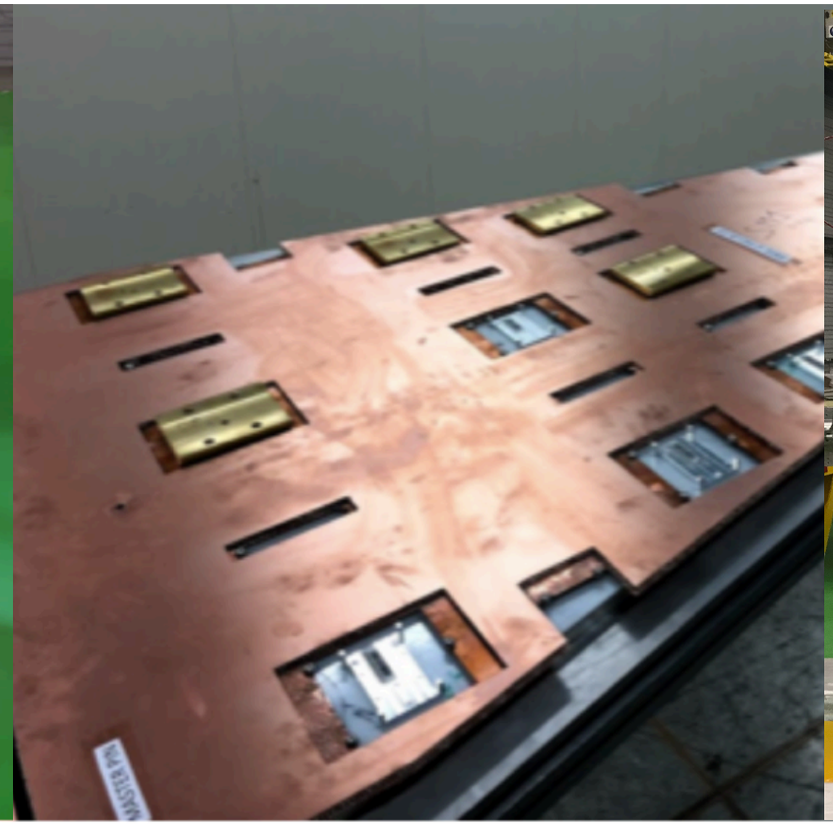


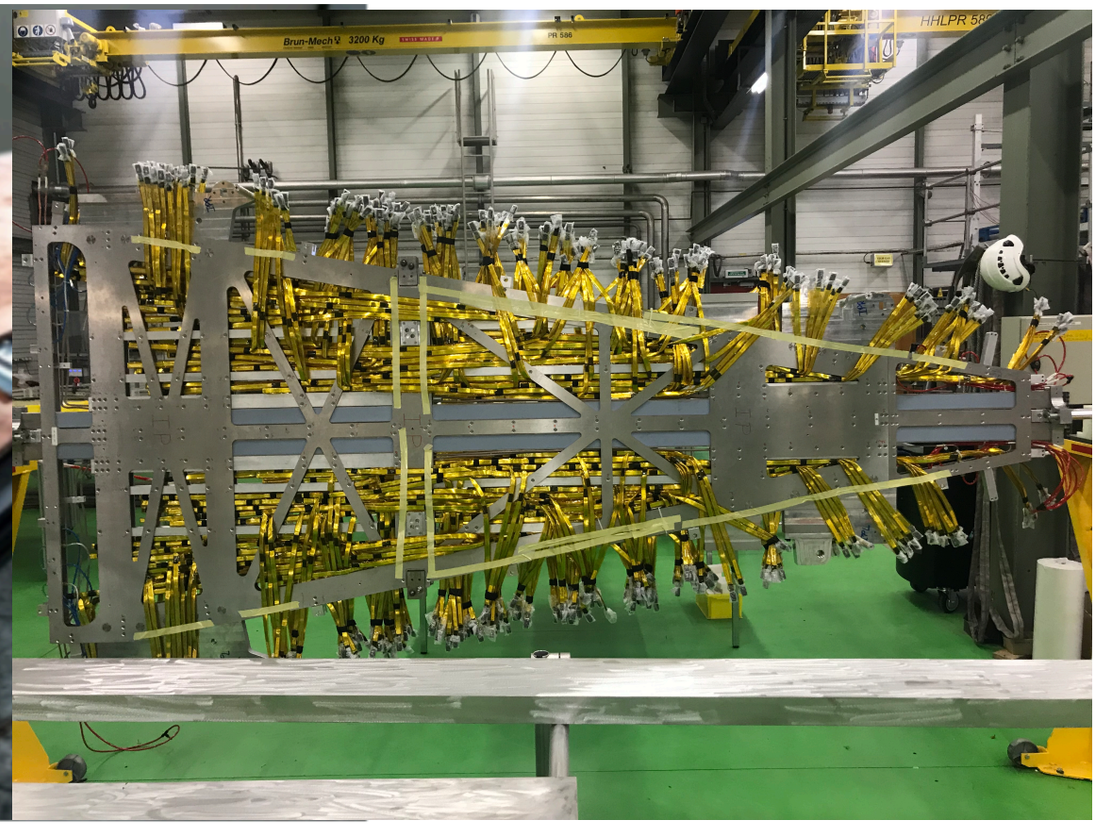
Linear fit after filter

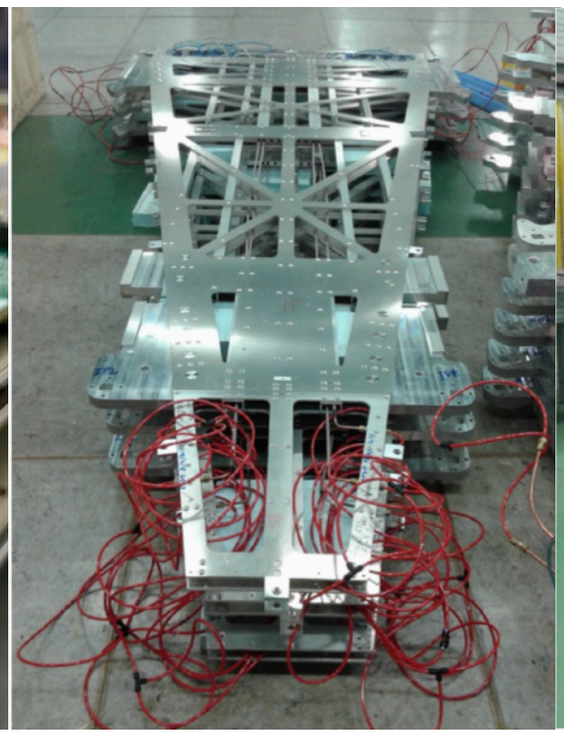


Integration highlights



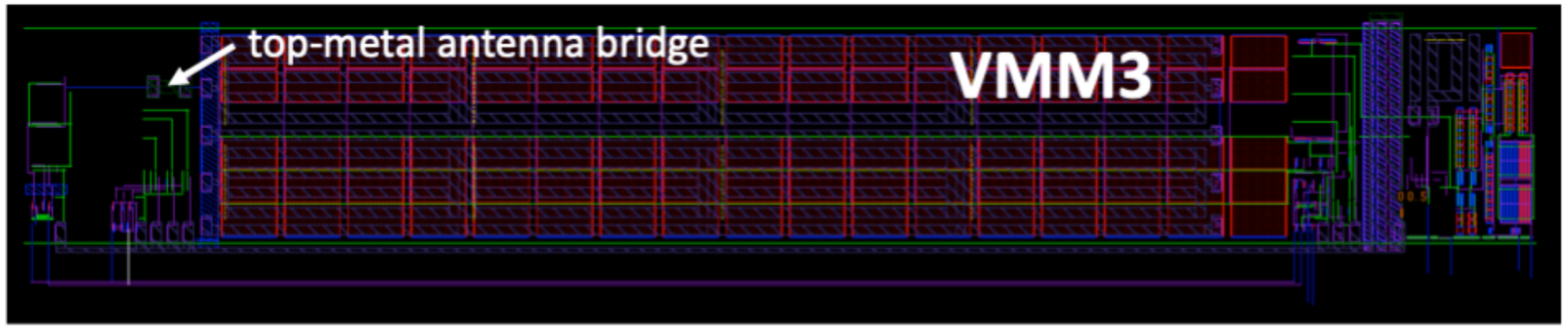


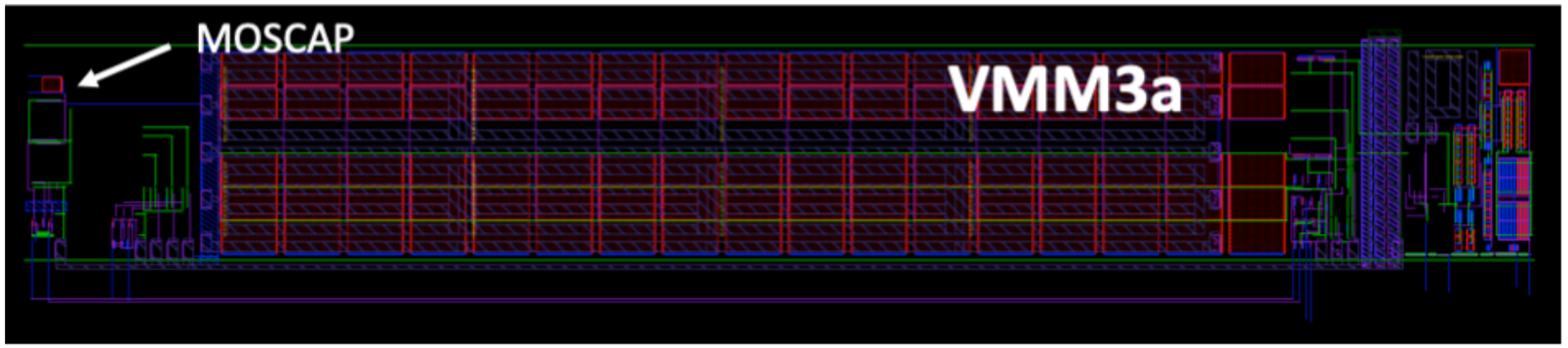


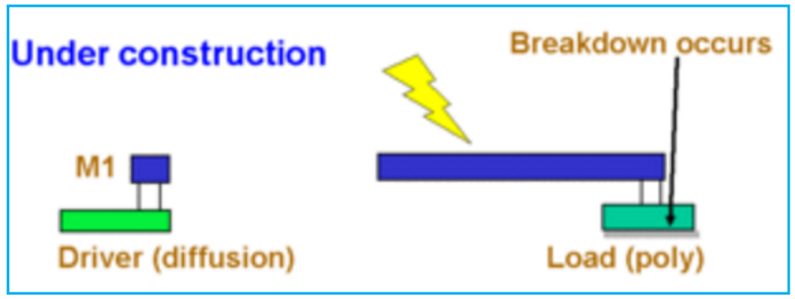


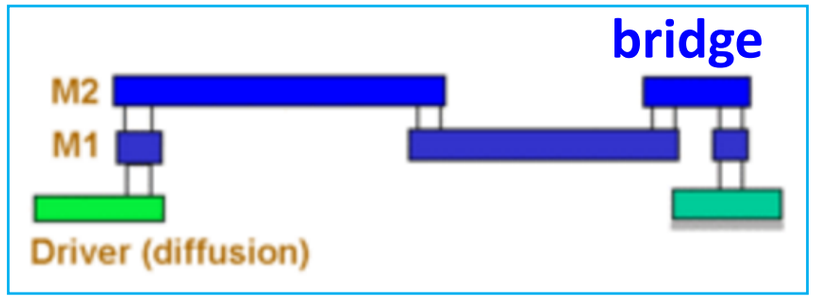
Integration highlights

- On VMM3a, under the suspicion of antenna damage, the bridge of the top layer was replaced by a MOSCAP
- **Just to note that both designs are satisfying the DRC for antenna damage**









- The issue cannot be explained from simulation:
  Points to damage of the gate, or degradation of it