A scalable High Voltage power supply system with SoC control for Micro Pattern Gaseous Detector

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in collaboration with ICTP MLAB
Outline

• The main goal of the project
• The HVPSS: the main blocks
• The characterization of the main components
• The performance of the system achieved so far
• Future plans
Introduction, the goal of the project (HighVoltagePowerSupplySystem HVPSS)

Main goal is to match the HV requirements not commercially available for the MPGD needs

- true real-time monitoring of the main parameters (voltage and/or current)
- the fast control of the HV channels (related to the next point)
- The possibility to apply user defined actions when pre-breakdown conditions are detected, useful for systems where the large number of HV channels increases the monitor and control complexity of the system
- HV generated at the detector level: HV cabling, connectors, space constrains, cost, accumulated charge issues
- Modularity of the system: large size projects employing MPGDs may use a large number of channels (M/S architecture)
- Compactness
Introduction, the HVPSS desiderata

By combining commercially available devices as well as custom made

- Time stamp resolution for current/voltage monitoring in the order of 10 ns or better
- High resolution voltage monitoring better than 0.5 Volt on several kVolt scale
- Precise current monitoring at the level of 10 pA
- On board logic for decisional operation on predefined monitored parameters conditions well as warning on “interesting” events to the user

A system at two “speed”
- 1) normal monitoring with time separation between consecutive data samples ~100ms
- 2) very fine monitoring information in case of non standard events (user defined) ~ns

features summary
1. true real-time monitoring
2. A tool to perform MPGD R&D: by the detailed time-stamped information, understand the precise evolution of the break-down events
3. HV generated at the detector level
4. Reduced size: each HV unit must be compact

Applications:
MPGD characterization studies
Powering of segmented large-size MPGD systems

Use of SoC
The main building blocks of the HVPSS

The main blocks I will illustrate

- Selection of the DC to DC converter (Commercial device)
- ADC Board FMC standard adopted (Custom made)
- The custom-made Pico ammeter (Custom made)
- Carrier (Commercial)
The DC to DC Converter: characterization

Low voltage input (5 or 12 V version) → up to ±6kV

A good noise figure is fundamental to avoid its propagation to the FE → Dedicated measurement

Reduced dimensions helps in miniaturizing the system

**EMCO**
- Q60-5R \( (V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } +6kV/0.5W) \)
- Q60N-5R \( (V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } -6kV/0.5W) \)
- A60P-5 \( (V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } +6kV/1W) \)
- A60N-5 \( (V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } -6kV/1W) \)
- AG60P-5 \( (\text{SMD, } V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } +6kV/1W) \)
- AG60N-5 \( (\text{SMD, } V_{in} = 0 \text{ to } +5V, \ V_{out} = 0 \text{ to } -6kV/1W) \)

**ISEG**
- BP040105n12
  - PCB-HV-module of 4W BPS series (now available also up to 6 kV)
  - \( V_{out} = 0 \text{ to } -4kV / I_{out\text{nom}} = 1 \text{ mA} / V_{in} = 11,5 \text{ to } 15,5 \text{ V-DC} \)
  - \( V_{remote/mon} = 0 \text{ to } 5 \text{ V} / V_{I_{mon}} = 0 \text{ bis } 5 \text{ V} / V_{ref} = 5 \text{ V} \)
  - Ripple & noise < 40 mVpp at full load
- BP020205p12
  - PCB-HV-module BPS series (4 W)
  - \( V_{out} = 0 \text{ to } -4kV / I_{out\text{max}} = 2 \text{ mA} / V_{in} = 11,5 \text{ to } 15,5 \text{ V-DC} \)
  - \( V_{remote/mon} = 0 \text{ to } 5 \text{ V} / V_{I_{mon}} = 0 \text{ bis } 5 \text{ V} / V_{ref} = 5 \text{ V} \)
  - Ripple & noise < 20 mVpp at full load
Setting Voltage resolution 0.3 Volt
16 bit DAC MAX5216

H. Voltage setting repeatability: Set an DAC value (HV) value and apply a sequence of random values, shut down, power off cycles each followed by the setting back of predefined DAC (HV) value and the measurement of the HV → 0.4 Volt

Measurements of the HV output as function of the \( V_{\text{set}} \) both at the HV output and at the \( V_{\text{mon}} \) pin available (KEYTLEY 197A)

Deviation from the set voltage to the measured one
Region A (2000V) \( \sigma < 1 \) volt
Region B \( \sigma \sim 7 \) volt
Discharge evolution time has driven the choice of the ADC Chip
Capability to detect fast transients

Discharges stimulated by increasing the Voltage across a THGEM detector over the breakdown Voltage.
(time resolution: ~2ns)

ADC:
- ADC08500 High Performance, Low Power 8-Bit, 500 MSPS A/D Converter

The ADC board (custom design):
- ADC self-calibration
- multiple ADC synchronization capability
- Low-Pin-Count FMC connector
The Current to Voltage converter scheme and the OPA in transconductance

Current measurement via custom built Picoammeter

(OPA in transconductance)

Based on the Ultralow Input Bias Current Operational Amplifier AD549LHZ

\[ V_{out} = R_F \cdot i \]

1pA~10μV with (10MΩ)

Different feedback resistor has been tested

10 MΩ → 100 MΩ

Good linearity of the system
The Current to Voltage converter scheme and the OPA in transconductance

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\[ V_{out} = R_F \times i \]

\( i \) from 1 pA to 10 μA

Different feedback resistors has been tested

10 MΩ \( \rightarrow \) 100 MΩ

Good linearity of the system

Scaled Voltage \[ \mu V / 10 \]

Good linearity of the system also when coupled with the ADC

Average ADC VALUE sampled at 2.6 KHz for a static current input

Good linearity of the system also when coupled with the ADC
The FPGA Carrier Board: SoC Xilinx Zynq 7000 family

Zed Board based on hybrid Xilinx Zynq-7000

- commercial carrier including high throughput low-pin-count FMC
- Fully Programmable System-on-Chip (SoC) device
- combining a ‘hard’ dual core ARM processor with an FPGA fabric
- dual-core ARM Cortex-A9 processor,
- Programmable Logic: FPGA Artix-7 or Kintex-7 fabric

Second Stage FPGA Soc high-pin-count FMC:

from the commercially demo board to the open hardware FMC carrier based on a Zynq-7030 CIAA ACC

- Open HW, SW programming under VIVADO Package
- More compact design well suited for our application

PCB of 12 layers and a size of 90 x 96 mm.

- Main device: Xilinx Zynq-7000 (XC7Z030-2FBG676I, also compatible with a XC7Z045).
- Memories: DDR3 (1GB), QSPI (128MB).
- Peripherals: SD/SDIO, GEth, USB OTG, 2 x I2Cs, SPI, 3 x UARTs (one RS-485), CAN, Real Time Clock, HDMI.
- GPIOs: 2 x LEDs, 8 x GPIOs, 8 x optical isolated digital IOs (for industrial applications).
- One VITA 57.1 FMC-HPC Connector.
- PCIe/104 connectors (to allow stackable applications).
FPGA design: VHDL code for the Programmable Logic of Zynq

The main purposes of the firmware implemented on the PL of the Zynq device are:

a) Hardware control of the HV DC-DC converter (directly and by mean of DAC)

b) Hardware control of the FMC ADC Board through a high data throughput FMC connector

c) Hardware control of PMOD DAC and ADC Modules

d) Communication Protocol with the PS through the Custom Communication Block

e) Hardware histogram generation for probability distribution analysis using the RAM memory available in the Communication Block.

f) Specific data processing blocks/IP: discharges detection, high-resolution time stamping, oversampling,

PL (FPGA) → Deal with Time critical operation
FPGA design: VHDL code for the Programmable Logic of Zynq

The PS acts as a server TCP/IP for the exchanging of predefined data packets between the Zynq device and a PC. Basically, the PS awaits and fulfills requests from the PC.

a) Reading data coming from PL (FIFO memory) through DMA configuration for data transmission from FIFO to an external DDR RAM memory

b) Packing data from DDR RAM according to PC-Zynq TCP/IP communication protocol specifications

c) Software for managing I2C temperature and pressure sensors.

d) Creation of Protocol Data Unit (PDU) containing header and data for transmission to PC. Unpacking data and fulfill requests from PC according to the information provided by the header of PDUs coming from PC (Middleware)

e) Read and Write into I/O peripheral interfaces via specific predefined ARM memory addresses

f) Communication Protocol with the Zynq-PL through the Custom Communication Block

PS (ARM) \(\rightarrow\) Communication and non Time critical operation
FPGA design: VHDL code for the Programmable Logic of Zynq

FIFO protocol

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And other info related to external sensors
**Test of the prototype: performance**

ADC works @ 500 MS/s @ 8 bit

The current resolution achievable is 62.5nA @ 500 MS/s over a $i$ range of $\pm 800$ nA. Resolution can be increased by

- Oversampling at the cost of reducing the sampling frequency: to gain N bits to obtain a larger ENOB $f_{\text{samp}}$ is scaled by $2^N$ *Decimation Factor*
- Changing the gain of the OPA in transconductance mode

Measurement performed by connecting a 1 current source, the PA and the Keithley 6485 calibrated Picoammeter

**At 100Khz and reducing the dynamic range at $\pm 200$ nA**

$\Rightarrow$ **Effective $i$ resolution** $\sim$ 25 pA vs 17 pA (theoretical one)

Average value of the current histograms at a larger decimation factor (x10,000)
Test of the prototype: performance, discharge tagging

Very simple trigger on discharges by sampling @ 500 MS/s and taking the difference between two samples, if the different is above a threshold → triggered event → save both the timestamp with 2ns time resolution within the waveform.

The Absolute time stamp is given by the sum of the timing of a RT slow Clock and of a fast Clock → Time stamping with 2 ns resolution

Communication via TCP/IP protocol with optical fiber to achieve HV insulation is fundamental

With direct connection we bring the Ethernet port of the PC in an unstable state → freeze the communication
Test of the prototype: performance

Temperature and pressure monitoring fully implemented via IIC ADT7420 and MS5611 sensors → physically connected to the JA1 PMOD

Automatic voltage adjustment of voltage based on the experimental temperature and pressure dependent equation has been fully implemented → PMOD 16 bit DAC MAX5216, MAXIM for HV control

\[ V = V_0 \left( 1 + 0.5 \left( \frac{P}{P_0} \left( \frac{T_0}{T} - 1 \right) \right) \right) \]
Test of the prototype: performance

Temperature and pressure monitoring fully implemented via IIC ADT7420 and MS5611 sensors → physically connected to

Experimental temperature and pressure dependence of gas density

\[ \rho'(0) \left(1 + 0.5 \left(\frac{P}{P_0}\right) \left(\frac{T_0}{T} - 1\right) \right) \]

Automatic voltage adjustment of voltage based on the experimental temperature and pressure dependent equation has been fully implemented → PMOD 16 bit DAC

Also QT Gui version available hopefully soon
Test of the prototype: performance

The HVPSS has been installed and operated during the RD51 October test beam on the hybrid prototype. It was operated on the only non segmented electrode available, namely the Micromegas Mesh.
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\[ G_{\text{eff}} = \frac{I_{\text{meas}}}{C \cdot \text{Rate} \cdot \#e^-} \]

Performed x-check from current measurement by HVPSS (UV LED)

And from amplitude spectra

SPS Super cycle change

Beam Intensity variation

Detector gain variation
Test of the prototype: performance

The HVPSS has been installed and operated during the RD51 October test beam on the hybrid prototype. Due to lack of time it was operated on the only non segmented electrode available, namely the Micromegas Mesh.

HVPSS - spillmonitor

Detector gain variation

Current measured • Current from gain fit
Test of the prototype: performance

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Test of the prototype: performance

The HVPSS has been installed and operated during the RD51 October test beam on the hybrid prototype. Due to lack of time it was operated on the only non segmented electrode available, namely the Micromegas Mesh.
Test of the prototype: next step

Added another feedback resistor to have the possibility to change the I/V converter gain and implement the switching system

Added a high precision temperature sensor on for the Operational Amplifier since we have observed a T dependence

New board will also include the 10 kV OC100HG HV opto-coupler to apply “fast cut procedures” on HV

Start to work for the multi channel system

Network of FPGA (PTP protocol on TDM network....)

The goal is to have a 7 channels system working for the end of the year

Thanks!
Spares