SRS VMM readout for Gadolinium GEM-based detector prototypes for the NMX instrument at ESS

Michael Lupberger
(now University of Bonn, presented work carried out in CERN GDD group)

MPGD2019, La Rochelle, 07.05.2019
Outline

● Introduction: What is SRS?
● SRS with the VMM ASIC
  - Implementation
  - Applications
● R&D for the NXM instrument at ESS
  - Detector prototypes
  - Test beams with SRS VMM
● Conclusion
What is SRS?

Scalable Readout System:
A generic readout system for laboratory and detector instrumentation developed and supported by the RD51 Collaboration since 2009
(Inventor: H. Müller)
What is SRS?

Front-end ASIC(s)

Hybrid
Hybrid
Hybrid

HDMI/optical links specific protocol

Detector

Detector
What is SRS?

Front-end ASIC(s)

Master only

Detector

Master/Slave

Adapter card

Hybrid

8x1

Hybrid

Adapter card

Hybrid

8x1

Hybrid

Adapter card

4x2

Hybrid

HDMI/optical links specific protocol

Detector
What is SRS?

- FEC Adapter card
- 8x1 Hybrid
- 8x1 Hybrid
- 4x2 Hybrid
- HDMI/optical links specific protocol
What is SRS?

- **SRU** (Service Request Unit)
  - 1 GbE data, trigger, clock, control links (CAT5)
  - 40x

- **FEC Adapter card**
  - 4x2

- **Front-end ASIC(s)**
  - Master only
  - Detector
  - Master/Slave

- **10 GbE data**

- **Trigger**

- **HDMI/optical links specific protocol**
What is SRS?

- **PC**
  - 10 GbE data
  - Ethernet switch
    - 1 GbE data, control (CAT5)
  - CTGF card
    - Clock & trigger generator fan-out (CAT5)

- **SRU**
  - 1 GbE data, trigger, clock, control links (CAT5)
  - 40x

- **FEC Adapter card**
  - 1 GbE data, trigger, clock, control links (CAT5)
  - 8x1

- **Master only**
  - Detector

- **Master/Slave**
  - Detector
  - 4x2
  - HDMI/optical links specific protocol

- **Front-end ASIC(s)**
  - 10 GbE data, trigger, clock, control links (CAT5)
  - 8x1

- **Trigger**
  - Master only
  - Detector
  - Master/Slave
What is SRS?

- Trigger: 10 GbE data
- PC: 1 GbE data, trigger, clock, control links (CAT5)
- Ethernet switch: 1 GbE data, control (CAT5)
- CTGF card: Clock & trigger generator fan-out (CAT5)

Example AVP25 (strip readout) up to:
- 82k ch/SRU
- 2048 ch/FEC
- 128 ch/hybrid + (master/slave)

Front-end ASIC(s):
- Hybrid
- Master only
- Detector
- Master/Slave

HDMI/optical links specific protocol

8x1

4x2
What is SRS?

1 GbE or DDTC to SRU

10 GbE SFP+

40x DDTC from FECs

FECv6 (2013)

FECv3 (2010)

Virtex-6

CTGF v3

Virtex-5
SRS and front-end ASICs

Different ASICs are implemented in SRS:

- APV25 (backbone of MPGD R&D)
- Beetle
- VFAT
- Timepix
- SiPMs

Ongoing:

- Timepix3
- VMM (future backbone, as APV25 is discontinued)

Future:

SAMPA (by/with Sao Paulo group)
Reminder: VMM front-end ASIC

Talk by George Iakovidis from Monday: VMM3a, an ASIC for tracking detectors

- 130 nm CMOS technology
- 64 input channels, each w/ preamplifier, shaper, peak detector, several ADCs
- Pos. & neg. polarity sensitive
- Digital block w/ neighbouring logic, FIFO, multiplexer
- Adjustable gain 0.5-16 mV/fC
- Adjustable shaping time from 25 ns – 200 ns
- Input capacitance from few pF – 1 nF

VMM developed for the ATLAS NSW upgrade by BNL
Reminder: VMM front-end ASIC

Talk by George Iakovidis from Monday: VMM3a, an ASIC for tracking detectors

- Internal test pulser with adjustable amplitude
- Global threshold & adjustment per channel
- Self-triggered, zero suppressed
- 38 bit per hit

(if input charge goes over threshold)

1. Event flag (1 bit)
2. Over threshold flag (1 bit)
3. Channel number (6 bit)
4. Signal amplitude (10 bit)
5. Arrival time (20 bit)

VMM developed for the ATLAS NSW upgrade by BNL
Implementation of the VMM ASIC in SRS

Project in Gaseous Detector Development group at CERN

- funded by EU BrightnESS and AIDA2020 project and the detector group of the European Spallation Source (ESS)
- Project driver: NMX instrument at ESS
- Benefit for whole RD51 community and beyond
- Goal: replace SRS APV as backbone for MPGD R&D
  - VMM will become available with general purpose SRS
  - THE readout for the next decade within the community
  - Application beyond the community
  - Application beyond R&D → experiments
Implementation of the VMM ASIC in SRS

Hardware: Prototyping completed, transition to industrial production, establish QA, supply teams
Firmware: ready for small systems, basic features, used test beam, continuous further development
Software: DAQ, slow control, monitoring tools merging into new SRS VMM DAQ

More details on the system status: RD51 WG5 session on Friday morning
## Future SRS VMM users and interested groups

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*: not yet approved

- Wednesday
- Friday
- Monday
- Poster #37
- Today afternoon
- This talk

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*This talk*
The European Spallation Source ERIC

- Multi-disciplinary research center based on world’s most powerful neutron source
- Pan-European project hosted by Sweden and Denmark
- Research facility currently under construction in Lund
- Data Management and Software Centre located in Copenhagen (Denmark)
The European Spallation Source ERIC

- 12 founding states + 1 new member: Czech Republic, Denmark, Estonia, France, Germany, Hungary, Italy, Norway, Poland, Spain, Sweden, Switzerland and the United Kingdom
- 2 observer states intend to become member states in near future: Belgium and the Netherlands
The European Spallation Source ERIC
The NMX instrument at ESS

Illustration taken from https://europeanspallationsource.se/
NMX detector prototype

Demonstrator v0 “Zita” by Patrik Thuiner @ CERN

Cross-section
NMX detector prototype
Demonstrator v0 “Zita” by Patrik Thuiner @ CERN

ESS Detector Group Seminar 30.08.2018: P. Thuiner, NMX Zita - Building the the NMX detector prototype v0
https://indico.esss.lu.se/event/1100/
NMX detector prototype
Small (10 cm x 10 cm) prototype tests with VMM readout

Budapest Neutron Center (July 2018)
NMX detector prototype

Small (10 cm x 10 cm) prototype tests with VMM readout

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Neutron transmission through Cadmium mask
Holes: minimum separation (center to center) of about 2.0 mm horizontally, 1.6 mm vertically, and 1.3 mm diagonally.
NMX detector prototype

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Small (10 cm x 10 cm) prototype tests with VMM readout

Institut Laue–Langevin D-16 (October 2018)

Not in picture:
Viviana Cristiglio
Olivier Aguettaz

Slide: Patrik Thuiner, GDD meeting 17.10.18

Esko Oksanen
Patrik Thuiner
Detector Franz
Michael Lupberger
Dorothea Pfeiffer
NMX detector prototype

Small (10 cm x 10 cm) prototype tests with VMM readout: ILL

Experimental setup

HV drift
HV GEMs
10 x 10 cm² active area
cooling
boron shielding
diffraction sample

neutron beam
1.451 Å

wax stopper
crystal
sample holder
saturated vapour

TPI w/ 2PG inhibitor
crystal

powder
sample holder

YIG powder in container

3 mm diameter B4C diaphragm

Slide: Patrik Thuiner, GDD meeting 17.10.18
NMX detector prototype

Small (10 cm x 10 cm) prototype tests with VMM readout: ILL

Crystal diffraction spot

YIG powder diffraction rings

Preliminary data analysis by Dorothea Pfeiffer

Results obtained within ILL beam time proposal *Demonstration of high position resolution Gd-GEM detectors for macromolecular crystallography*, doi:10.5291/ILL-DATA.1-10-39
Conclusion

- VMM ASIC has been implemented in the Scalable Readout System within the BrightnESS project, outcome is a prototype system

- VMM was correct choice by RD51 due to flexible configuration

- Application of the system now starts!

- NMX prototype was a pioneer and the driver for the project

- Looking forward to fully instrumented “Zita” NMX demonstrator
The End

Thanks for your attention
SRS APV

APV25 ASIC: Readout chip for CMS tracker
- 250 nm CMOS technology
- Delivered: 2001
- Configuration via I2C
- 128 channels with preamp and shaper
- Output: multiplexed analogue levels
- 40MHz clock

APV25 hybrid:
- One APV25 ASIC
- PLL
- LDO for power
- Master/Slave
- Protection circuit

Adapter card:
- Mainly ADCs
- Can read up to 16 APV25 hybrids

S. Martoiu et al., Development of the scalable readout system for micro-pattern gas detectors and other applications, JINST 8.03 (2013), C03015
SRS APV

1) Detection and imaging of high-Z materials with a muon tomography station using GEM detectors

2) Performance in Test Beam of a Large-area and Light-weight GEM detector with 2D Stereo-Angle (U-V) Strip Readout

3) GEM-based polarimeter detector development for storage ring EDM experiment
S. Park, Presentation given at the AFAD2018, Jan 2018.

4) Development and test of the DAQ system for a Micromegas prototype installed in the ATLAS experiment

5) Performance studies under high irradiation of resistive bulk Micromegas chambers at the CERN Gamma Irradiation Facility

6) Characterization of triple-GEM detectors for the Phase I Muon System Upgrade of the CMS Experiment at LHC

7) More than 100 systems sold via CERN store
SRS APV - Drawbacks

- ASIC is more than 15 years old
- Low trigger rate $O(10\ kHz)$
- Low data rate due to multiplexed analog output of ASIC
- Limited input capacitance range $< 50\ pF$
- Limited gain range
- No zero suppression in ASIC (only on FEC)
- Export restrictions
- No new production of the ASCI CERN store stock $< 600$ hybrids

⇒ New ASIC implementation required
SRS APV

Maximum trigger rate with special firmware: 5 kHz

(K. Gnanvo @ RD51 Collaboration Meeting Aveiro 2016)
SRS Beetle

Common project with ATLAS NSW before VMM was available

Project had to be stopped

- ACTEL FPGA proposed for radiation hardness – could not be verified
- Company could not deliver hybrids due to problems with four row wire bonding
SRS VFAT

RD51 VFAT hybrid

Not successful:
- too much noise
- wrong information from designers

→ abandoned

But...
SRS VFAT

TOTEM DAQ upgrade
VME based electronics in LHC phase 1
for VFAT opto carrier board

SRS for phase 2:
- trigger rate 1 kHz → 24 kHz
- Zero suppression
- L2 hardware algorithms in FEC

SRS Timepix

Implementation in framework of feasibility study for a pixel-TPC at ILC → InGrid/GridPix readout

SRS SiPM

NEXT readout system

SRS in ATCA, upgrade for next White detector

Implementation of the VMM ASIC in SRS

Status

Hardware components:

- SRS FEC: general SRS component → ✔
- Hybrid: 4 v3 (VMM3, VMM3a), 4 v4 (VMM3a, final), 20 v4 (VMM3a) from industrial test production → ✔
- Adapter Card: 8 prototypes, 2 final version prototypes →

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- Redesign into VMM DAQ ongoing with CERN EP-DT-DI →

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Integration
- Single FEC (4 hybrids) used at many test beams → ✔
- Multi-FEC systems not tested →