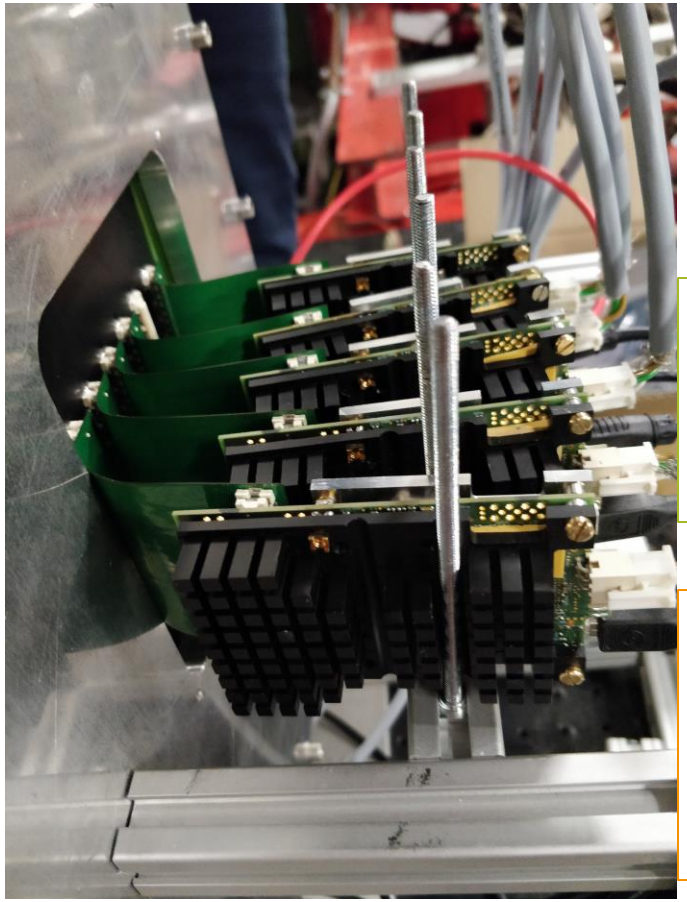
PLAYING WITH VMM3 IN MAINZ

Stefano Caiazza

ELECTRONICS

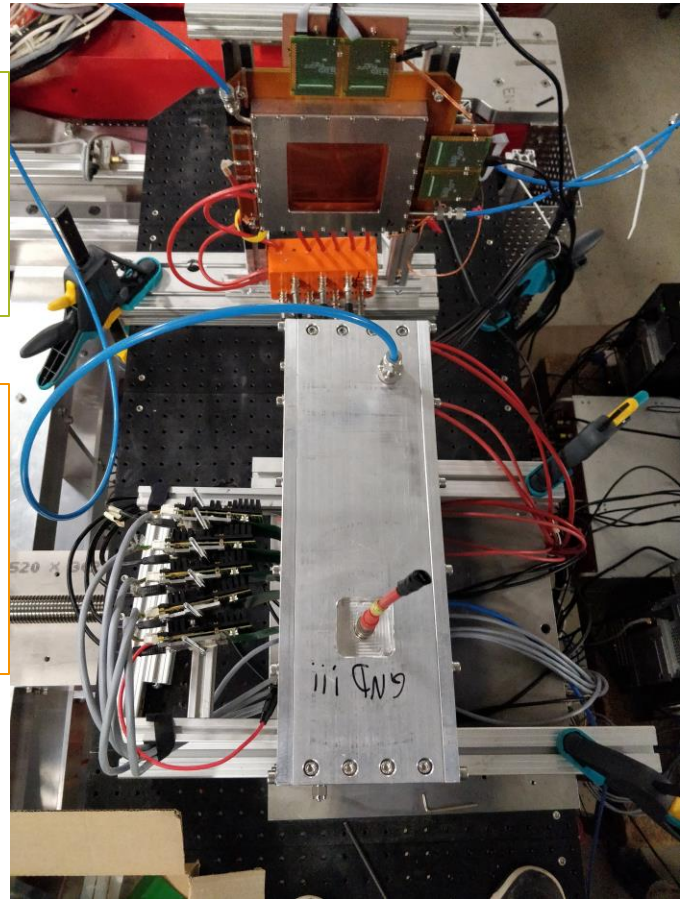


One of the main users of SRS VMM

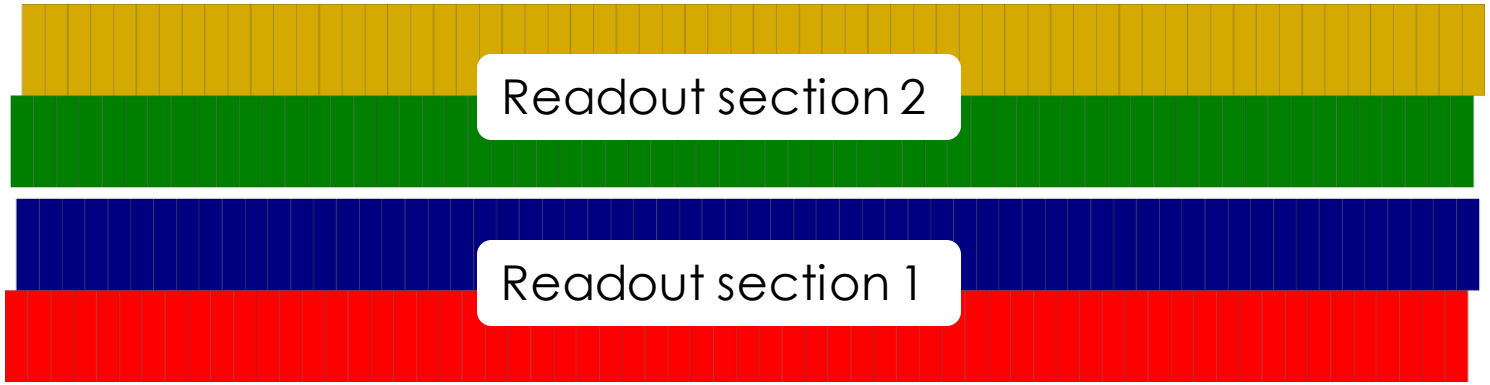
- Each detector needs at least 7680 channels
- 120 VMM3a per detector in 60 hybrids

VMM development

- First test-beam with TPC and VMM completed on May 4th at MAMI in Mainz
- SRS DAQ software to share within RD-51 under development



SMALL PROTOTYPE SETUP



Readout plane

- 12 rows of 64 pads covering a bit more than a 10x10 cm^2 surface
- Rectangular pads 2x8 mm^2
- Modular layout with 128 channels readout section routed to an HiRose connector
- 6 readout sections cover the entire sensitive surface

Drift and amplification

- 3 GEM stack
- 8 cm drift region
- Argon-$C0_2$ 70-30
- Operated as a TPC

VMM PREPARATION

Available materials

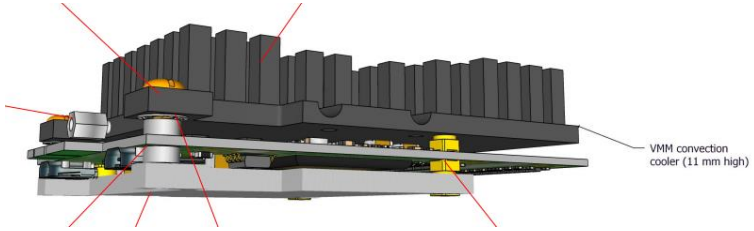
- 1 VMM hybrid with assembled cooling kit and 3 VMM hybrids with cooling kit components on loan from CERN
- 1 assembled hybrid with 1 broken ASIC and 2 test hybrids without cooling kit from M. Lupberger
- VMM power connectors
- Instruction manual from H. Muller

VMM Hybrids assembly

- About 1 hour per VMM to assemble the cooling kit (can be improved with a bit of experience)
- An hour to assemble 6 power cable

Additional required devices

- Full SRS with Minicrate, FEC, DVM card and HDMI cables
- 1 Low voltage power supply
- 1 JTAG programmer to load the firmware in the FEC



DVM CARD ASSEMBLY

The problem

- Only a few DVM card v4 prototype were available, difficult to obtain and only for short term
- The final DVM card, v5, is not yet production ready

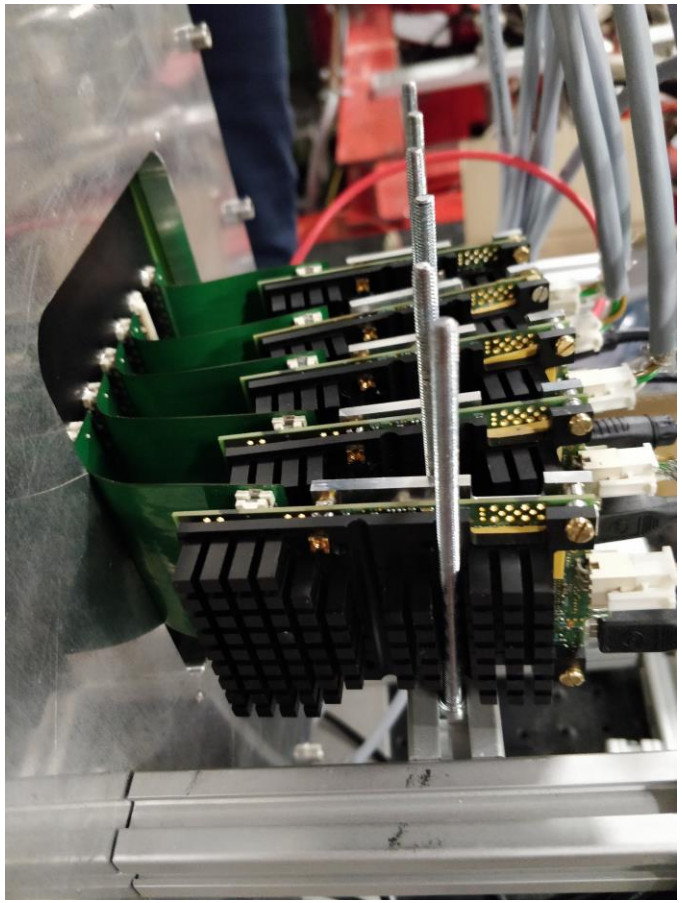
In house production and assembly

- Layout provided by H. Muller to order the PCB
- Components ordered according to the modified BOM provided by M. Lupberger
- Assembly of 4 DVM cards with the pick-and-place machine of the electronics workshop of the KPH institute in Mainz
- Assembly completed on April 17th 2019

DVM card testing

- 1 card used during the test-beam with up to 5 VMM.
- We couldn't yet do a systematic testing due to the time constraints but at least 4 of the HDMI connections worked without problems for a few days in beam, a couple seemed to be unstable

TESTBEAM OPERATION



Up to 5 VMM installed

- Reinforced Kapton cable adapter to connect the hybrids perpendicularly to the readout
- Support structures in the cooling pipe grooves
- The cooling kits are a bit too thick for our current design, we may have to reduce the radiator thickness

General consideration

- A good grounding is very important, much more than for the APV
- The new connectors are mechanically very stable
- The cooling kits allow very stable operations with just a large fan even for compact installations
- The integration of the hardware components is almost plug-and-play. Load the firmware, connect everything, power up the system and the data start flowing

FIRMWARE

General notes

- JTAG programmer and Xilinx (free) ISE tool to program the FEC FPGA
- The ISE tool is old and not supported on W10 (but there is a workaround) but it's the only one supporting the Spartan6 FPGA

Triggering firmware

- New firmware M. Lupberger wrote in 2 days for our testbeam
- The VMM are self-triggered so it's difficult to sync them with other detector and with external triggers
- We wanted to take data in parallel with our APV-based standard detector
- The new firmware inserts a marker in the data stream for each received trigger so that the systems can be synced

SOFTWARE

ESS software tools

- Borrowed the ESS software tools for this test beam
- Quite functional in the operation but not the easiest to setup as it was created for a much more complex environment

SRS DAQ software

- Started an RD51 project for a common SRS DAQ software in 2018
- Currently a bit stalled due also (on my part) to the lack of hardware to work with
- Most of the framework is ready and now I can implement the working parts to make a simple working system that can be used by all SRS users