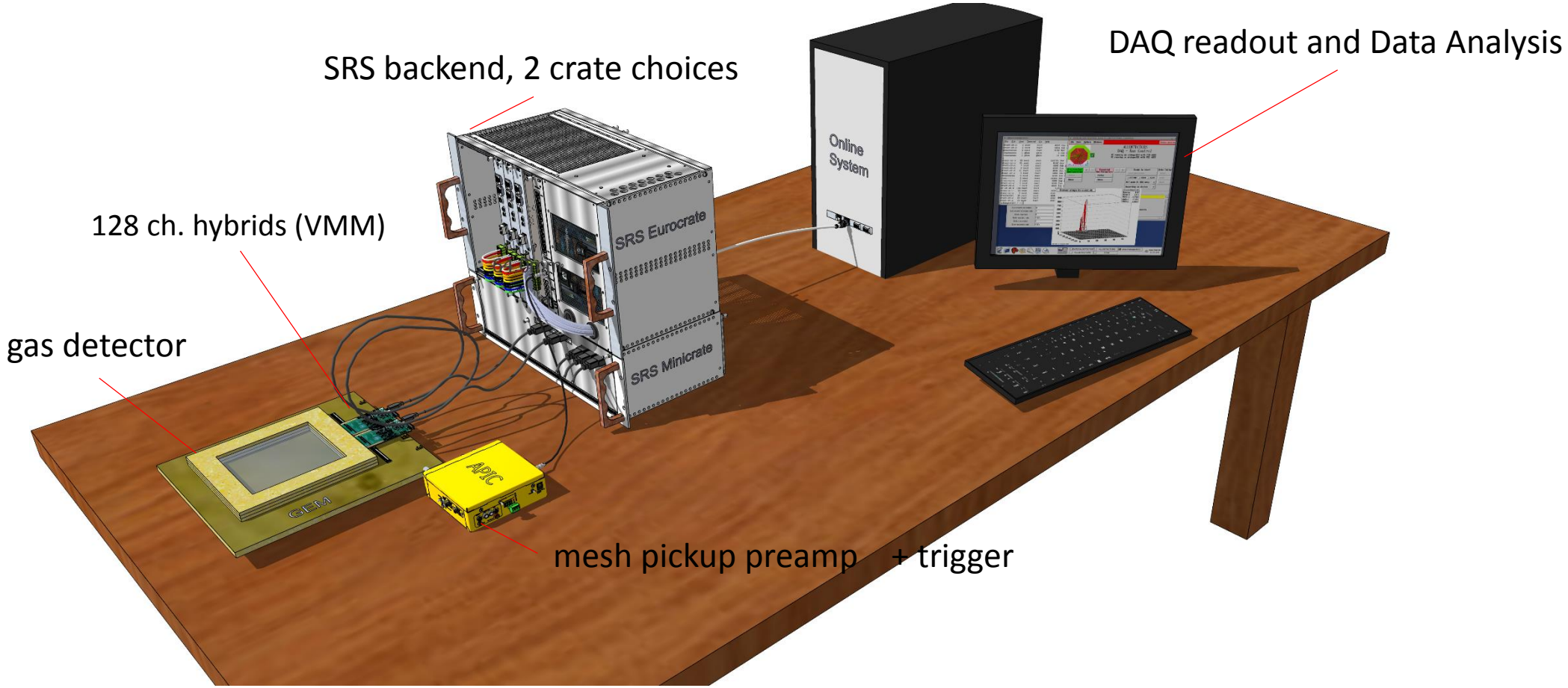
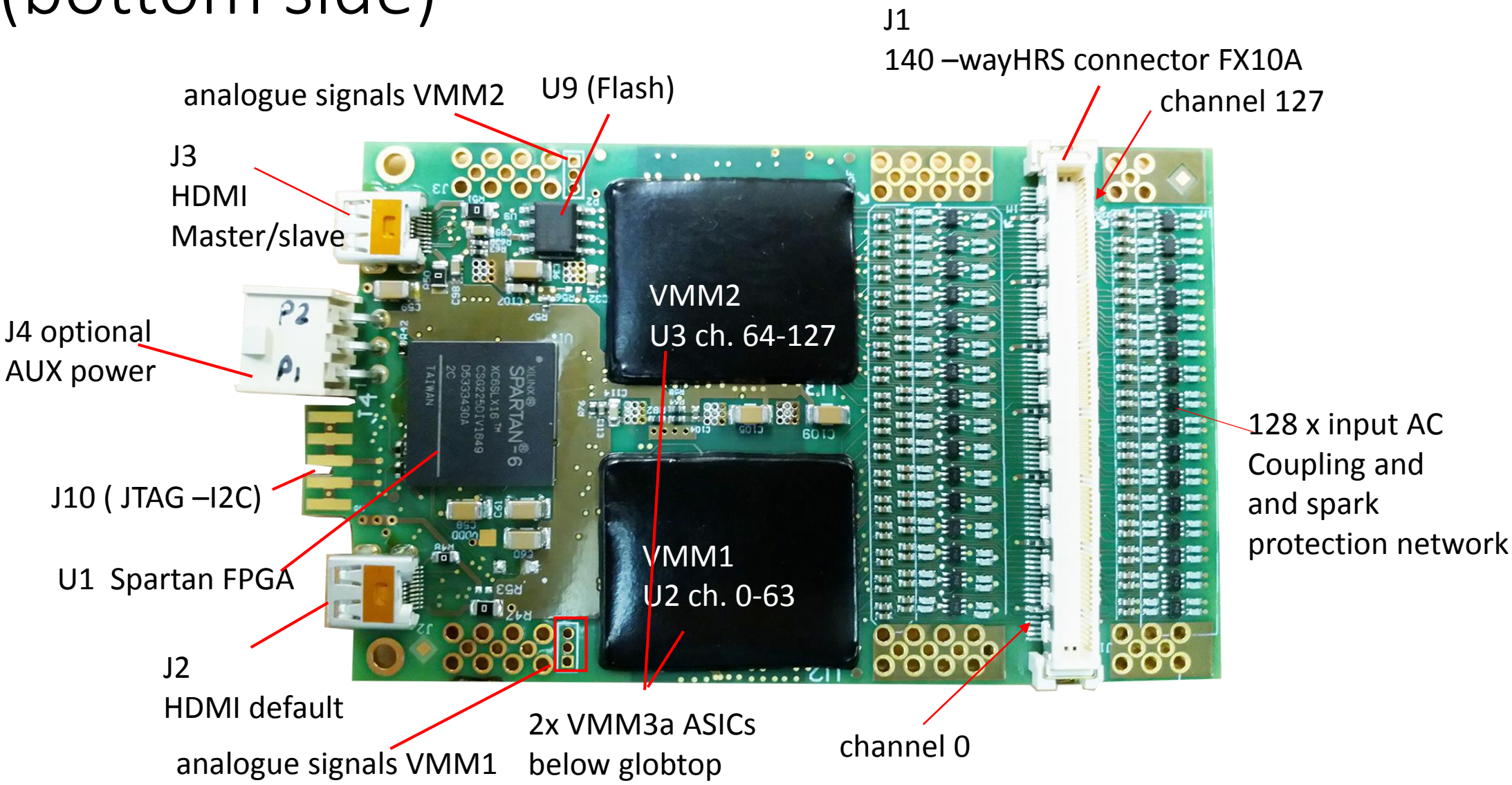
# “SRS for the VMM era”

## Status of Mai 2019, GDD lab CERN

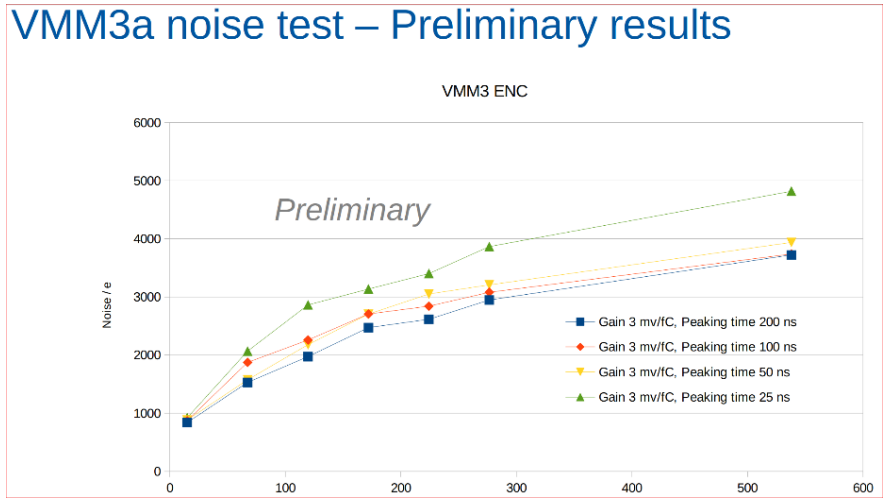


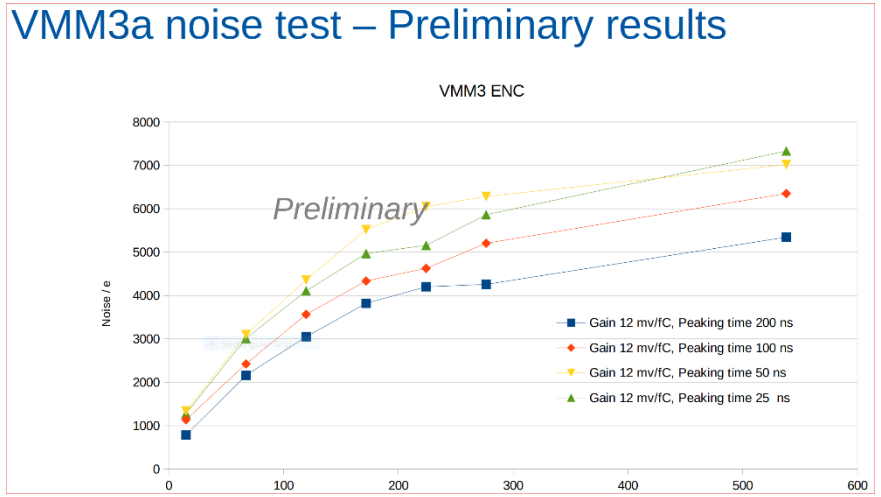
# SRS hybrid V4.0 commercial 2019 (bottom side)

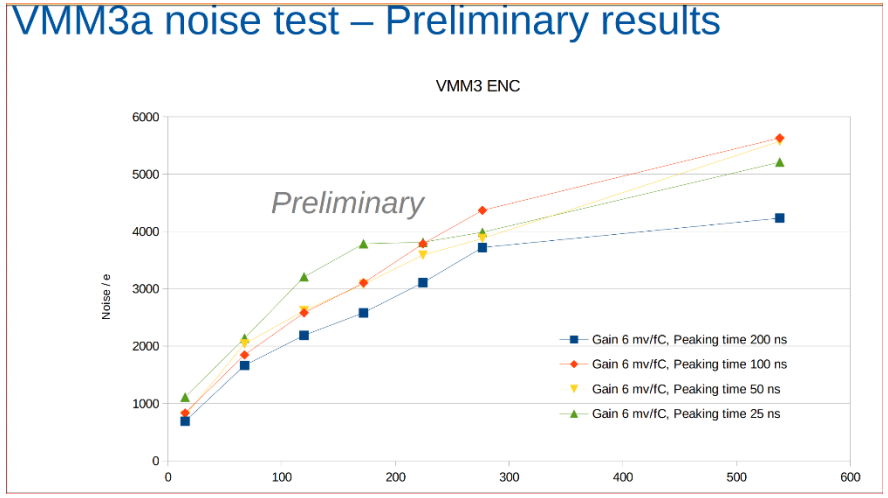


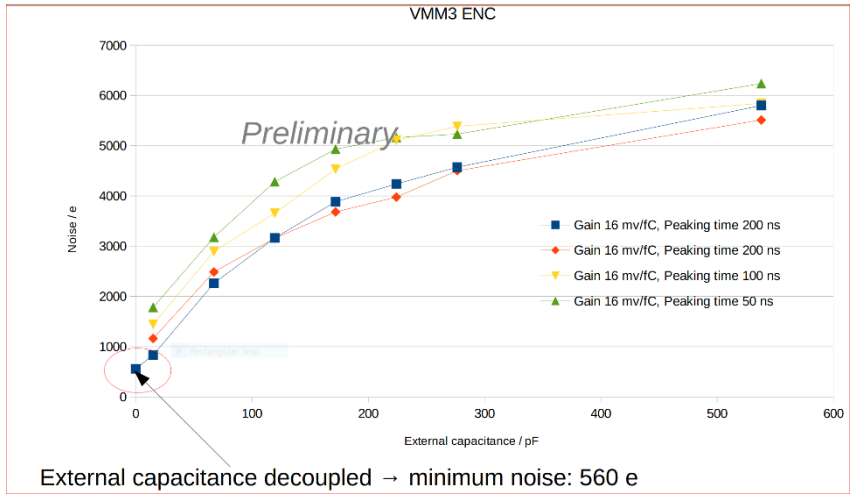
# ENC noise measurements VMM3 SRS hybrid

as function of detector capacity* see WG5 https://indico.cern.ch/event/702782/




**ENC minimal with:**

- low gain
- high peaking time
- low detector capacity

**Minimum ENC for Zero –pF detector: 560 e-**

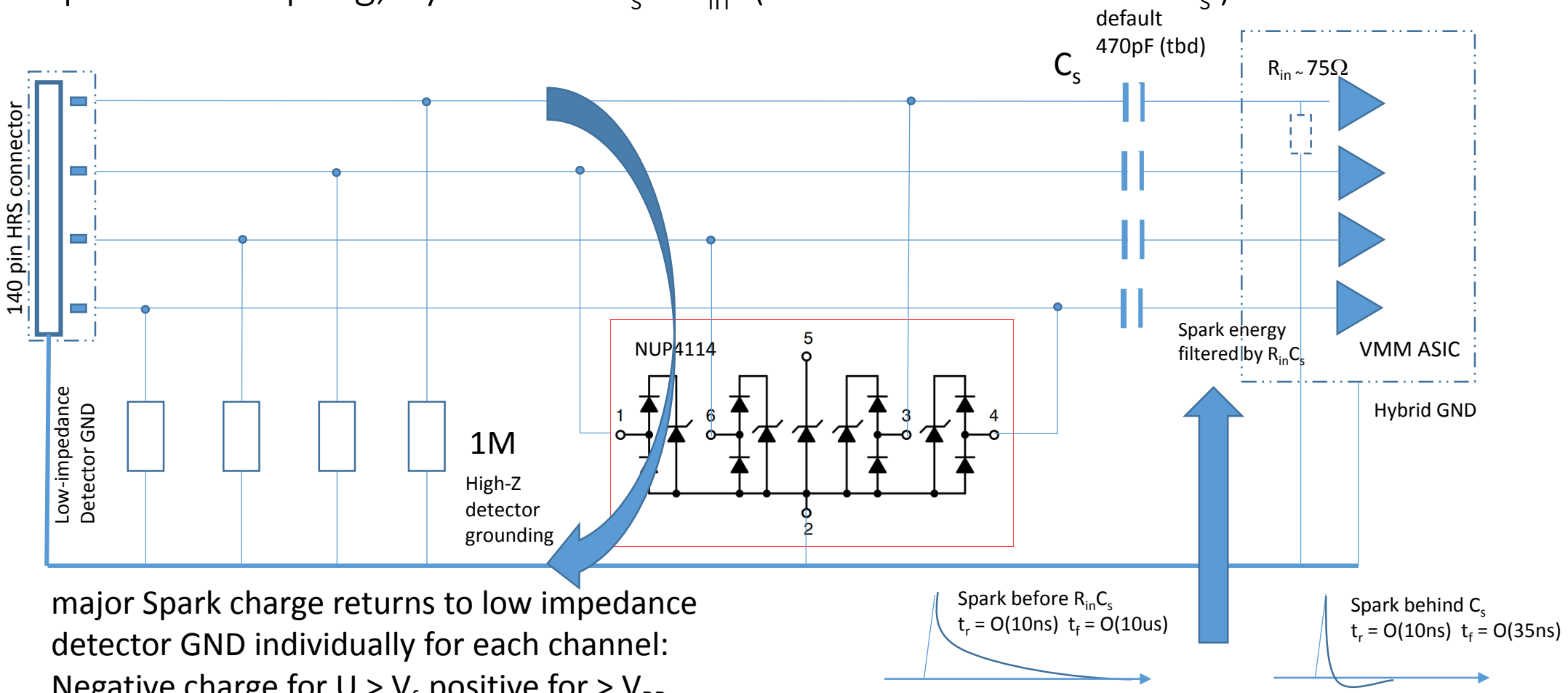
**ENC maximal with:**

- High gain
- low peaking time
- high detector capacity

**Maxium ENC for Cdet=520pF: 7300 e-**

# Spark energy mitigation

capacitive coupling, by default $C_s$ x $R_{in}$ ( ~ 35 ns with default $C_s$ )*

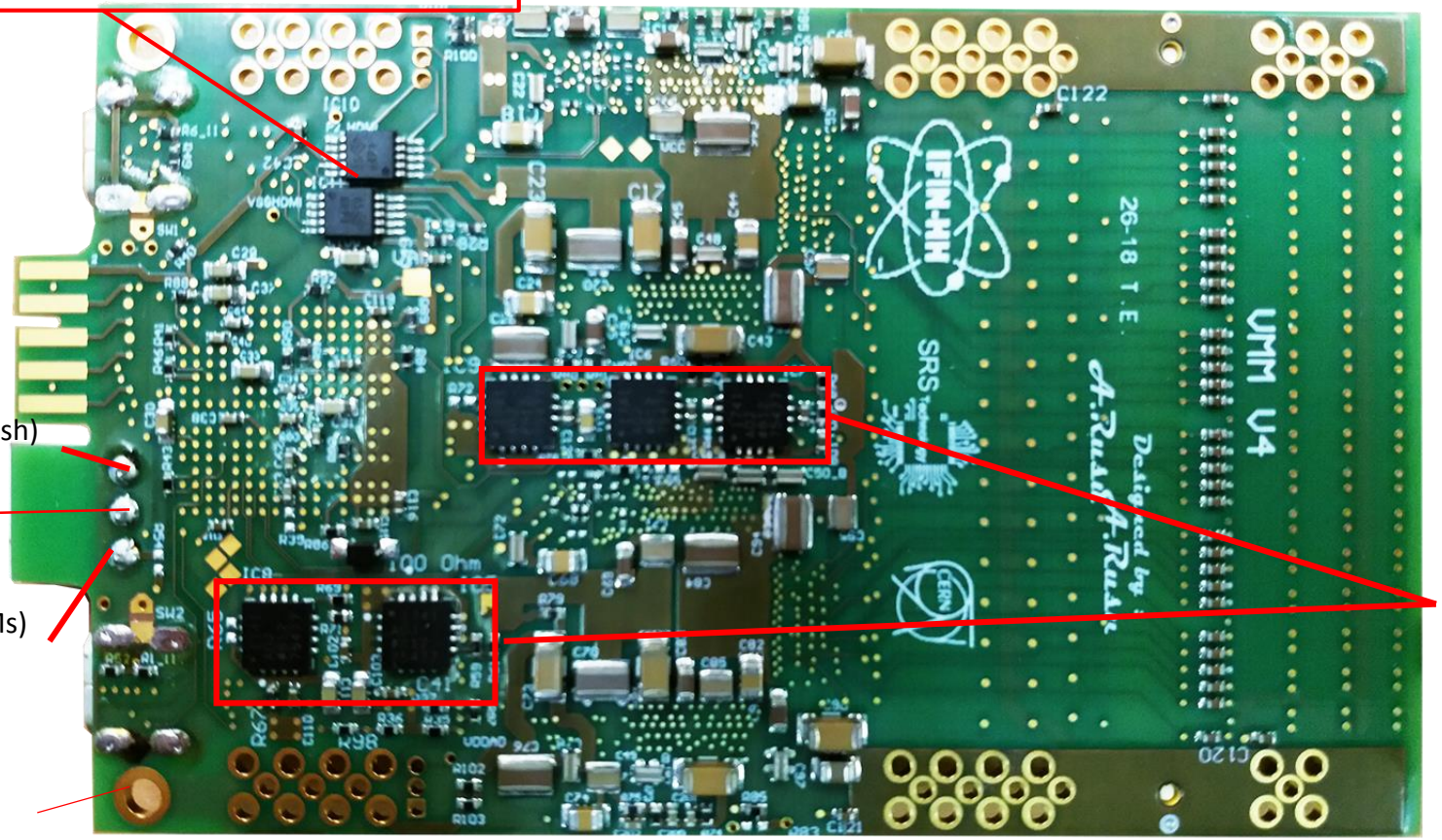



major Spark charge returns to low impedance detector GND individually for each channel:
Negative charge for U > $V_f$ positive for > $V_{BR}$

*$C_s$ are discrete mounted capacitors, custom values or Zero Ohm to be indicated before production

# SRS hybrid V4.0 2019 (top side)

uADCs ADS1015, 12 bit 4 channels ( readout via I2C)
Connected to PDO, PTO, MO analogue lines on P1,P2
IC10 - U2 VMM1 I2C Adr . 1
IC11 - U3 VMM2 I2C Adr. 0




Power input P1 ( FPGA, Flash)
Min. 2.9 V

GND

Power input P2 ( VMMs)
min 1.8V

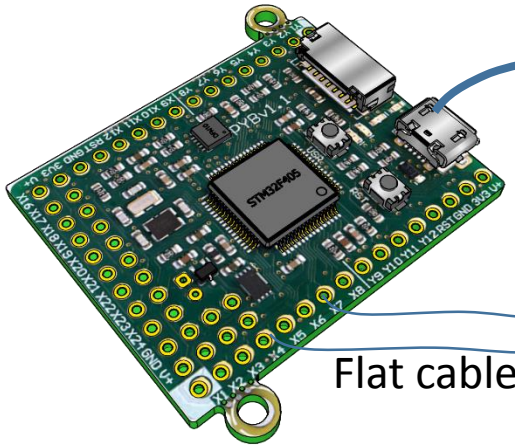
GND hole

LDOs: IC5-9 are 2-Ampere
CMOS LDO's of type
ADP174ACPZ-R7
IC7 VDPP, 1.2V , 150 mA preamplifiers
IC6, VDD, 1.2V, 400mA analogue section
IC9, VDDAD, 1.2V 200mA , ADC's
IC5, VDD, 1.2V 150 mA,Digital +SLVS drivers
IC8, VAUX, 2.5V, 150mA, FPGA and Flash

# ID chip in Rev 4.1

Putty window

uPython board PYBv1



USB

3V power*
2.5V AUX
SCL,SDA 2.5V
GND

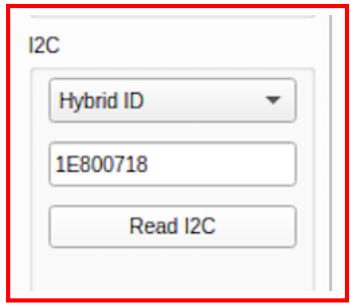
Flat cable

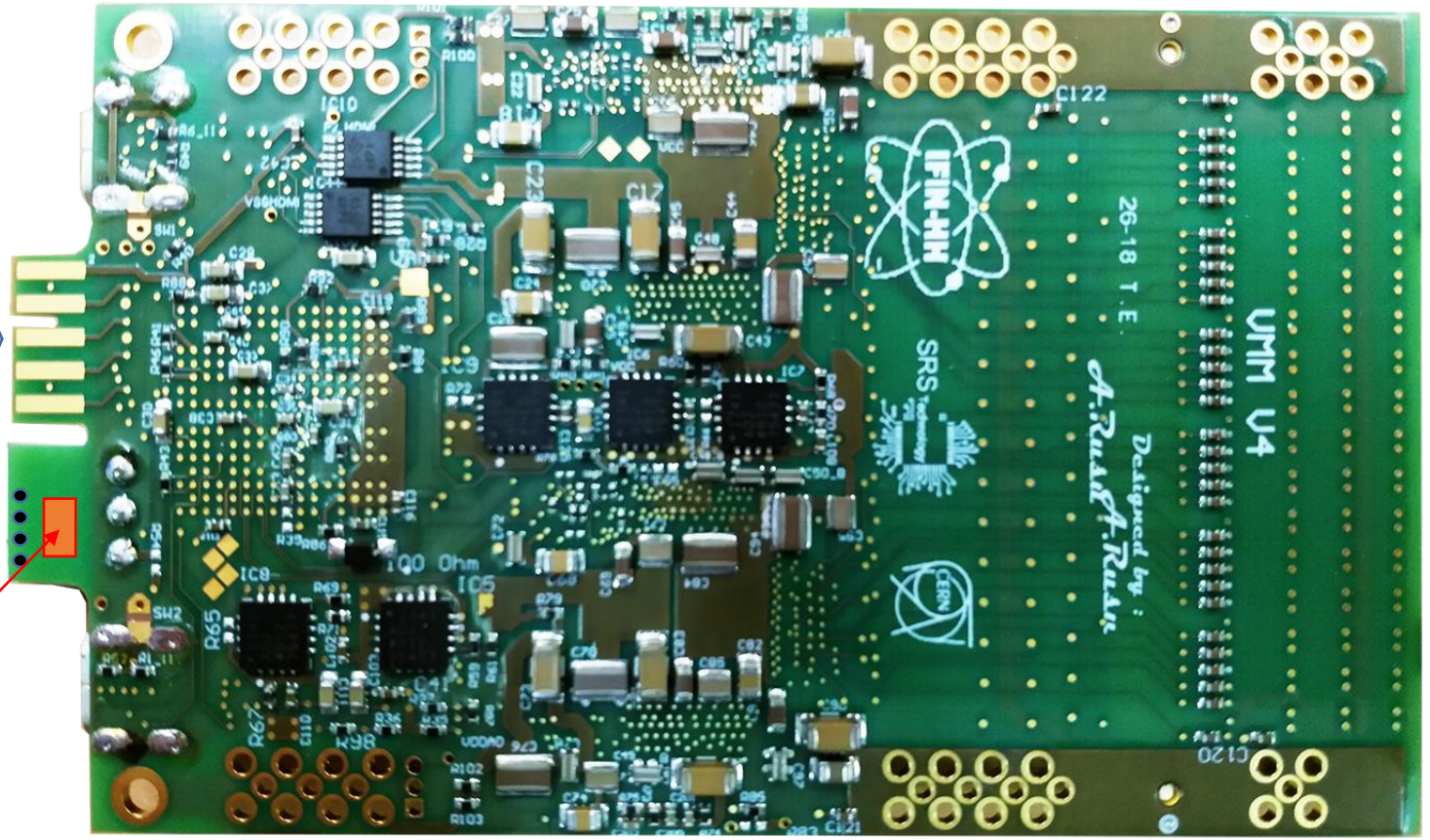
New small programming adapter PCB

1.) Unique 128 bit ID for VMM hybrids
- user readable via standard software (new I2C address )
- production readable via Python testcard

1. - integrated into VMM3 slow control

2.) Default VMM configuration at Power up
- VMM in default status after power-up
- programmable via Arduino likes



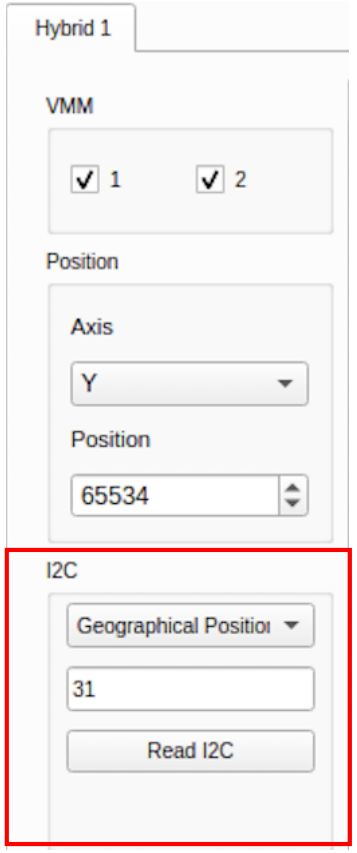




## ID chip

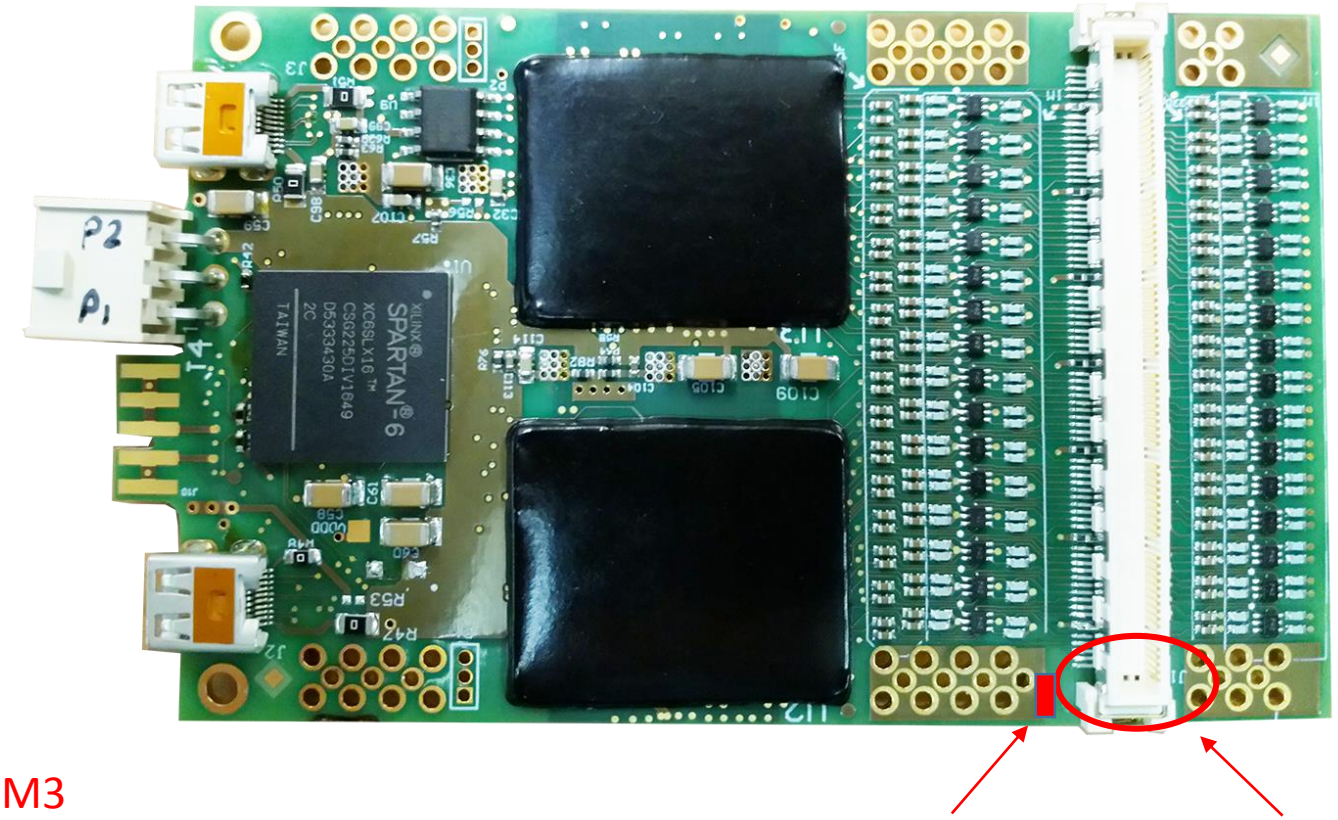
**I²C-Compatible (2-wire) Serial EEPROM with a Unique, Factory Programmed 128-bit Serial Number**
**1-Kbit (128 x 8), 2-Kbit (256 x 8)**

*for testing via python board, only P1=3V is needed, leave P2 without power

# Geographical Position readback in Rev 4.1

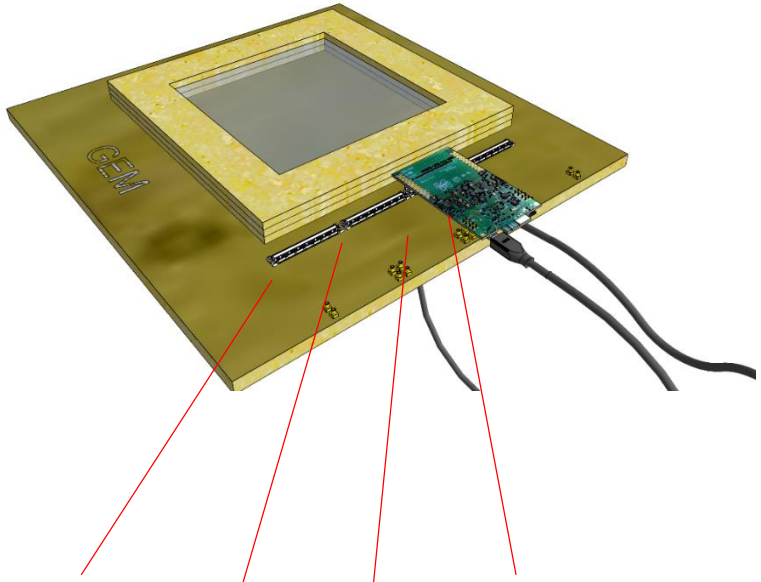



Integrated in VMM3 slow control




Pullup resistor array

HRS connector pins 1-6




0x00 – 0x01 – 0x02 -0x03 ….
Pin coding on detector

readback via I2C also possible
In-situ via Python card
An unconnected hybrid reads back as “11.1111”

# Test: readout geographic position

```
>>>        test 4 read geographic address from  I2C register via Pyhon board
>>>        for this test, a fixed GEO address is wired <P7:P0> = b0011.0001
>>>
>>> i2c.mem_write(0x0,33, 0x00)    # Set pointer to input register 0x00 at device addr 33
>>> i2c.mem_read(1, 33, 0x00)      # read 1 byte from 8 bit inputregister = GEO address
b'1'
>>> bin(_[0])                      # convert to binary
'0b110001'                         # read back correctly fixed GEO address
>>>
```

# Upcoming VMM functionalities (Firmware)

## VMM functionality wishlist

1.) add 6 bit geographical hybrid- position readout ( tested OK, available from Rev4.1)

2.) add VMM ID chip and direct serial readout adapter ( tested OK, available from Rev 4.1)

3.) add default VMM Configuration at Powerup ( New EEprom tested, requires FW update)

4.) spill-buffer mode ( DDR3 in FEC ) (implemented: DDR firmware of Yan to be integrated in DAQ mode, to do: 8 resistors on FEC have to be modified)

5.) Consolidate DVM-card channel numbering to agree with front panel (implemented in latest firmware and slow control versions)

6.) add ART = Fast-OR & Mask to FEC -NIM output ( new feature in DVM 5.1, requires FW update)

7.) add fast VMM global counter reset via double Trigger-> 1st step to spatially distributed SRS systems

8.) add Atlas-mode level-0 trigger mode ( so far emulated at FEC level, requires major FW update )

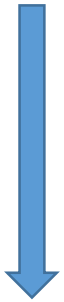
9.) stabilize readout at highest trigger rates ( >= 1MHz , better understand and fix lockup effects)

10.) add configuration download mirroring from VMM chips ( alive test, required FW update)

11.) add powerbox MasterSlave and dual BW modes (FW updates when box becomes available)

12.) Consolidate DVM-card channel numbering in slow control to agree with front panel

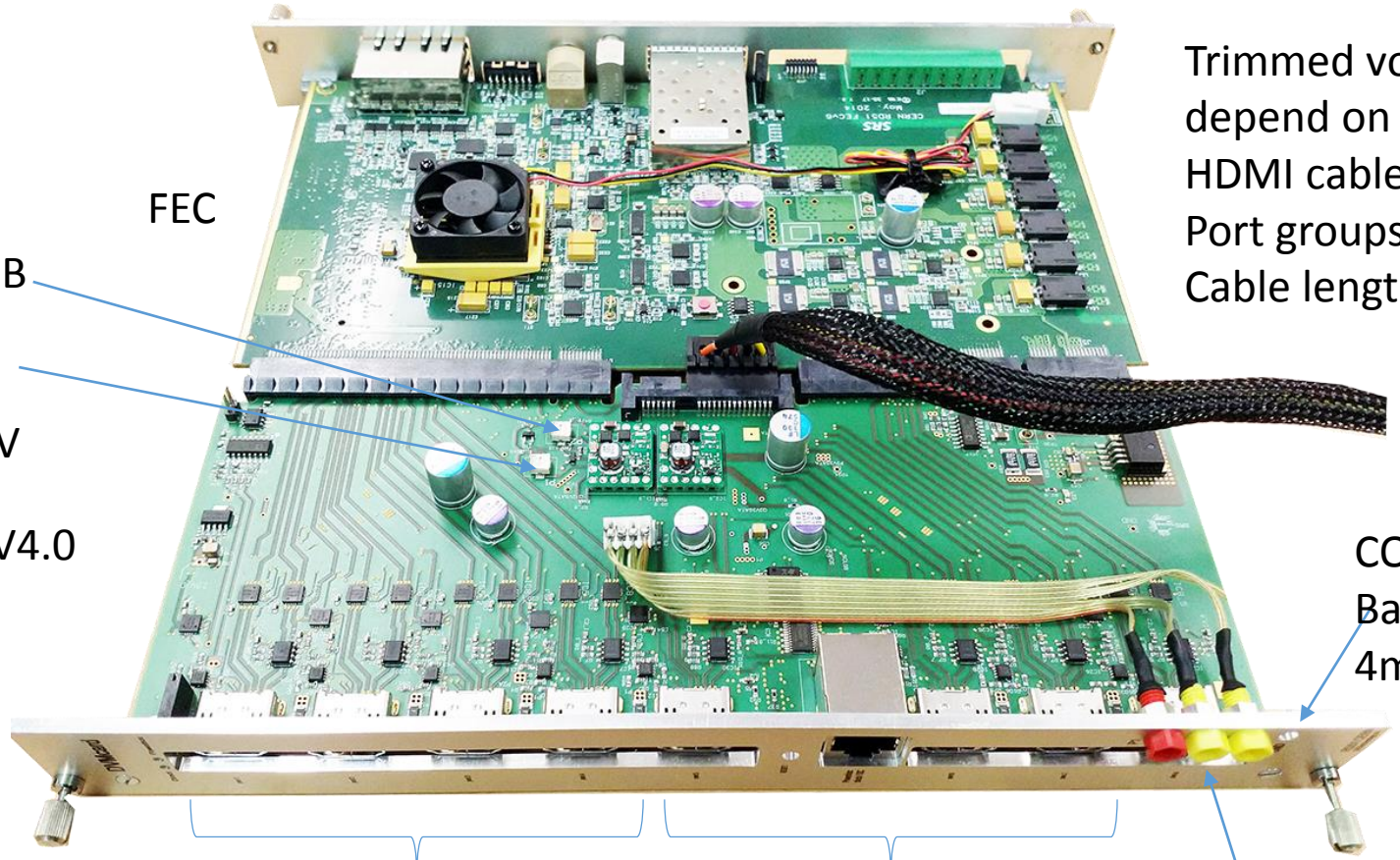
13.) tell us more ….



# HW- Upgrade VMM V4.0 -> V4.1 (June 2019 )

- increase PCB thickness to 1.6 mm by adding 1 layer
  - JTAG –I2C programming connector (new) requires 1.6 mm for making good contact
- add 64 bit ID chip with 2kbit EEprom on back of Powerconnector pad
  - unique serial Number via I2C readout
  - 1728 bit configuration code loading at powerup
  - I2C readout of serial Number and programming of default config file via Python /USB card
- increase diameter of 2 GND fixing holes to 3.1 mm, increase GND collar
  - passage of M2.5 screws for top/bottom cooler plates with some slack, good thermal contact
- reduce footprint of all MMCX connectors for more precise positioning
  - higher precision of MMCX centre required for fixation of VMM cooler
- add geographic code of hybrid position on a detector, readable via I2C
  - add two I2C programmable lines to spare pins of HRS connector
- add measurement of VMM supply voltages P1 and P2 to the 2 spare channels of the micro ADC's

# New DVMcard V4.1 ( fully tested OK)



FEC

Trimmer Voltage P2- B

Trimmer Voltage P2- A

2.7..4V

DVMcard V4.0

Trimmed voltages P1 and P2
depend on
HDMI cable length.
Port groups A and B must use same
Cable length.

SATA cable 12V , 3.3V

COMMON GND plug
Banana 4mm
4mm2 copper cable to detector

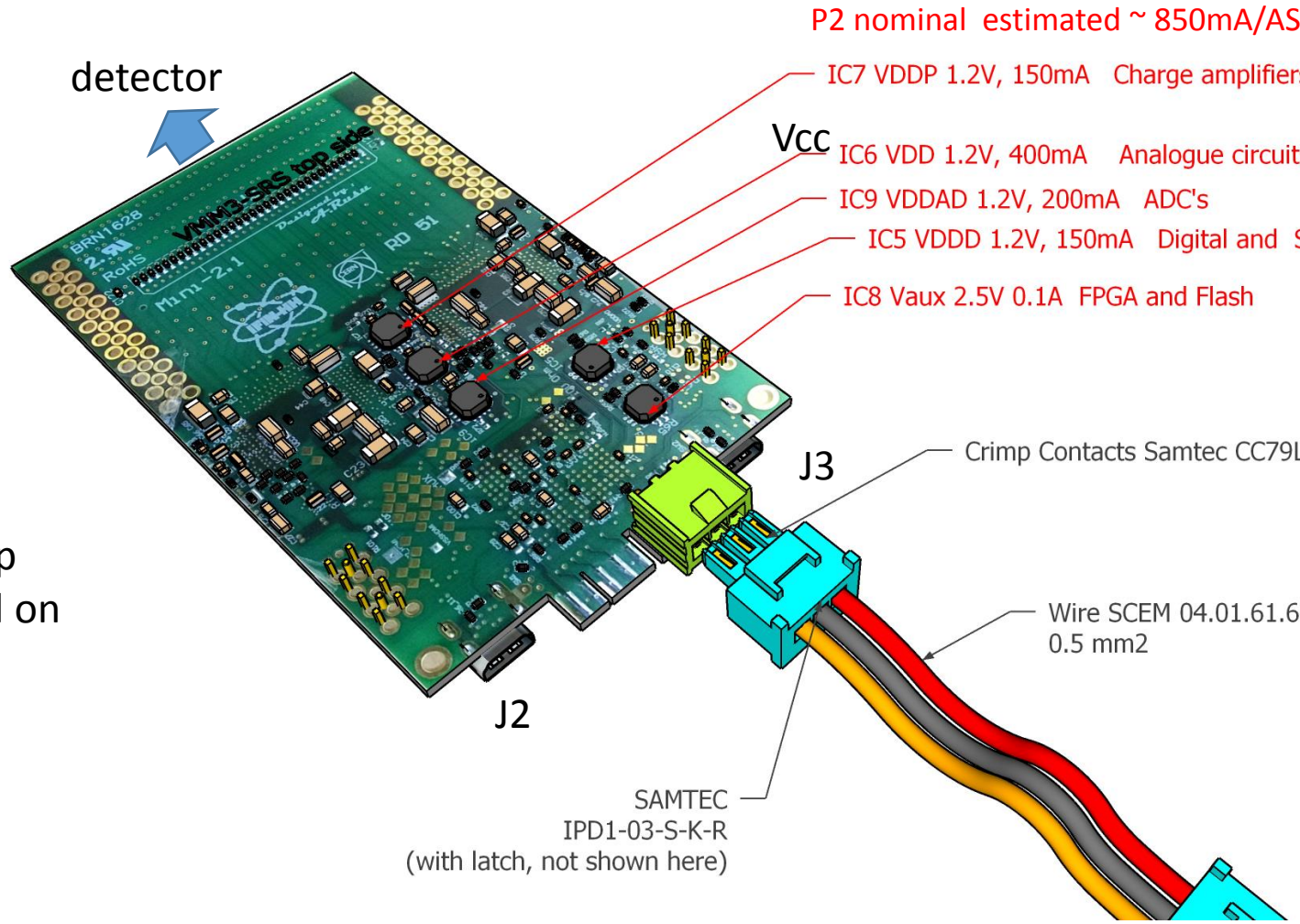
4 x HDMI ports A

4 x HDMI ports B

P1 and 2 x P2 Voltage monitoring

# Direct Hybrid Power (optional)

## if used, SATA cable must be removed from DVMcard




Note: IC5-9 are 2-Ampere CMOS LDO's of type ADP174ACPZ-R7

Note: IC6 has highest power dissipation and is hotter than the other LDO's

View from top when plugged on detector.

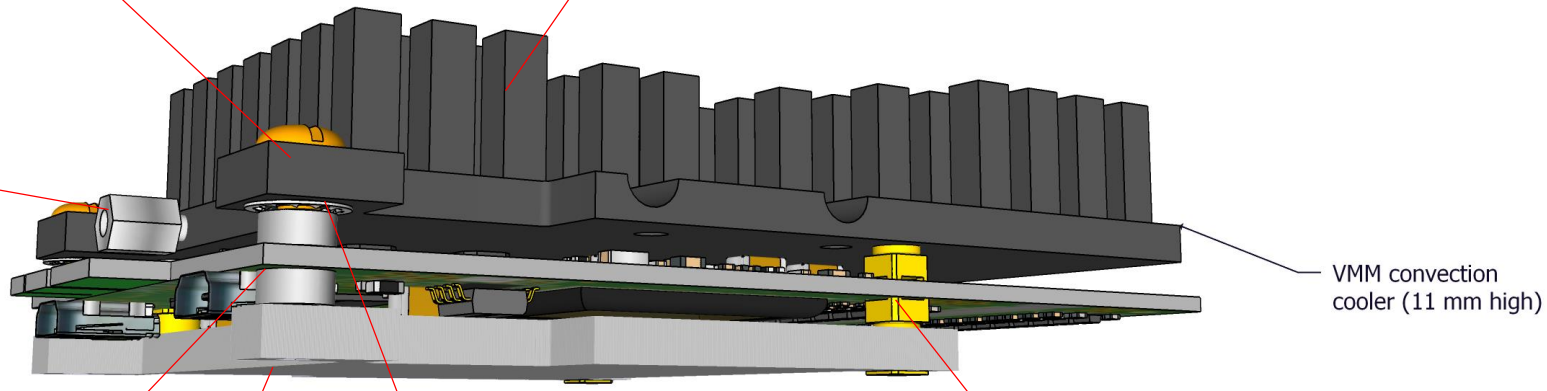
<u>Note:</u>
The auxiliary power cables/connector shown here are optional. By default VMM hybrids get powered via the HMDI link to the DVMcard or Powerbox

# Convection cooler

M2.5 traversing screw
12 mm , brass, bombhead

Top cooler:
Radian
CRN001 CUSTOM 77.5X50X13MM SQUARE PIN HEAT SINK

Hex spacer M2 x 8
GND cable contact



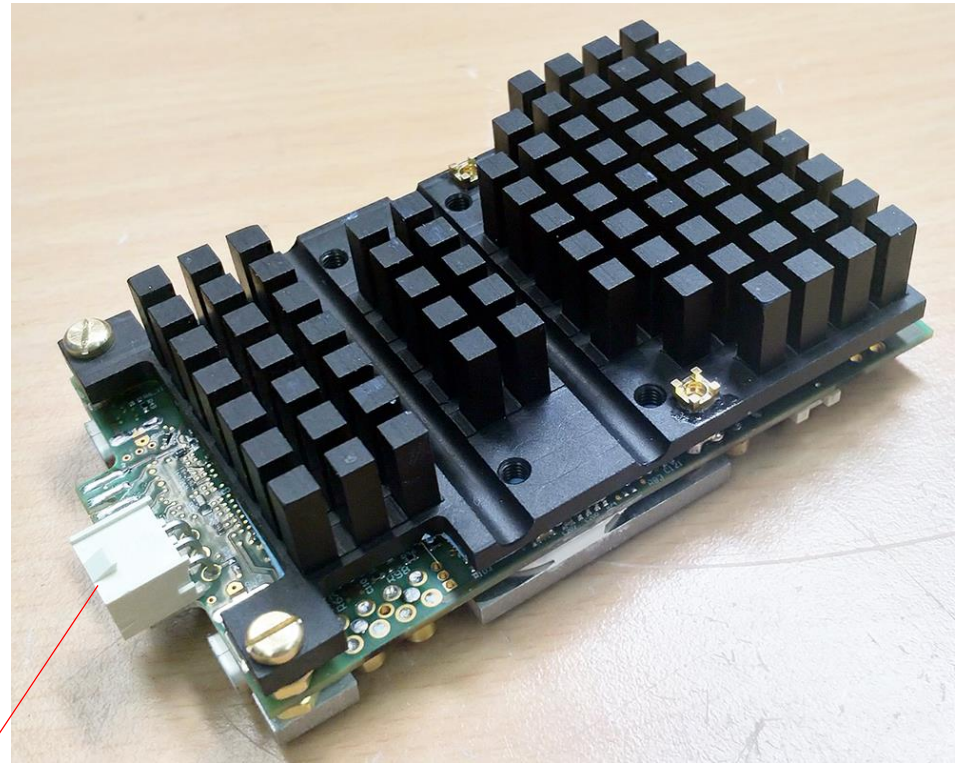

M2.5 x 2 mm spacers

Bottom cooler
M2.5 taphole

M2.5 tooth-washer
0.5 mm thick

MMCX click-in shells
on T/B cooler plates:
pressfitted into 3.40 dia holes
On PCB: soldered both sides into same MMCX footprint

# Photos Top (left)  bottom (right)

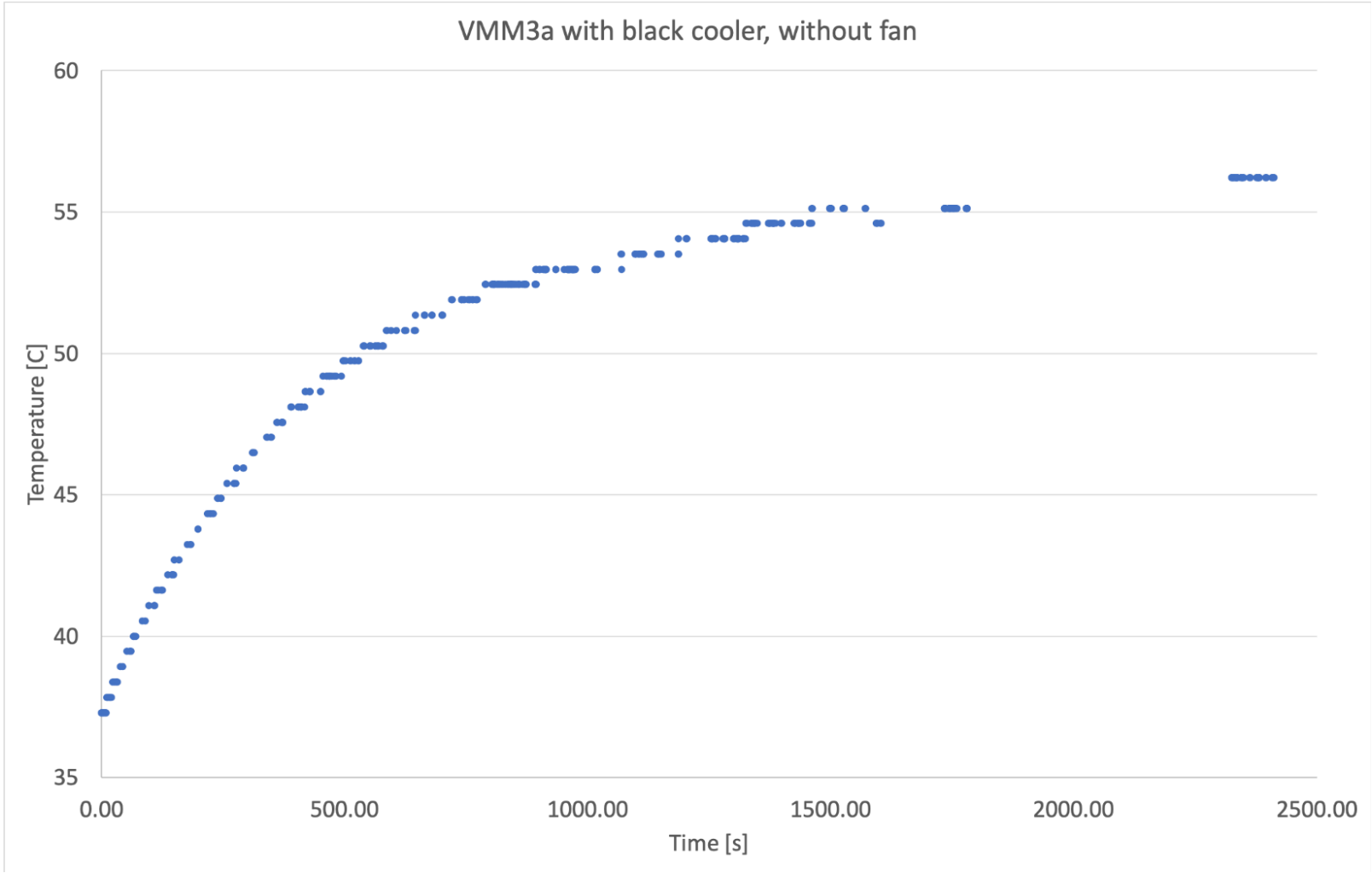


Note 3:
these MMCX shells
are optional
not mounted
by default

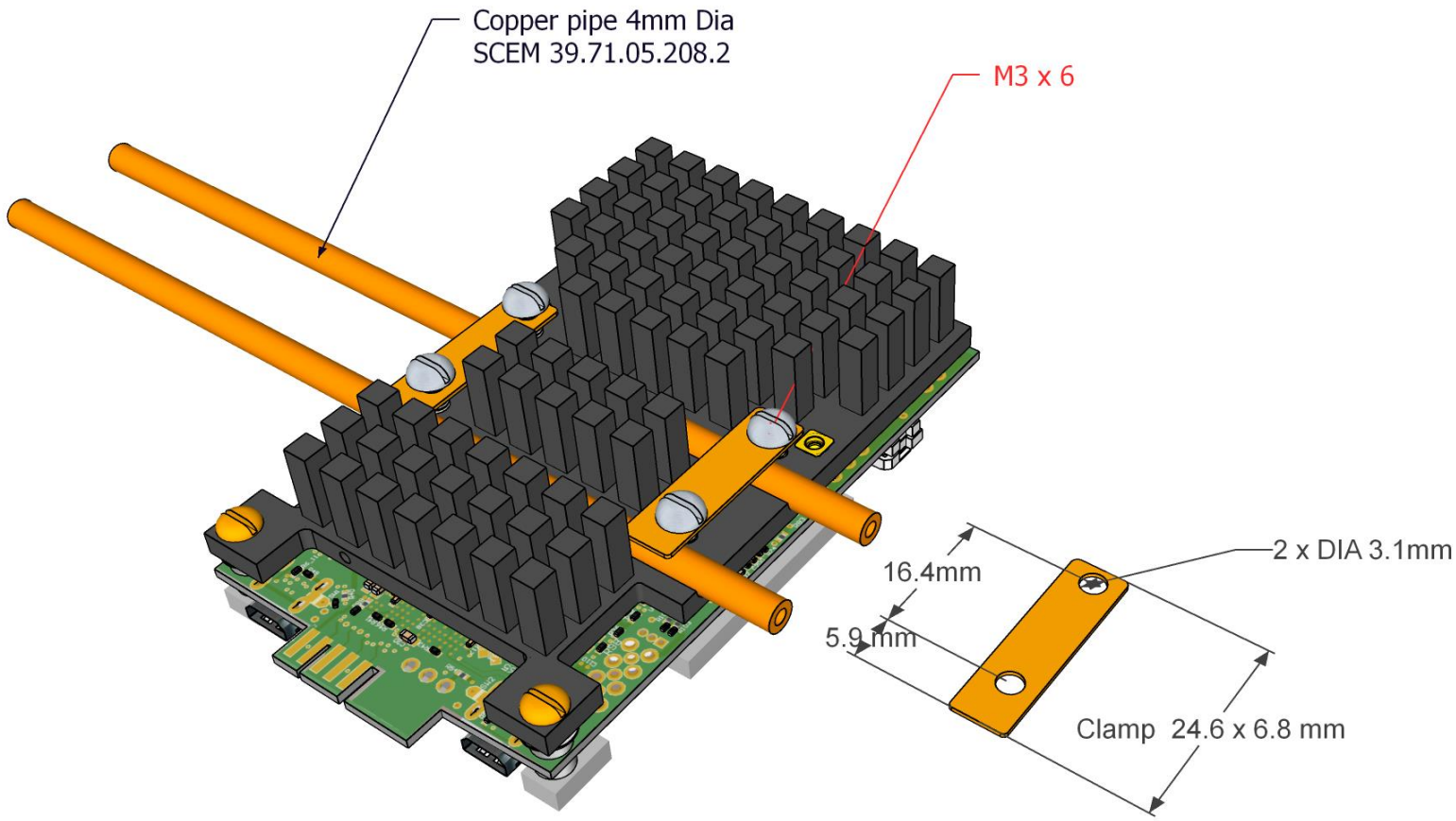
Note 2: these MMCX –J-P-H-ST-SM1  true coax connectors are optional,  not mounted by default

Note 1: power connectors are optional, not mounted by default

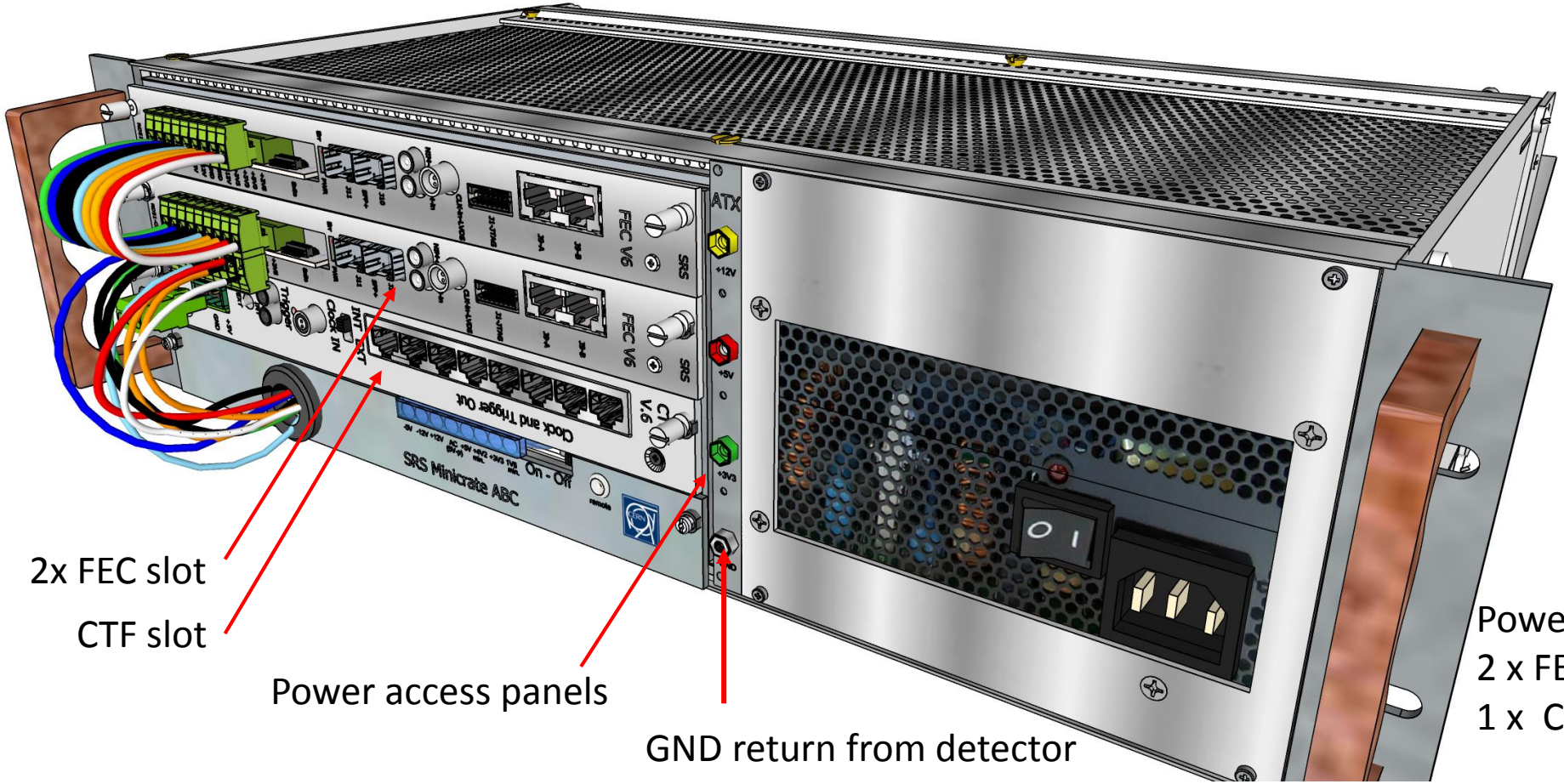
# VMM3a core temperature  with black convection cooler



# Water cooling option



# New Minicrate ABC*
## for VMM3 frontend with direct HDMI power




Max Nr. channels

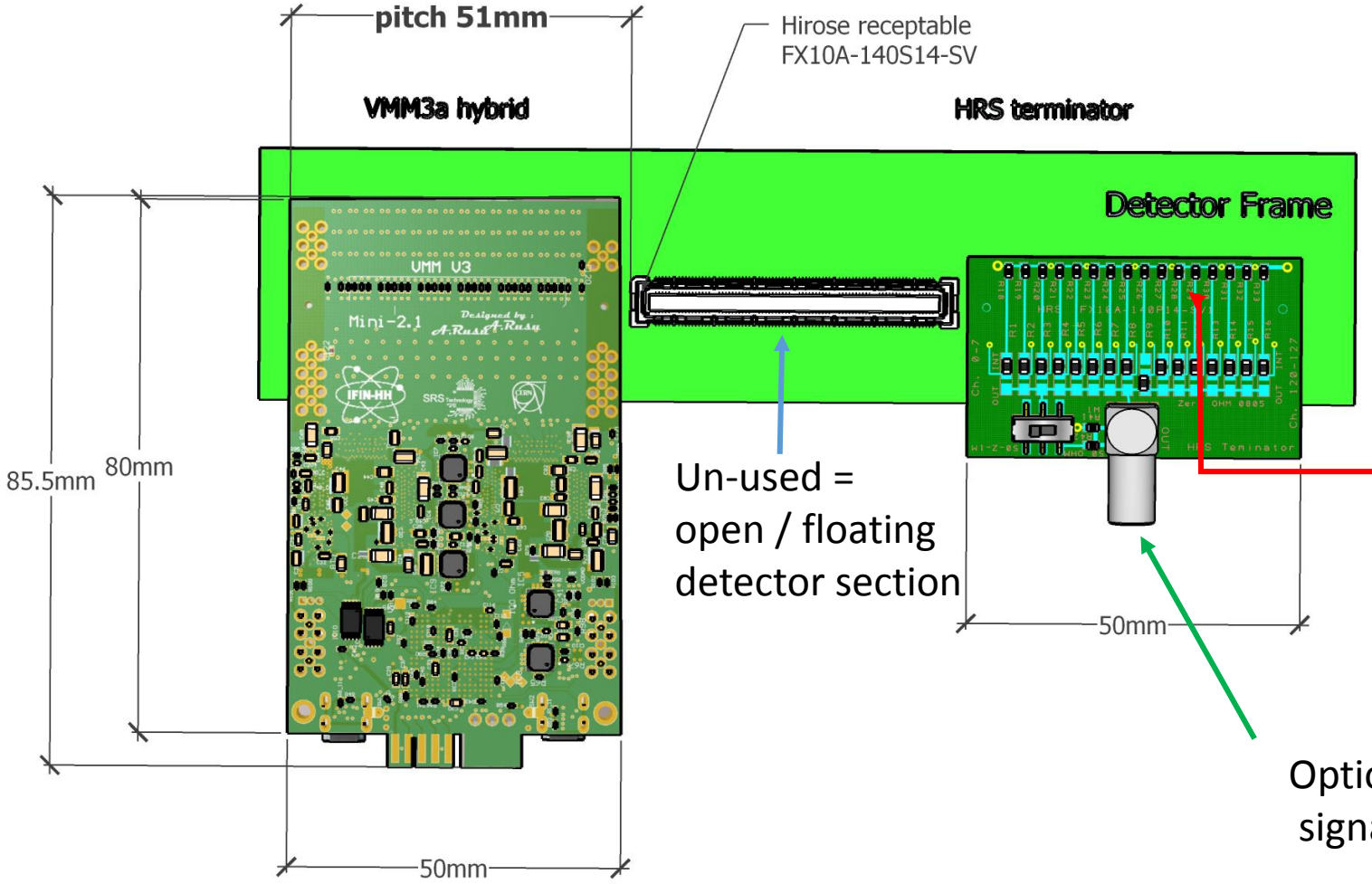
Direct HDMI power
16 VMM hybrids = 2K

Master/Slave Powerbox
32 VMM hybrids = 4K

Power and slots for:
2 x FEC + DVMcard
1 x CTF (clock and trigger fanout)

* links to construction/upgrade documents on request

# HRS terminators primarily for unused HRS slots on a detector frame



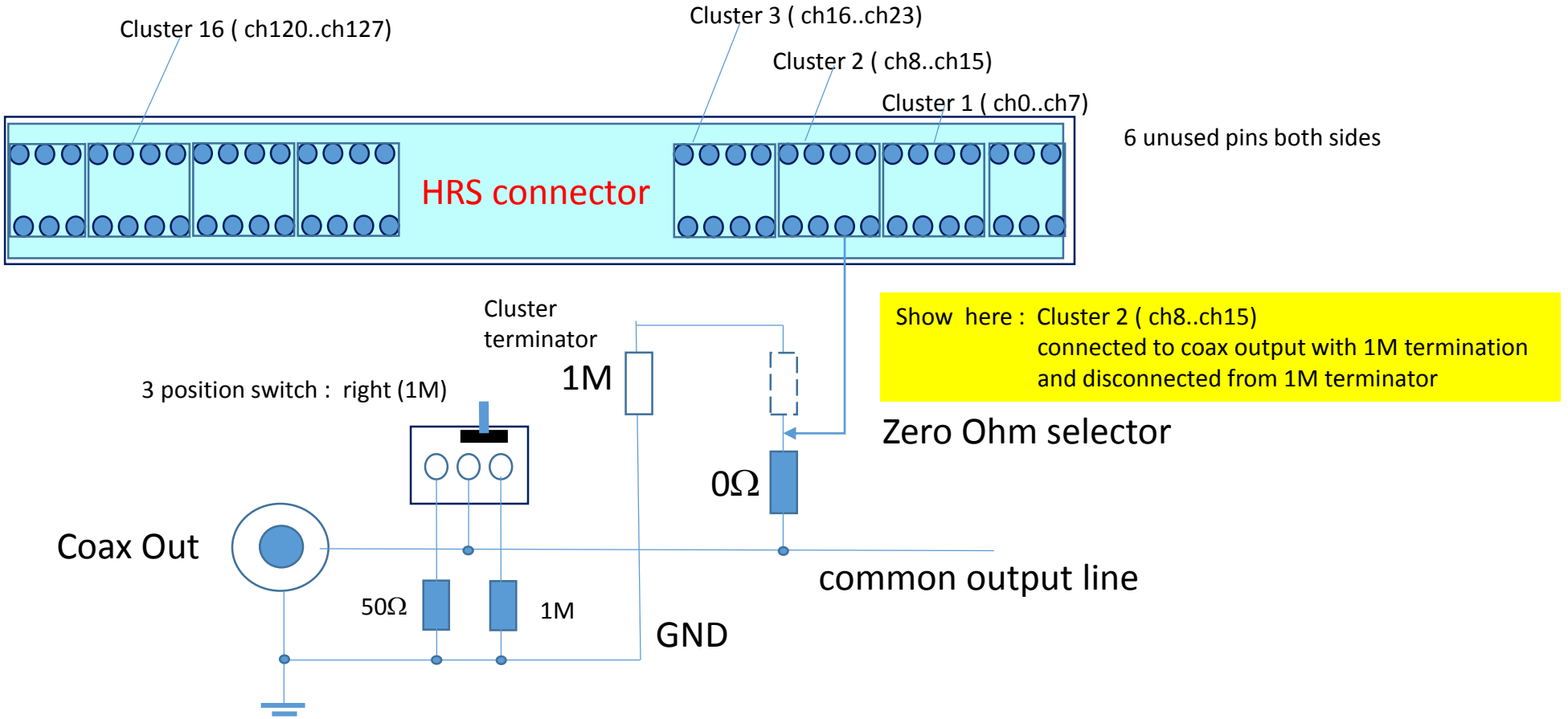

Un-used =
open / floating
detector section

Plugged HRS terminator =
defined GND potential on octal
Channel clusters (1M to GND)

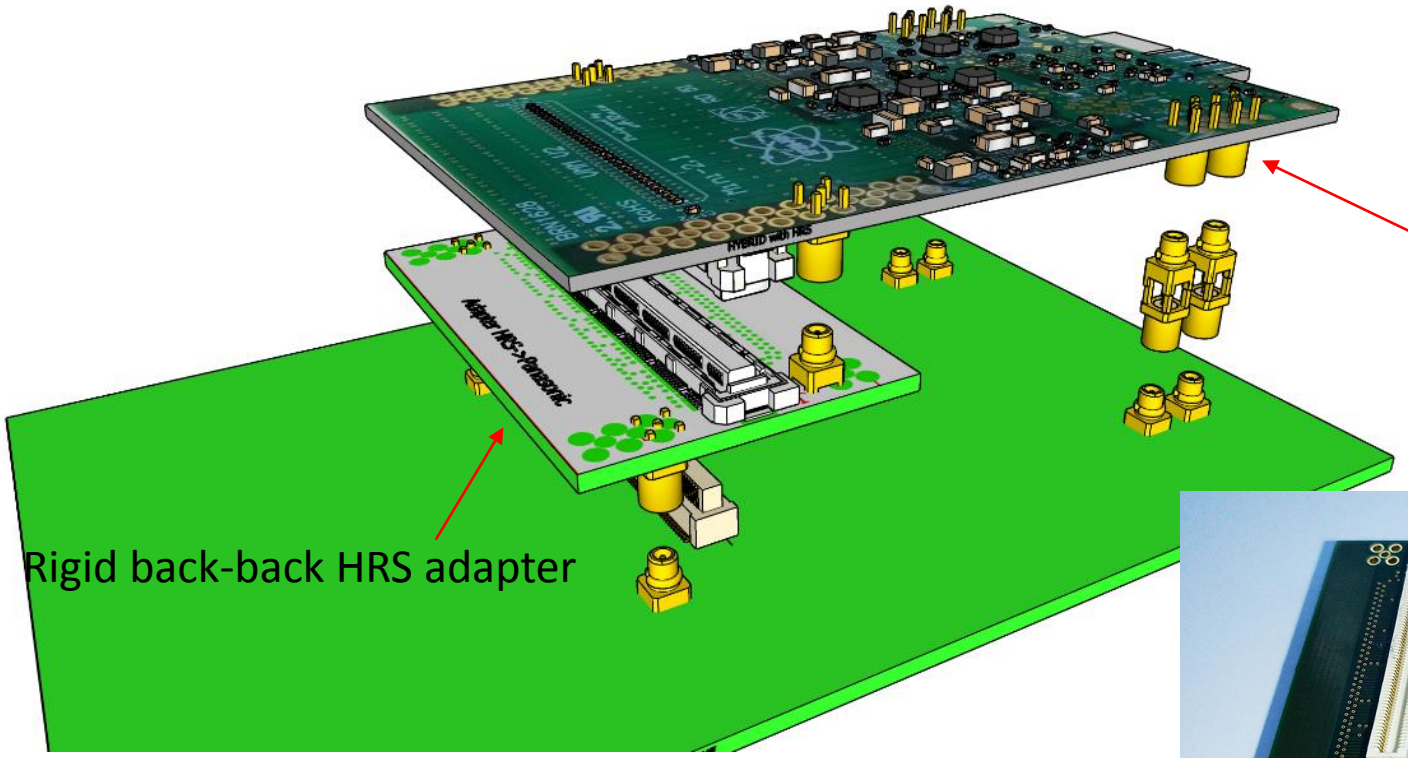
Option to select cluster(s) for
signal monitoring with 1M or High Z termination

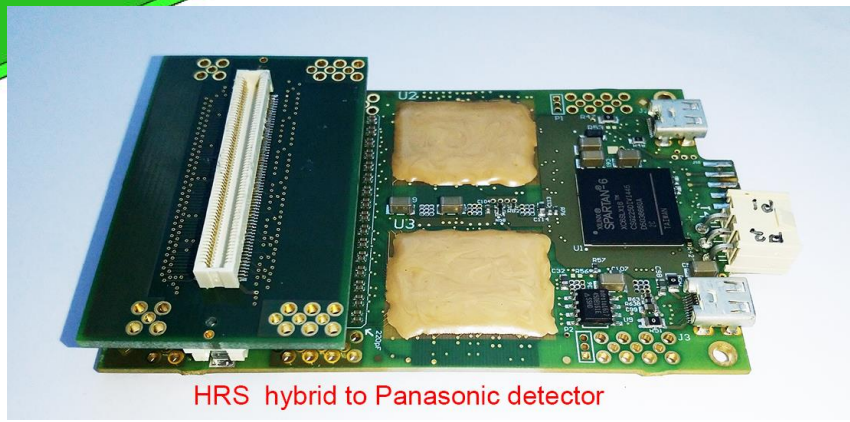
Note: **Exact <u>pitch of HRS connectors on Detector frames is 51.2 mm</u>**
**<u>( = 128 x 0.4 mm detector strips )</u>**

# Example: channel cluster 2 ➔ Coax (1MΩ) out
# all other channels ➔ 1M to GND



# Rigid adapter for VMM hybrids
## plugged to Panasonic connector




Revised version April 2019: fixed the reversed neighbor channel grouping

# Team interest in VMM-SRS systems

- **NMX @ ESS + ESS general readout**
- LSBB
- TU **Munich**
- **CERN GDD**
- Univ Tsukuba
- INFN Trieste
- **Univ Mainz**
- **Univ Bonn**
- **Budker**
- USTC
- Univ Kobe
- Univ Helsinki
- **Univ Virginia**
- N.N. ?

AdditionalObserving teams:

- CERN BE
- TU Munich
- U Peking
- ETH Zurich

Assuming 90% yield, our 25 wafers (arrival summer 2019) would be good for 1250 VMM hybrids
90% corresponds to our pilot production yield with untested VMM chips
The de facto yield could however be less, or fluctuating between wafers

=> **We will only find out by doing**

# VMM/SRS Pilots systems & Interested groups for the initial phase

Hybrids:

- 22 produced (can be shared depending on the needs)
- 27 ready around June (ordered by interested groups)

DCARD:

- 3 DVM v4 @ CERN/GDD
- 4 DVM v4 Assembled (BONN, MAINZ)
- 2 DVM v5 assembled @ CERN
- New version in production soon

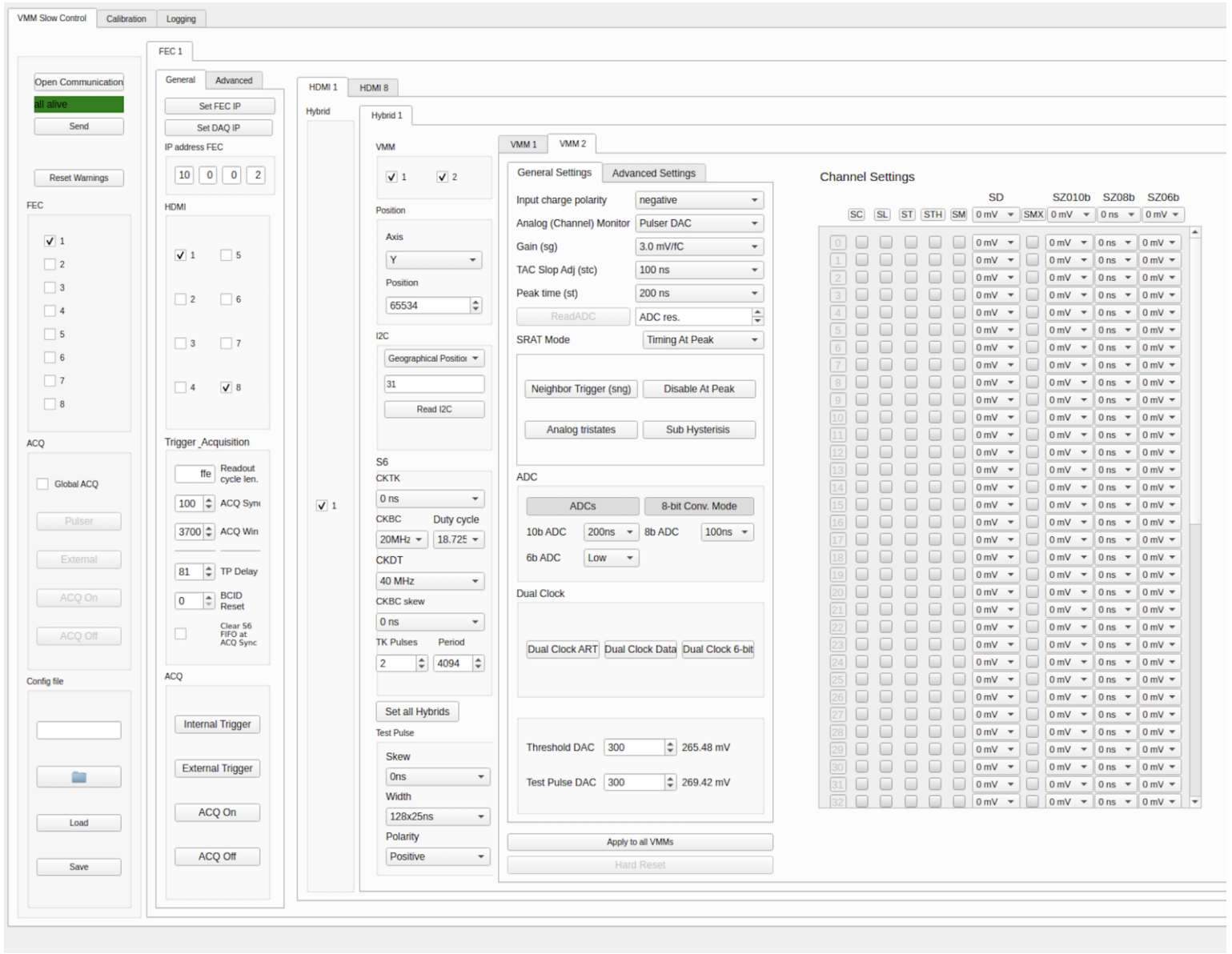
FEC: CERN Store

Mini-Crates:

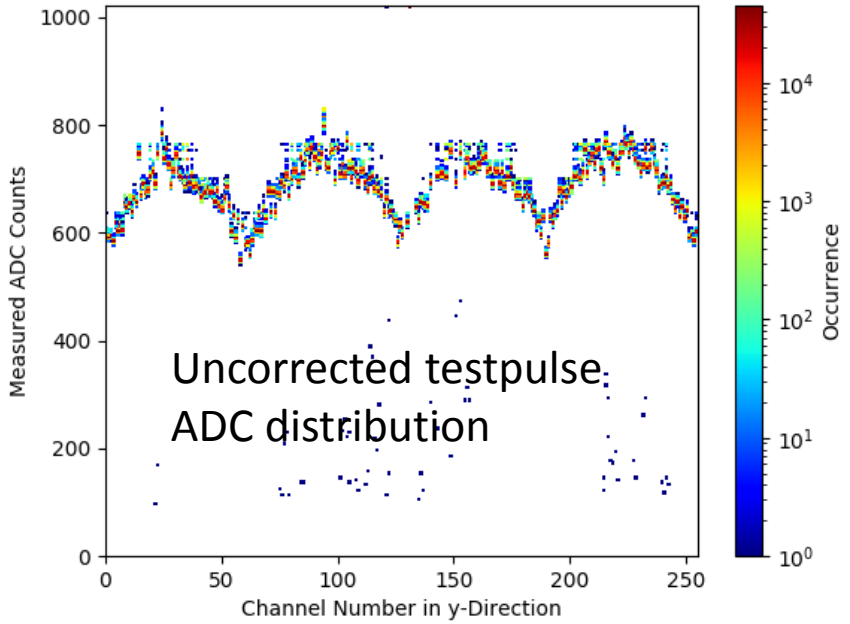
- 5 Prototypes at CERN/GDD
- Instruction to upgrade the old Mini-Crate available
- CERN Store Production most likely End of 2019, beginning 2020

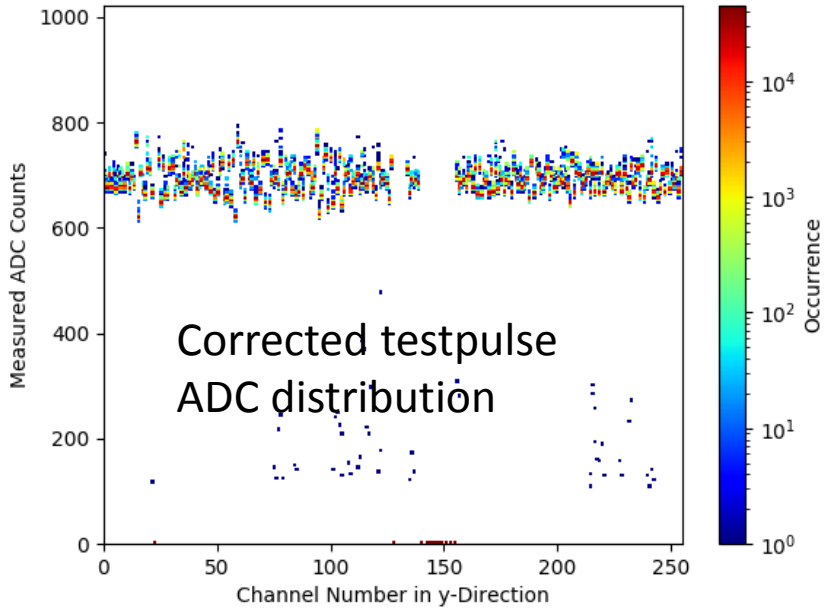
# Current software tools (GDD/ESS, ESS, ATLAS): Slow Control VMM3

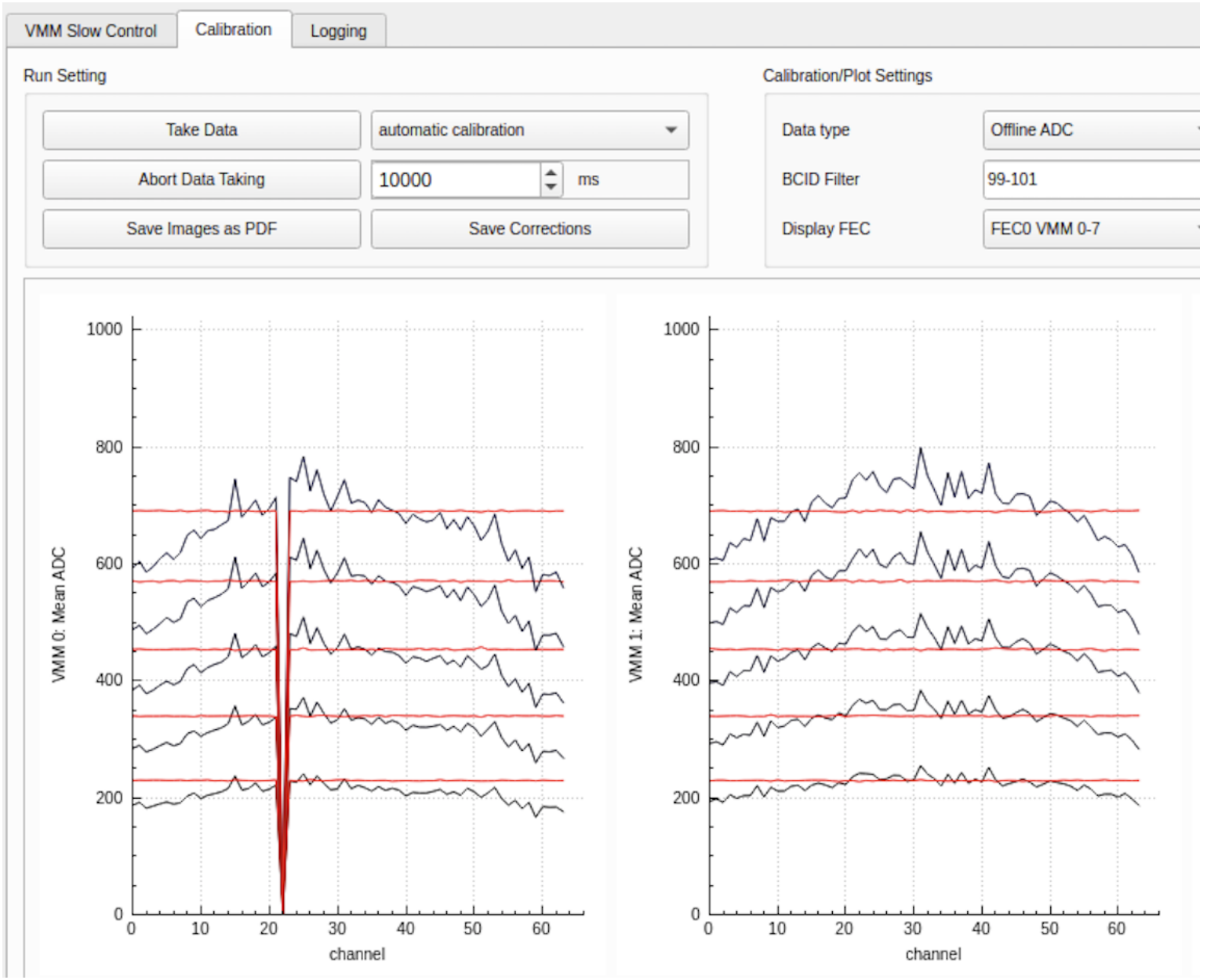
- Freely available under https://gitlab.cern.ch/mguth/VMM-software-RD51
- Used to configure multiple FECs and hybrids attached to them
- Has integrated DAQ feature to verify functionality of the system
- Calibration feature to correct ADC and TDC/BCID measurement of VMM
- JSON Correction files can be read in by ESS DAQ
- Threshold calibration in progress



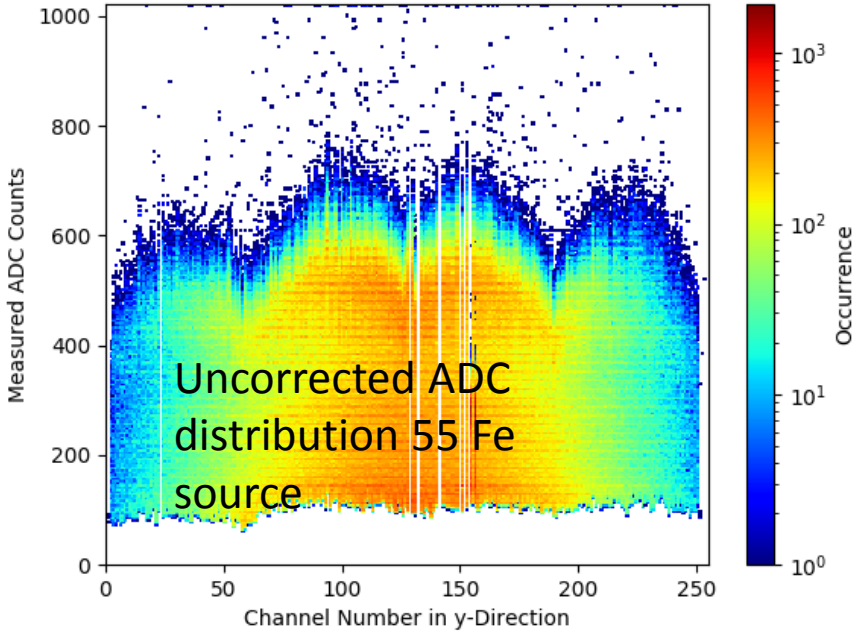
# Current software tools (GDD/ESS, ESS, ATLAS): Slow Control VMM3 – ADC correction

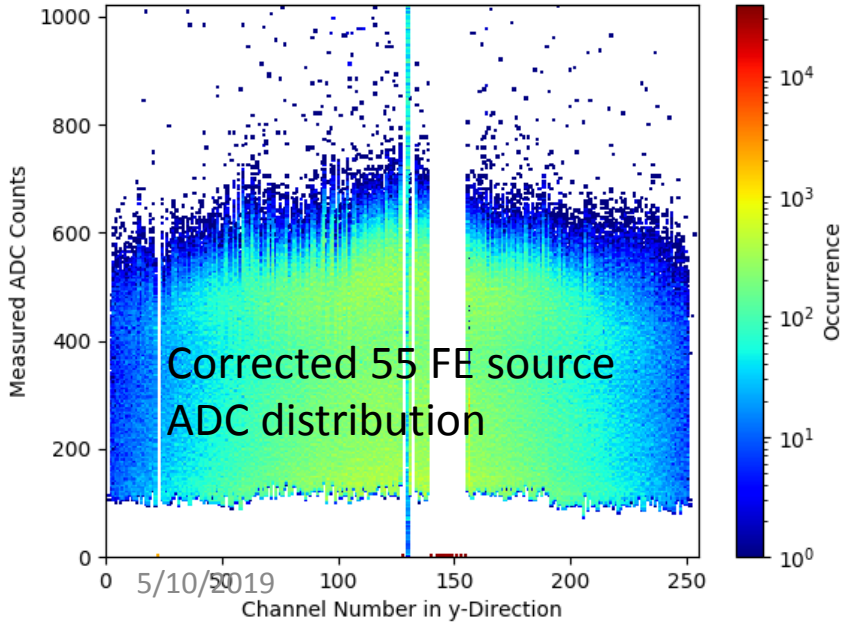


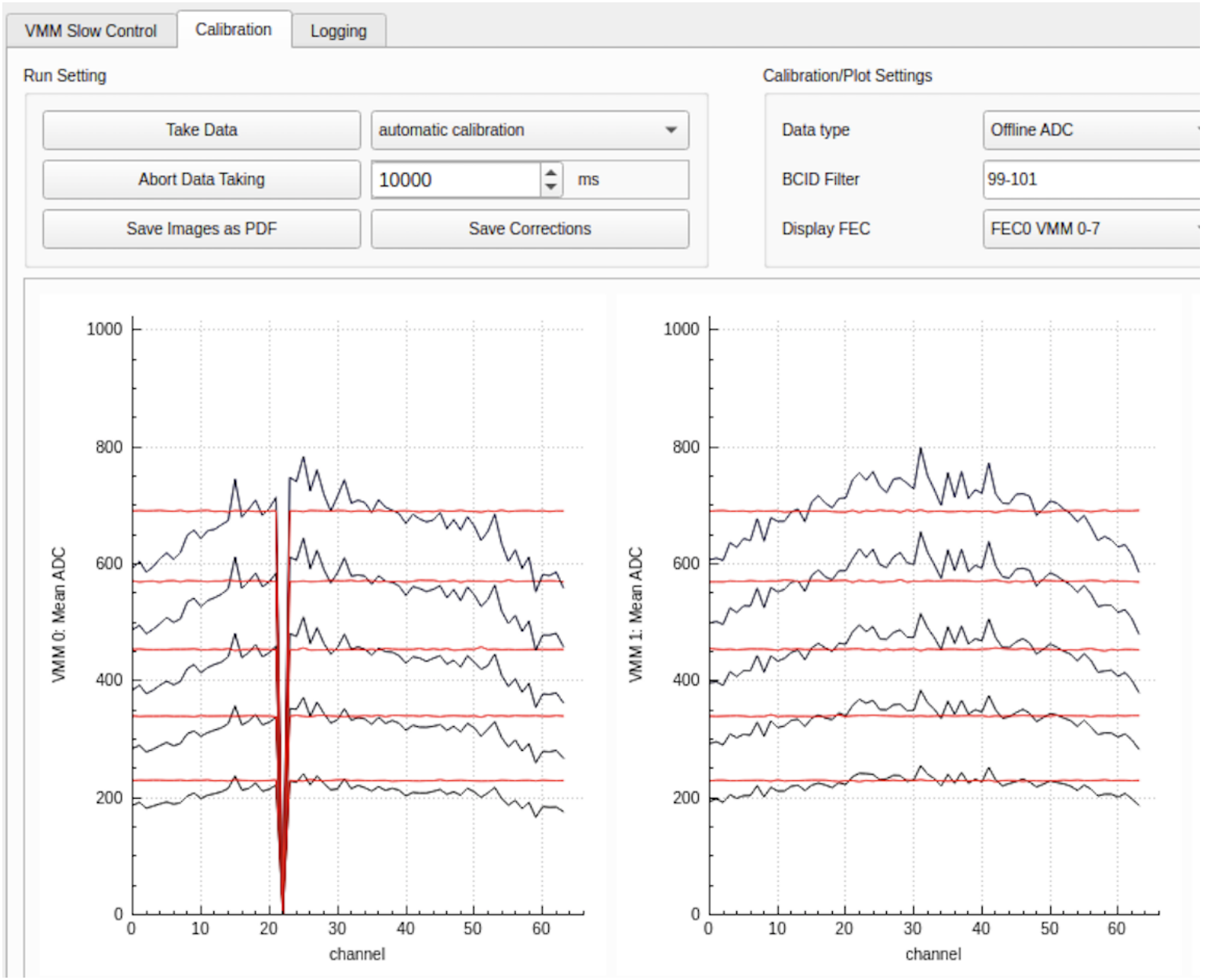



# Current software tools (GDD/ESS, ESS, ATLAS): Slow Control VMM3 – ADC correction

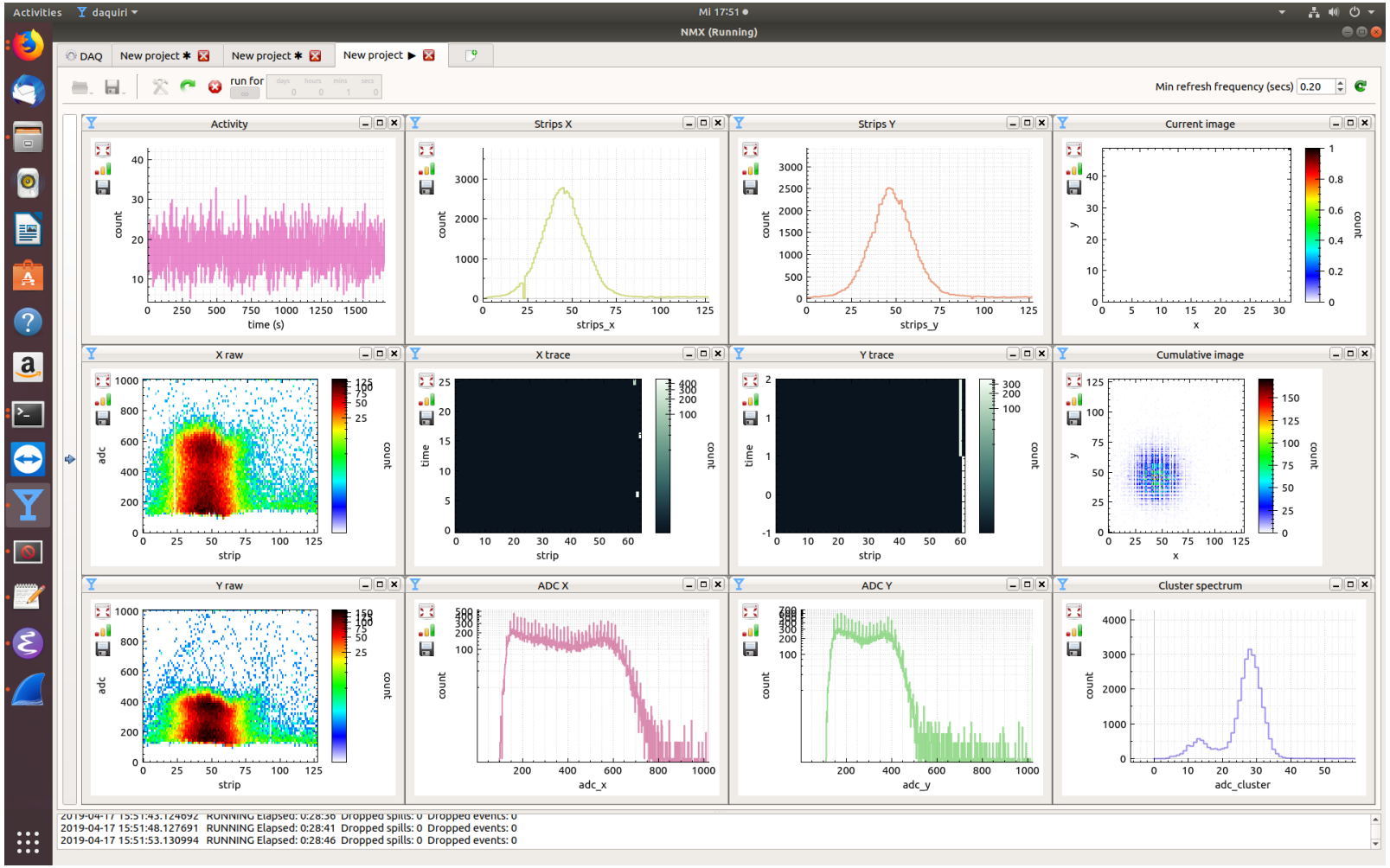


# Current software tools (GDD/ESS, ESS, ATLAS): ESS DAQ

- Freely available under https://github.com/ess-dmsc/essdaq
- Supports VMM3a and SRS readout
- Includes online monitoring software DAQUIRI
- System performance monitored with Grafana
- Option to write raw VMM3 data to HDF5 file
- Analysis tool to create ROOT tree from HDF5 file available https://github.com/ess-dmsc/vmm-hdf5-to-root



# VMM/SRS DAQ Software

- Existing and running in the GDD/RD51 Laboratory
  - Complete readout ctrl/chain available
  - Contributions coming from several groups (GDD/ESS, ESS, ATLAS)
  - Development ongoing

Today: Fine and without real critical points.

- RD51 groups interested in VMM and working on DAQ (RD51-WG5-SRSDAQ e-group created with about 40 members (number of active developers <10)
  - Mainz (S. Caiazza)
  - BNL (M. Purschke)
  - Atlas NSW
  - …

- Work Package with CERN EP-DT-DI DAQ team: Additional developments and support to add to the current situation.

# Work Package with EP-DT-DI

Collaborative effort for the development of a DAQ modular software for the SRS readout system. EP/DT-DI will contribute to the development and support of the DAQ software. It will assist the collaboration, will provide documentation and operations training, and will give best effort second line support in case of problems.

- *DAQ core with raw data writing* that can be “comfortably” implemented by users.
- *Scalability:* DAQ should preserve scalability of SRS: from the minimum of a single Front End Card (FEC) with 1 hybrids, to a system with multiple FEC.
- *Data transmission and error checks:* Implements tools to qualify the data transmission and possible losses.
- *System configuration:* Configuration files should be stored together with the recorded events.
- *High rate:* The core of the DAQ should provide raw data on disk and it should be optimized to reduce or eliminate any effect on the maximum rate of acquisition.
- *Future developments and interfaces:* List of the possible or needed implementations to improve the readout system and to facilitate its interface with other readout systems (busy signals as one example).
- *Open source code*

## Resources

EP-DT-DI has allocated 0.8 FTE to general DAQ development, of which a variable fraction will be dedicated to the integration of the RD51 readout use case, depending on the project phase.