MicroWeekly meeting

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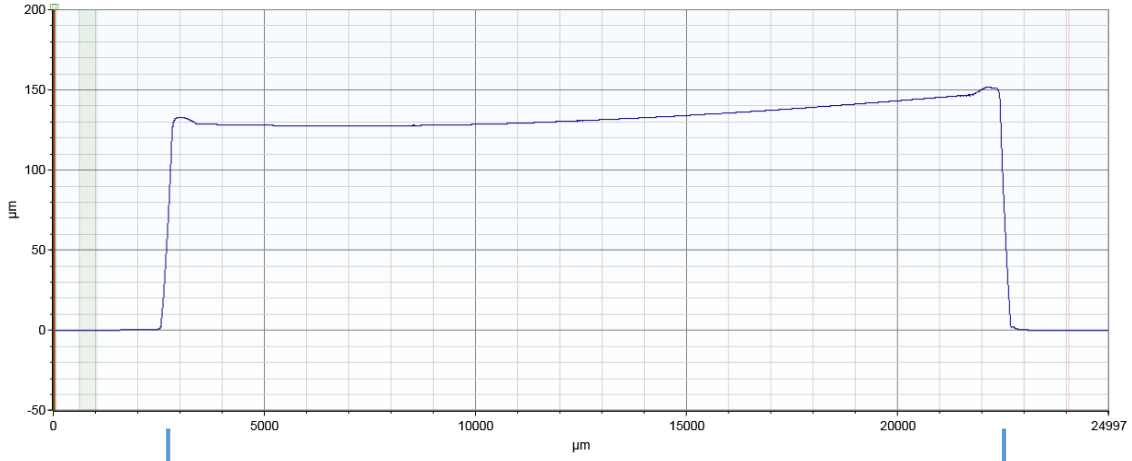
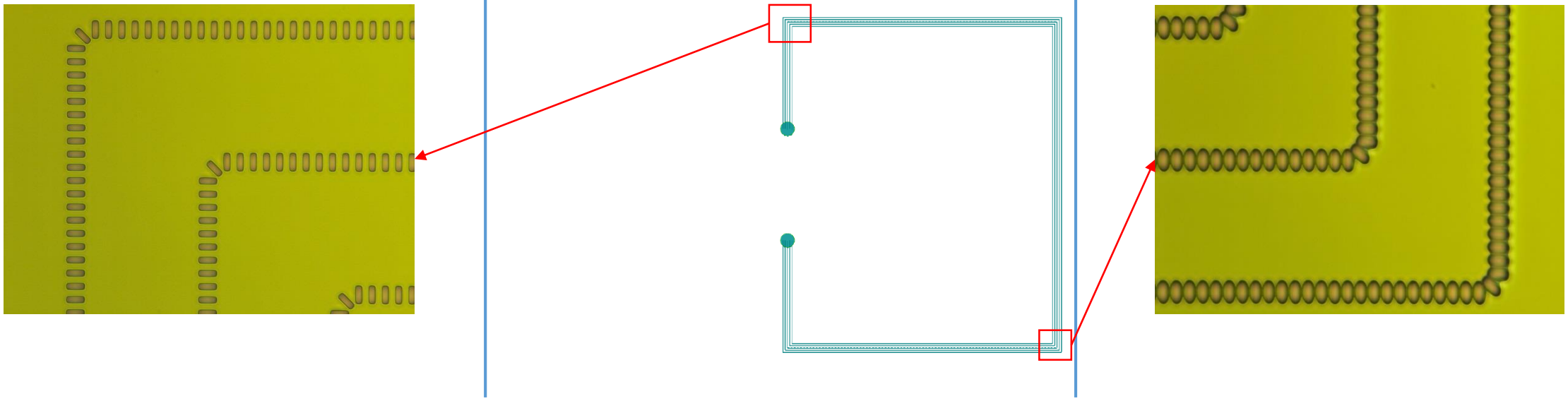
As a reminder: failure exposure

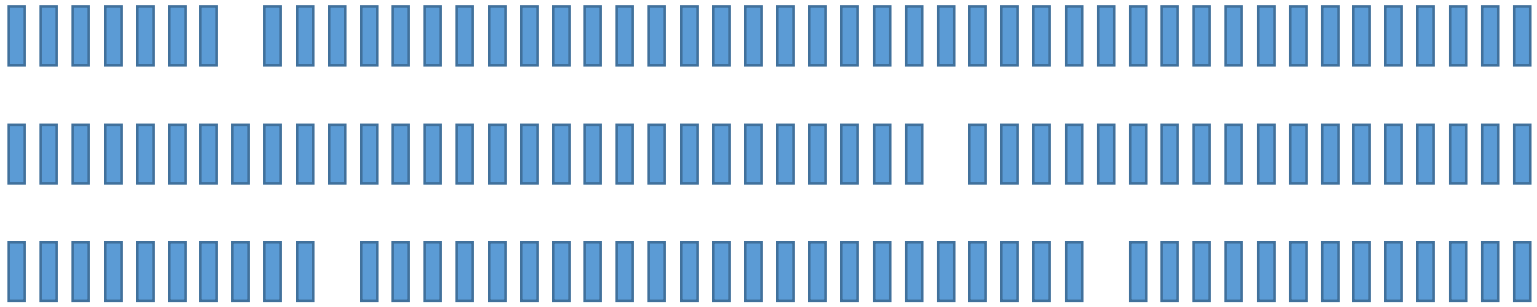




Solution: manual coating

Quite good results. However:

- Goodbye certainty, welcome probability: few trenches are missing (as if they were missing from the design). Reason unknown (bug?)



The function “AutomaticRectangle” of the MLA150, which automatically detects the edges of the chip, centering the design does not work in the proper way: misalignment in the Y direction of about +1 mm.
Solution: “fake” alignment with the corners of the chip.

Photoresist is missing from the borders due to edge effects. How to protect the underlying material?

Current situation:

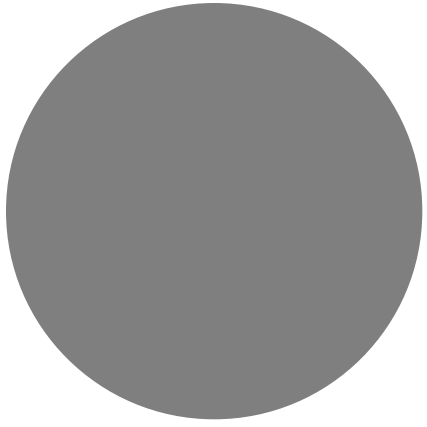
The integration of buried microchannels has started on 2 MALTA chips batch 1.

One of the chip has been contaminated by quickstick during the vacuum pumping in the dry etcher (bubbles of air which explode). Cannot be further processed.

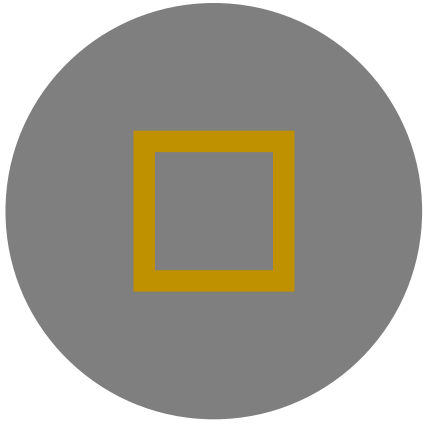
The other one has been also contaminated but in a lesser extent and it has been delivered for parylene passivation.

The protective tape cannot be used anymore because it can strip the photoresist.

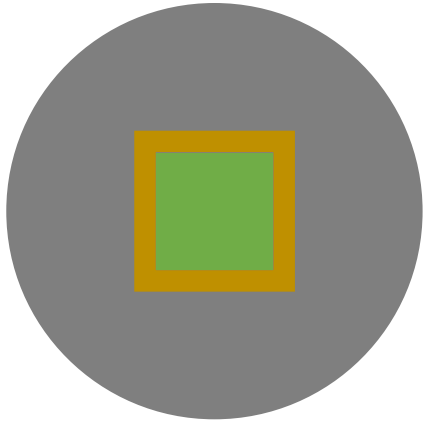
New procedure for the next time:



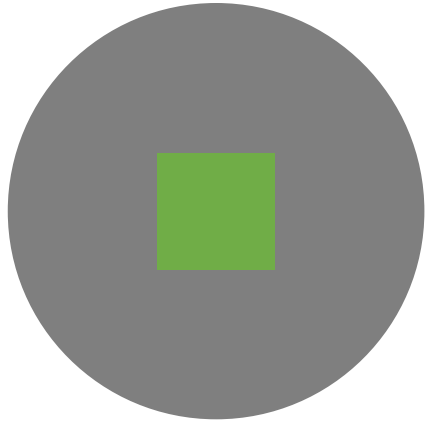
1. Naked carrier wafer



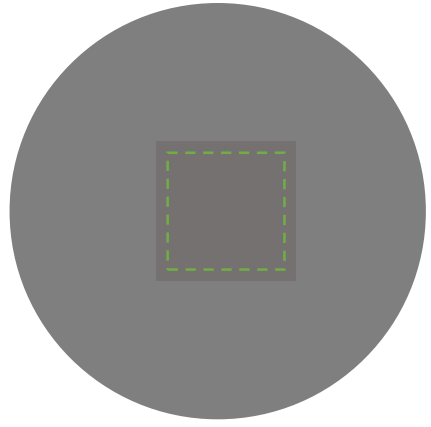
2. Kapton tape which recreates a shape a little smaller than the external dimensions of the chip



3. The cavity is filled with quickstick



4. The kapton is removed when the wafer is still on the hotplate (and quickstick is liquid)



5. The chip is attached, avoiding any quickstick exceeds

Pressure test: