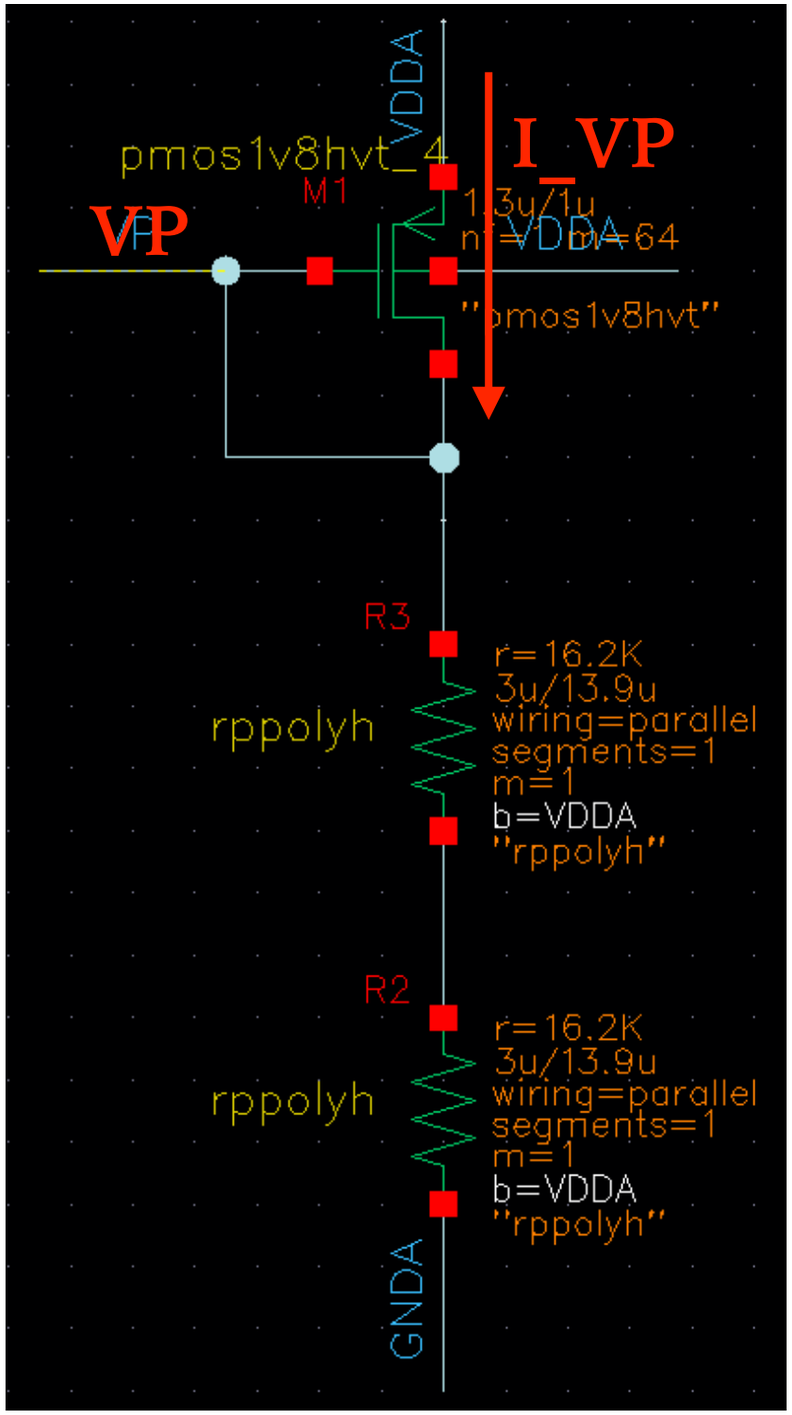
Matching issues on the bias voltages

- Serious mismatch of bias voltages has been observed from the measurement of RD50-MPW1. Although, there is suspicious issue with the measurement set-up, it is still worth to look into this matter.
- From the schematic design level:
  - All bias voltages are based on a reference voltage VP generated on chip. Variations of the transistor M1 and the resistors R2, R3 contribute to the mismatch of all bias voltages
  - Optimise the size of M1 and replace the rppolyh resistors (high resistivity, high variation) with rppolyl resistors (low resistivity, low variation) for better matching.
  - distribute the current I_VP instead of the voltage VP to generate different bias voltages.
- From the layout design level:
  - re-arrange transistors for better matching.



Comparison based on Monte Carlo simulations

	Before modification				After modification			
	Min	Max	Mean	Std Dev	Min	Max	Mean	Std Dev
VP	927 mV	1.06 V	1 V	24.7 mV	478 mV	620 mV	541 mV	22.5 mV
I_VP	26.9 μA	48.8 μA	36 μA	4.14 μA (11.5%)	29.2 μA	44.4 μA	35.8 μA	2.76 μA (7.7%)
VPCOMP	1.14 V	1.31 V	1.23 V	28.2 mV (2.29%)	1.15 V	1.31 V	1.23 V	27.7 mV (2.25%)
I_VPCOMP	7.27 μA	12.99 μA	9.95 μA	1.16 μA (11.7%)	7.7 μA	13.13 μA	10.33 μA	0.95 μA (9.2%)
VNFB	503 mV	671 mV	583 mV	27.3 mV (4.7%)	519 mV	653 mV	586 mV	22.8 mV (3.9%)
I_VNFB	277 nA	602 nA	396 nA	57.2 nA (14.4%)	294 nA	550 nA	411 nA	48.5 nA (11.8%)

- Modifications are on schematic design level by now.
- Standard deviations of generated currents are 20% - 30% smaller after modification. Smaller currents have higher variation (I_VNFB), larger currents have lower variation (I_VPCOMP).

Matching issues on the bias voltages

- use a Low Dropout (LDO) regulator to minimise the variation on the transistor?
- Opions?