# Investigation of new technologies and concepts for reliable computation and fast communication

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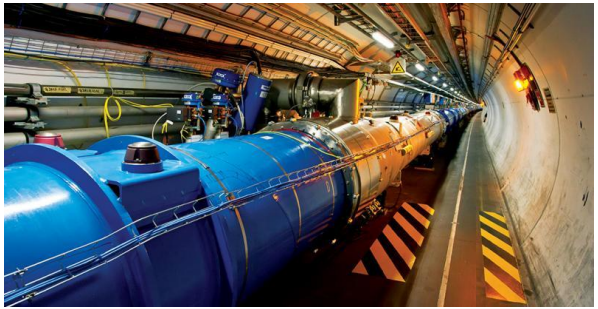
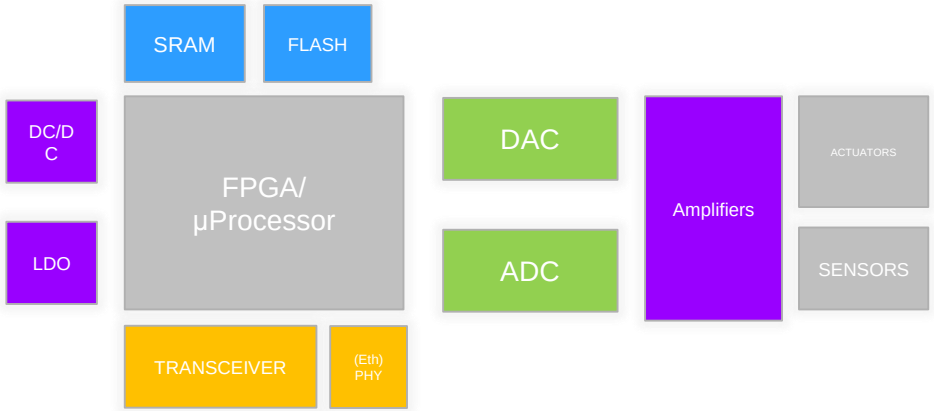
# Outline

- Introduction
- Problematic
- FPGAs Solutions
- µProcessors Solutions
- Future Work

# Introduction

- Electronic Systems are based in the co-existence between analogue and digital components
  - Central core (the “brain”) is usually a µProcessor, or an FPGA.
  - Computational, control and communication tasks
- The faster our “brain” works, the more (and better) things we can do!

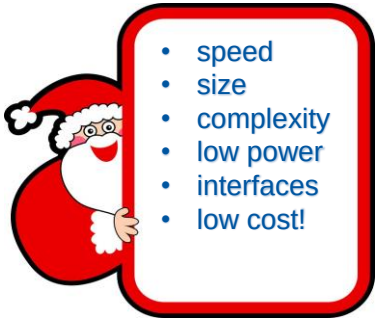


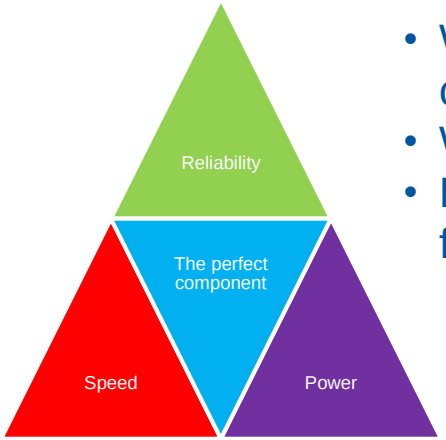



- However!!! Radiation Effects to Electronics have always been a limitation factor when it comes to performance:
- Future upgrades mean
  - More data, higher speeds
  - More radiation -> showstopper?

# Problematic

- So far there are two main type of systems:
  - Systems that operate in high speed
  - Systems that conduct complex operations



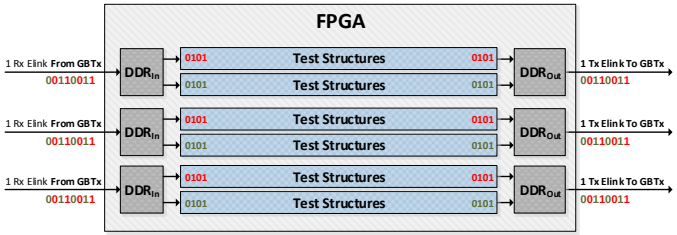




- What if we want both speed and complexity?
- What about reliability?
- Different applications require different features
  - A long investigation on FPGAs and µProcessors
  - provide users with as many options as possible for them to chose

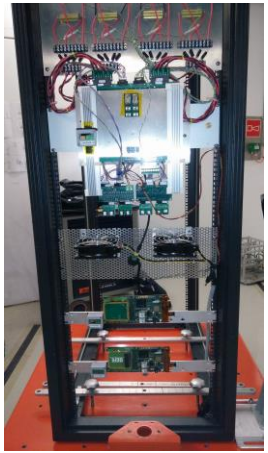
# FPGA Solutions ProASIC3E

- Traditionally at CERN two FPGAs have been used:
  - ProASIC3E FPGAs for less crotical applications
  - Anti-FUSE FPGAs for critical applications.
- Several new FPGAs and technologies are being considered by equipment groups and not only and are tested
- EN-SMM-RME leads the qualification of new FPGA and µProcessors
- Component level + System Level

- **ProASIC3E** Flash Based FPGA tests:
- EN-SMM-RME + BE-BI for the GEFE System.
  - Team of R. Ferraro, I. Deg'Innocenti, M. Barros Marin and G. Tsiligiannis
  - System Level testing @ CHARM
- E. Gousiou tests for NanoFIP converter @ PSI
- Results @ EDMS **1863774, 1183301**




© Courtesy of R. Ferraro, M. Barros Marin and I. Deg'Innocenti



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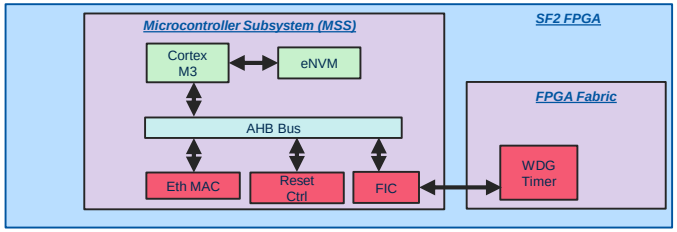
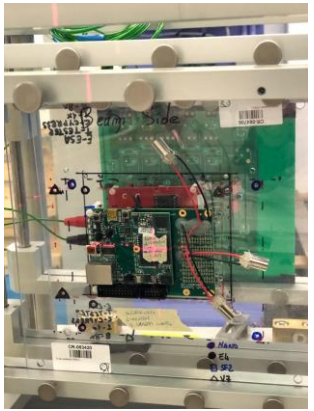
# FPGA Solutions SmartFusion2

- **SmartFusion2** Flash Based SoC FPGA: Fabric + ARM Cortex-M3
- Full qualification campaign @ PSI with 200MeV protons
  - flip flops, PLL, BRAM, DSP, dose level limitation, re-programmability, applications etc.
  - Results @ EDMS **1607767**
  - G. Tsiligiannis et al., "*Investigation on the Sensitivity of a 65nm Flash-Based FPGA for CERN Applications*," REDWS RADECS, Germany, September 2016.
- CHARM tests by TE-CRG @ EDMS **1892584**
- Further tests with µProcessor + FPGA fabric for fast transmission of data using RAW Ethernet
  - Bare Metal + RTOS - G. Gnemmi driving the tests now
  - Combined tests at **PSI**, **CHARM** (**protons**) and **CHARM** (**Heavy Ions**)
  - Results under processing and towards a full reliability analysis
  - RADECS + EDMS on the way!

CHARM Radiation tests of SF2
©Courtesy of G. Gnemmi



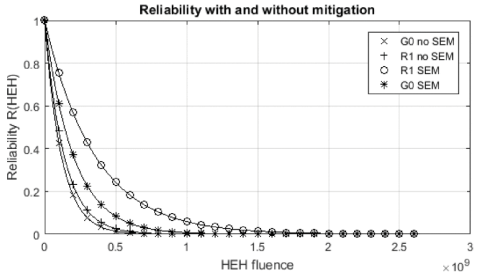

SmartFusion2 SoC FPGA



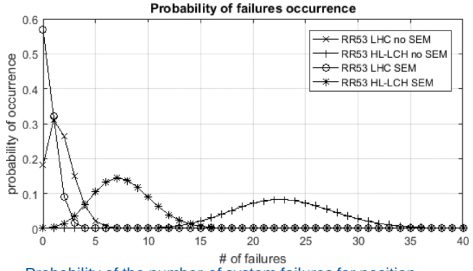
CHARM HI Tests
©Courtesy of G. Gnemmi

# FPGA Solutions Artix7

- The **Artix7** FPGA has been targeted: System Level testing
  - Configuration memory (CRAM) testing at **CHARM, Am-Be, ESRF and ILL** facility
  - System Level testing with µBlaze + LwIP @ **CHARM**
- A novel methodology has been introduced:
  - Reliability analysis of a System based on CHARM SEU data
  - Failure prediction of the System
  - G. Tsiligiannis et al., “Radiation Effects on Deep Sub-micron SRAM-based FPGAs under the CERN Mixed-Field Radiation Environment,” IEEE Trans. Nucl. Sci., vol.6 no.8, pp. 1511-1518, February 2018.

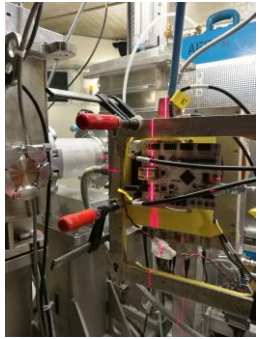



Reliability function of the application for locations G 0 and R 1, with and without the use of the soft error mitigation IP (scrubber).




Probability of the number of system failures for position RR53 calculated with the annual fluence for the LHC under run 2 at $2\times10^8$ HEH and for the HL-HC at $2.7\times10^9$ HEH.

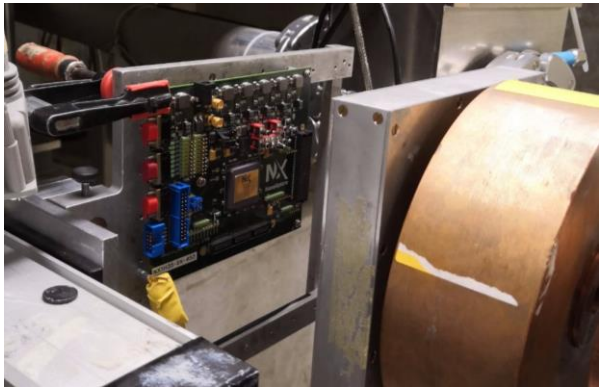
Am-Be Facility @ CERN



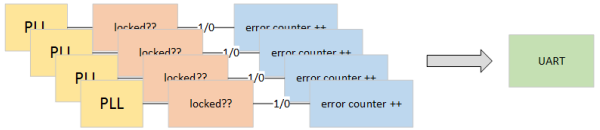
PSI Radiation campaign

# FPGA Solutions NanoXplore

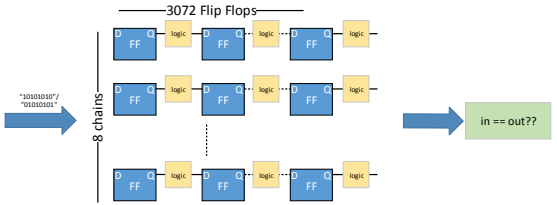
- **NanoXplore** supported by ESA and CNES to create a “made in Europe” RadHard FPGA
- NG-MEDIUM: 65nm Rad-Hard SRAM Based FPGA
- Full qualification @ PSI with 200MeV protons
  - FlipFlop, DSP, PLL, RAM, TID limits, CRAM etc
- Promising results
  - >3kGy + Good SEE response
- Technical Training to be scheduled the **30th of January to the 1st of February**
- Results @ October RADWG meeting (indico)
- Results to be published to the next RADECS + EDMS



NG-MEDIUM FPGA Radiation testing at PSI facility with 200MeV beam




PLL Test structure schematic




Flip Flop test structure schematic

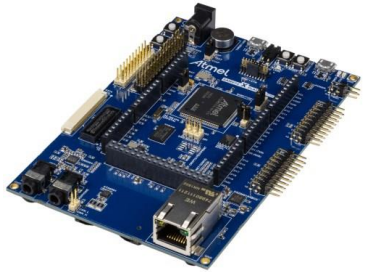
# MCU Solutions

- New approach for certain tasks that don't necessarily need an FPGA (we don't want to shoot a fly with a bazooka!)
- **STMicroelectronics** and **Atmel** offer large variety of COTS
- M0, M4 and M7 ARM Cores
- Multi-level testing:
  - Internal RAM, ADC, FPU, peripherals, Ethernet, Wireless
- **STM32F4, STM32F7, SAM4E, SAMV71, SAMD21** tests @ PSI with 200MeV protons
- G. Piscopo, A. Damigos Papotis, G. Gnemi
- Results show that some MCUs have outstanding resilience to TID (up to 500Gy)
  - Reports @ EDMS **2059030** + **2059033**
  - Further results: NSREC + RADECS +EDMS

STM32F4 MCU

SAMD21

SAM4E MCU



SAMV71 MCU

# Future Work

- Several options exist that can be well adapted to a wide range of applications
- Radiation can be limiting but thanks to the vast expansion of FPGAs and MCUs since the last decade, a wide range of COTS exists that can cover our needs
- Further developments and testing at the FPGA and MCU level
  - Focus at the System level performance of certain applications
  - Understand better and invest in Reliability Methods for the prediction of the performance of Systems operating in radiation environments
- More components to be tested -> always seeking for the best balance between performance and reliability
  - More fine grained tests

# Thank you for your attention!

Questions?!