

Powerlink: status and developments

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BE/CO/HT

Powerlink – What is?

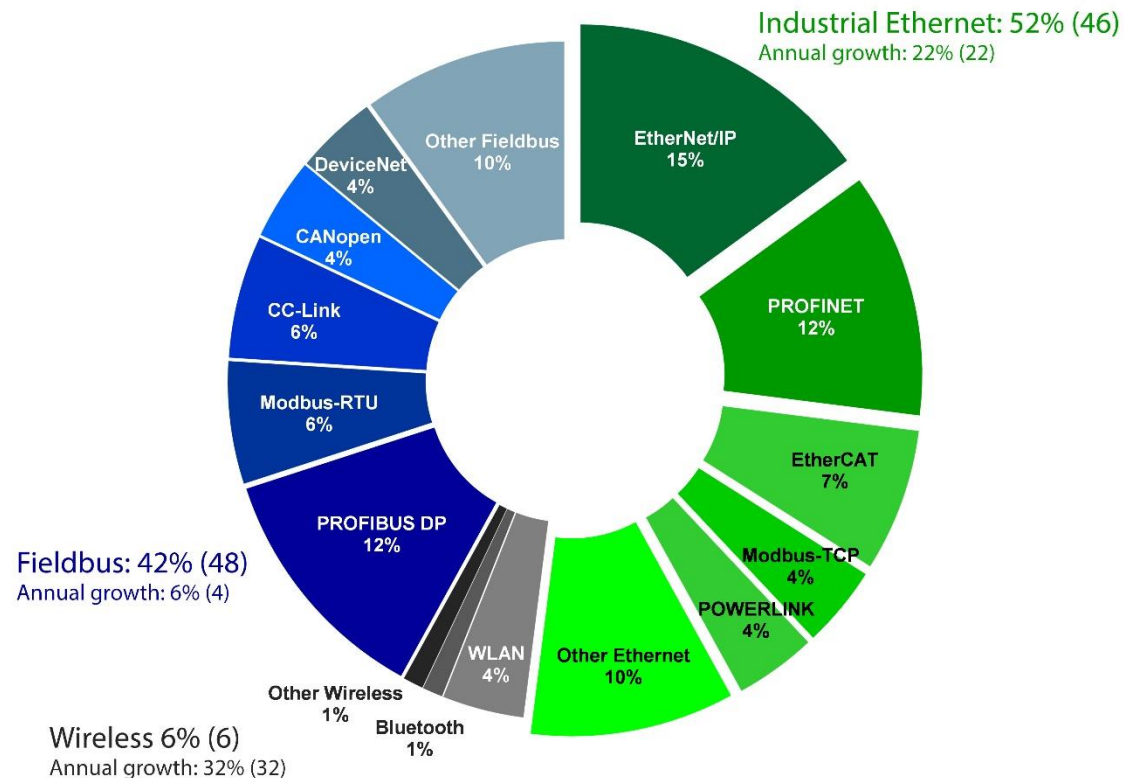


❖ Industrial Ethernet Fieldbus

- ProfiNET (Siemens)
- EtherCAT
- Ethernet/IP

❖ Open Standard

- No patents (royalties)
- No mandatory subscriptions
- No mandatory sell



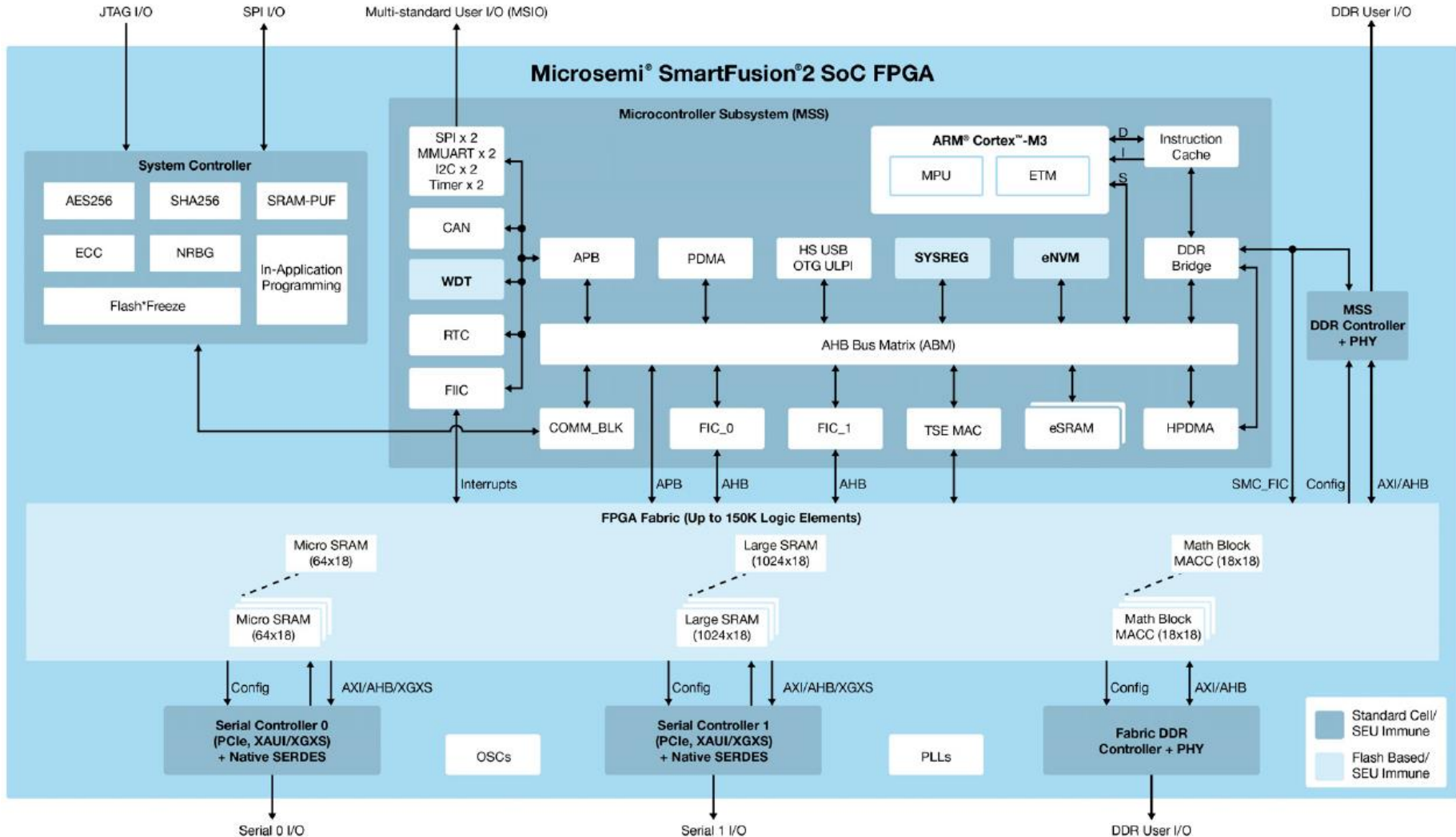
Powerlink stack

- ❖ Open source implementation available (openPOWERLINK)
- ❖ Run on a number of devices
 - ❑ PLC
 - ❑ Computer (userland and kernel)
 - ❑ Embedded devices
 - Userland runs in a ARM
 - Kernel runs in a soft-processor for real-time performances
- ❖ openPOWERLINK not designed for low-memory embedded device
 - ❑ Running userland & kernel stack require >300 kB of memory (code and data)
 - ❑ Code of Master and Slave implementation is mixed together
- ❖ Goal: run it on a SmartFusion 2 FPGA

SmartFusion 2



- ❖ FLASH based FPGA, with fabric SRAM and DFFs
- ❖ ARM core + ECC SRAM (64 kB) + eNVM (flash memory for code)



Results at CHARM using ARM Cortex-M3

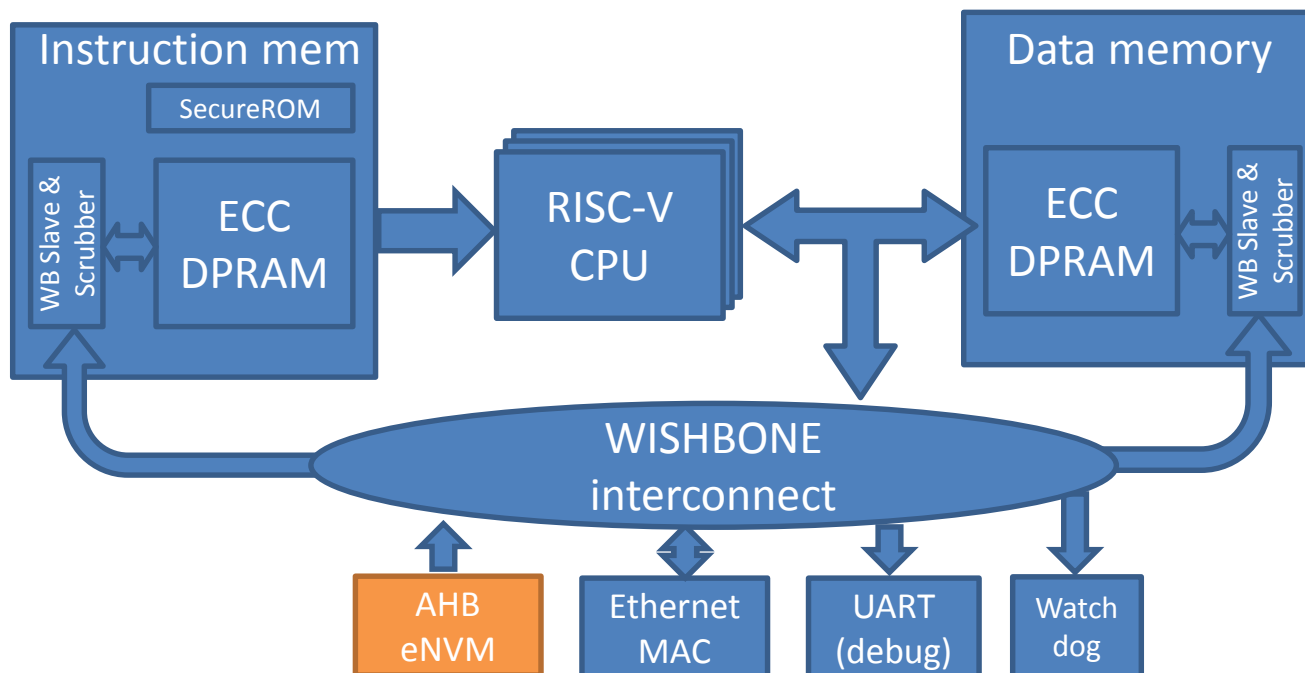
- ❖ openPOWERLINK memory footprint reduced to 170 kB (143 kB of code, 27 kB of data)
- ❖ Processor clocked at 100 MHz
- ❖ Data memory protected by ECC

- ❖ Tested in G0 position for one week (about 25 Gy TID)
 - Multiple self-resets due to internal PLL loss-of-lock
 - Freezed several times (one every 10 hours), power cycle required, no useful debug messages
 - No increased power consumption detected

- ❖ Cortex-M3 is not TMRed
- ❖ AHB interconnect is not TMR
- ❖ eNVM is OK under radiation, but it is connected to AHB interconnect!

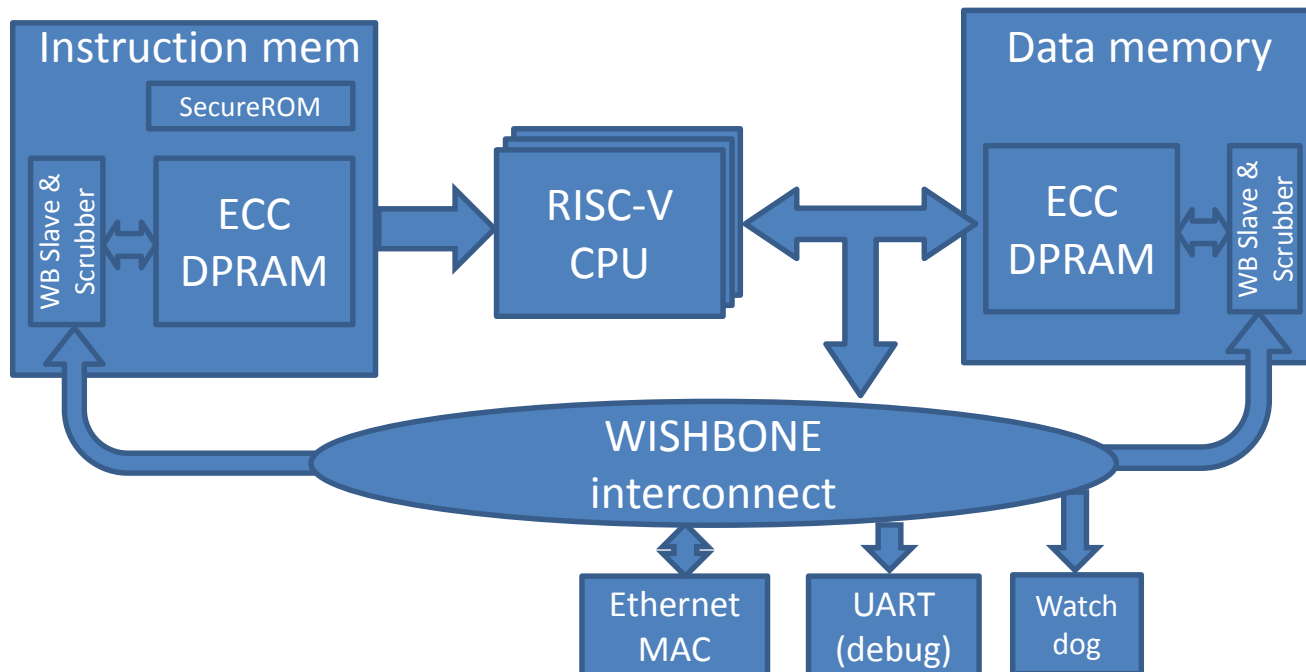
Soft-core based SoC

- ❖ RISC-V softprocessor with TMR
- ❖ ECC (SEC-DED) instruction memory up to 92 kB
- ❖ ECC (SEC-DED) data memory up to 32 kB ought to be enough for anybody
- ❖ Application loaded from eNVM memory and stored inside both memories (integrity check/cryptographic signature)



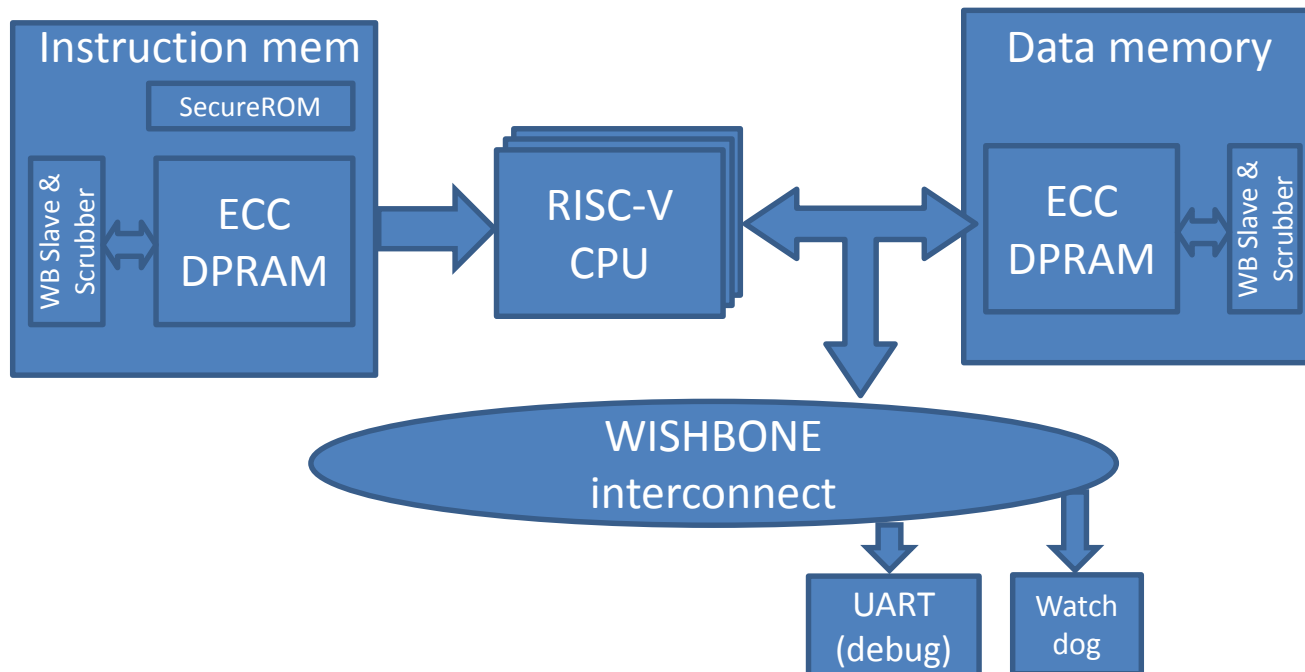
Logic utilization

- ❖ Partial TMR of RISC-V running at **50 MHz**, **32 kB + 32 kB of ECC SRAM**, Ethernet MAC
- ❖ **Fmax: 60 MHz**
- ❖ DFFs and LUTs with MS2050 SF2: **30% (15k LUTs, 13k DFFs)**



Results at CHARM using RISC-V SoC

- ❖ Partial TMR of RISC-V running at 50 MHz
- ❖ ECC instruction and data memory: **8 kB + 8 kB**
- ❖ RISC-V running a checksum of data memory
- ❖ ECC single error & double error stats
 - ❑ SEU Cross-section (single error correction): **2.4E-14**
 - ❑ Double error cross-section: **no data**



Prospects for 2019

- ❖ True TMR of RISC-V, keeping 50 MHz
- ❖ Optimize SRAM utilization
- ❖ Fix Ethernet MAC bugs and improve it for rad-tol
- ❖ Optimize Powerlink stack: 50 kB of code
- ❖ Test low-latency Industrial Ethernet PHY (Texas Instruments DP83822) under radiation