IsCMOS readout system status

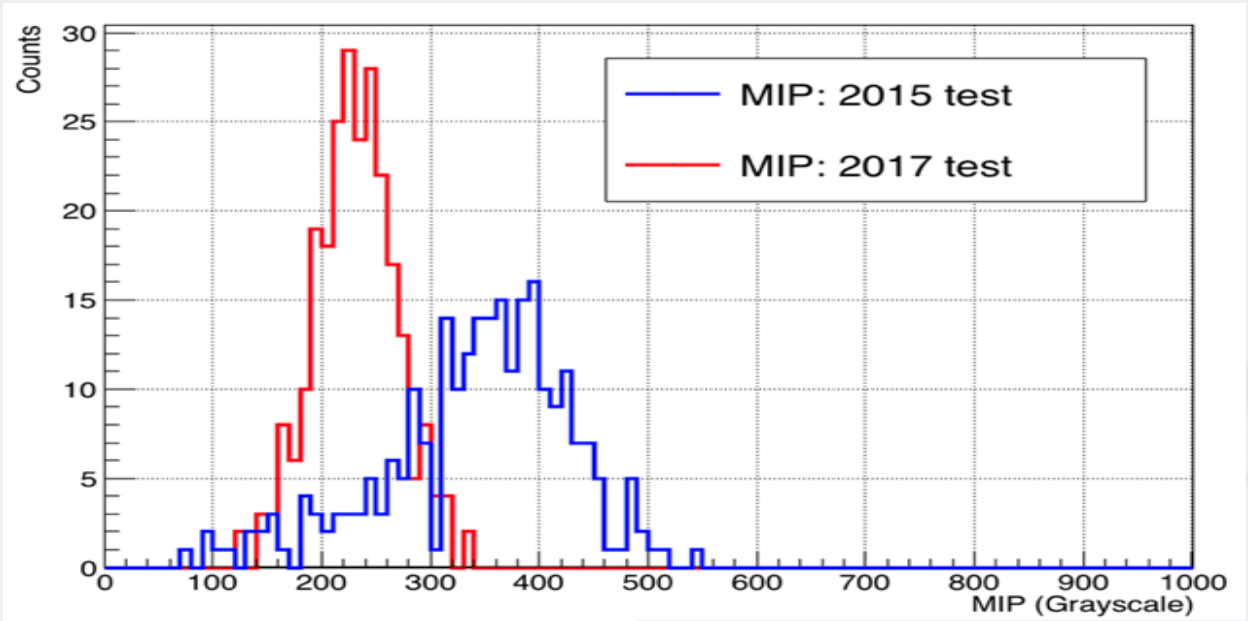
Yonglin Bai

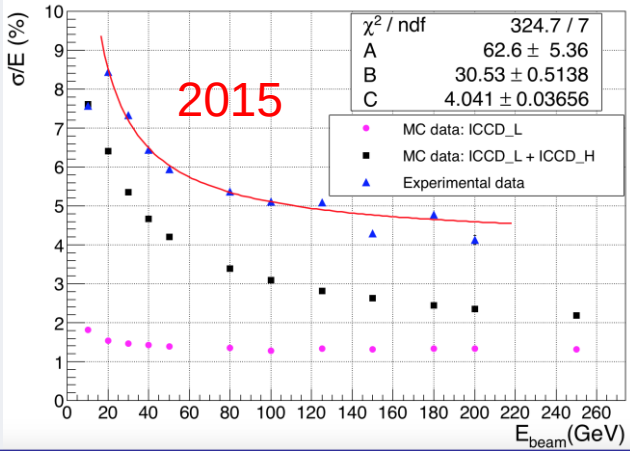
2018-11-06 CERN

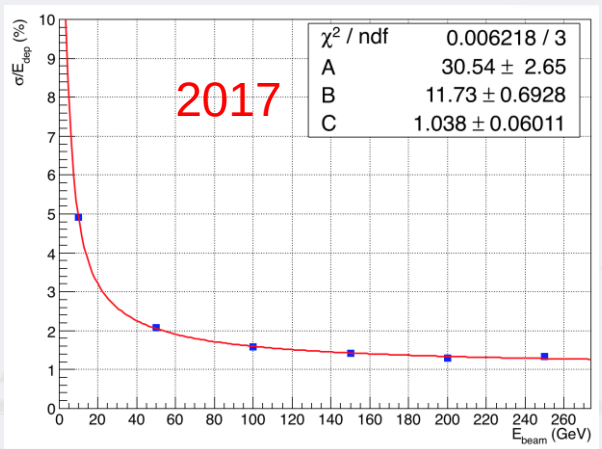
Outline

- Background
- IsCMOS Developement
- What to Improve
- Next to do

Performance of IsCMOS camera prototype 2017





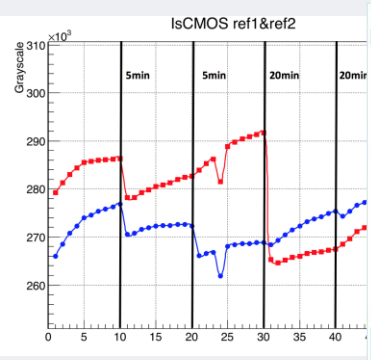


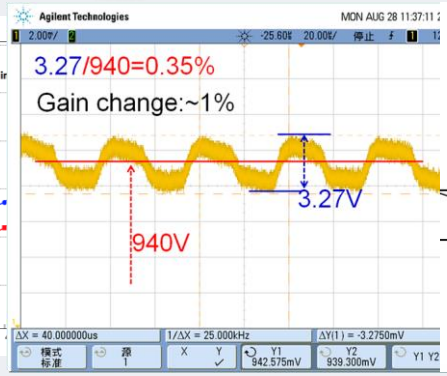
- Higher sensitivity；
- Low Noise；
- Globe shutter；
- 1MIP to P.E.：
  2015 ~200P.E.
  2017 ~100P.E.

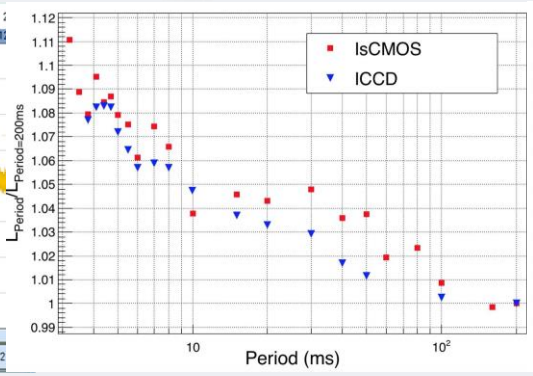
Energy Resolutions of electron ~1.3%@200GeV by apply a IsCMOS camera on high output channel ；

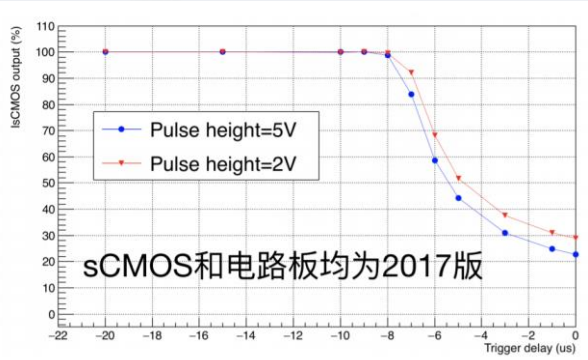
Performance of IsCMOS Prototype 2017

Defects of 2017 IsCMOS	Effect
Gain unstable under high density illumination	Difficult to calibrate for beam test
Gain vibration caused by HVP ripple	Lower energy resolution
Long afterglow of screen	Pulse pileup
Trigger delay of CMOS	Lower Sensitivity
CMOS noise	Lower dynamic range and poor sensitivity
CMOS image frame transfer error	Lower event detection efficiency





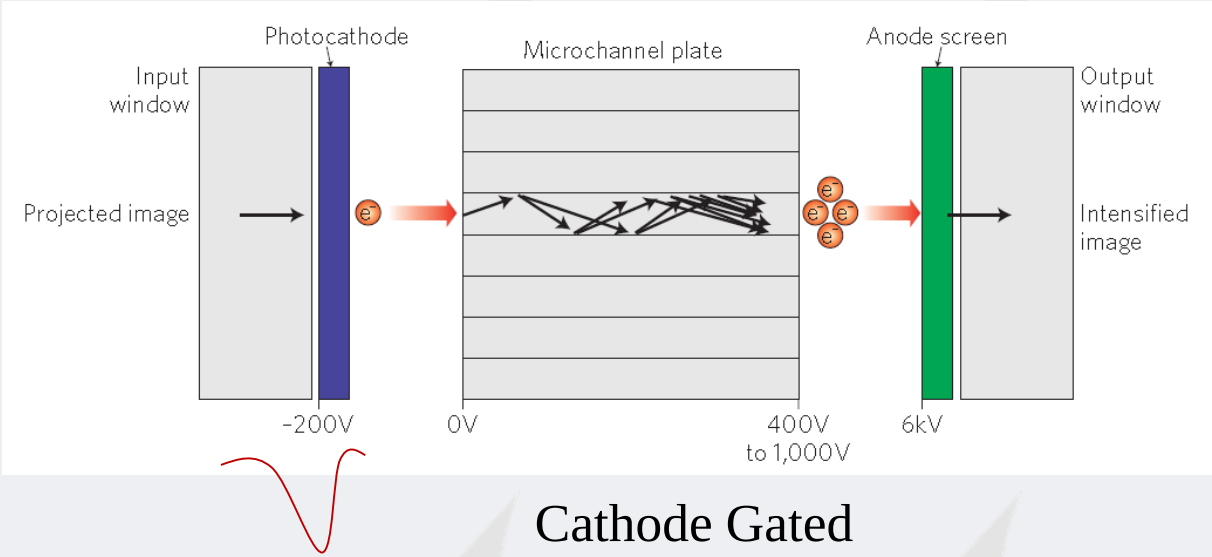




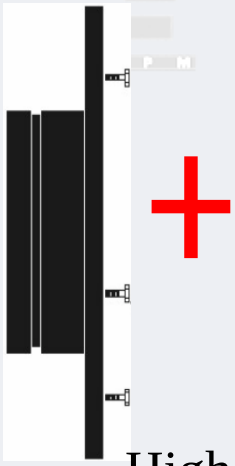
Requirement for prototype of 2018

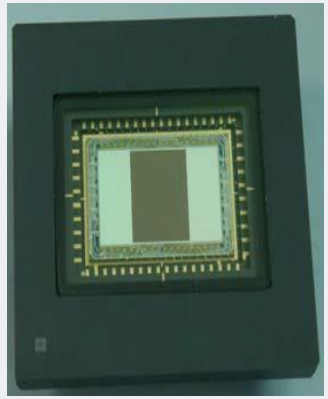
Frame rate	>500 fps
Dynamic range	Low output channel 50-5e4 P.E.，High 4e4-4e7 P.E.
Fiber channel	500ch /camera
Min signal	50 P.E.
Fiber optic tapers	Two stage
Decay of screen	0.1% @ 5ms
Trigger delay of IIT	<1us
sCMOS noise	No comment-mode noise, no drift with frame rate

IsCMOS Developement

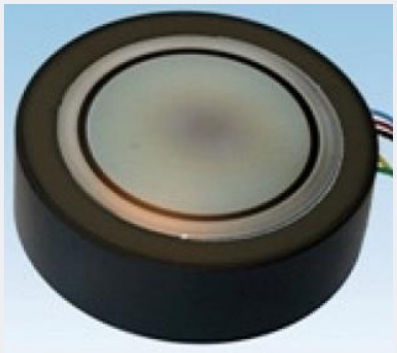


Cathode Gated Intensifier



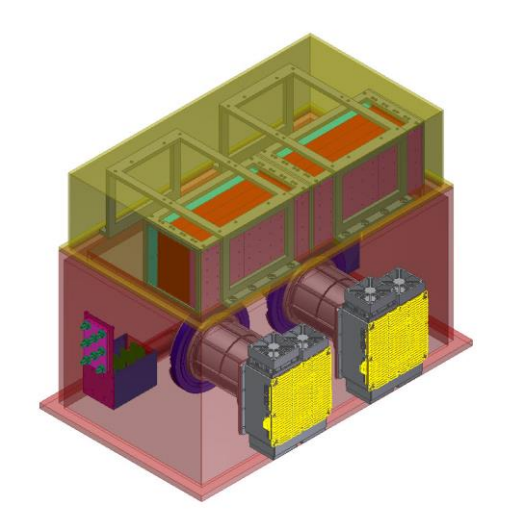


High frame rate and large area sCMOS

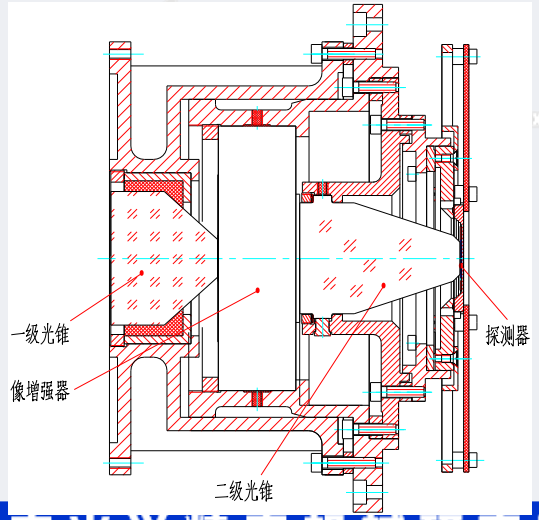


Fiber optical taper

What's new in IsCMOS of 2018



- ✓ Two IsCMOS cameras
- ✓ Low noise driver circuit board for sCMOS Chip
- ✓ FPGA program upgrade
- ✓ IIT with detached HVP of ultralow ripple noise
- ✓ Optimized fiber optic tapers
- ✓ Optimized CMOS chip cooling system



Prograss of sCMOS camera subsystem

Progress made by 2018 sCMOS as compared to the 2015 CCD and 2017 sCMOS sub-system:

compared to the 2015 CCD

- Electronic Shutter
- Better Dynamic Range
- Better Linearity
- Better Pixel response uniformity

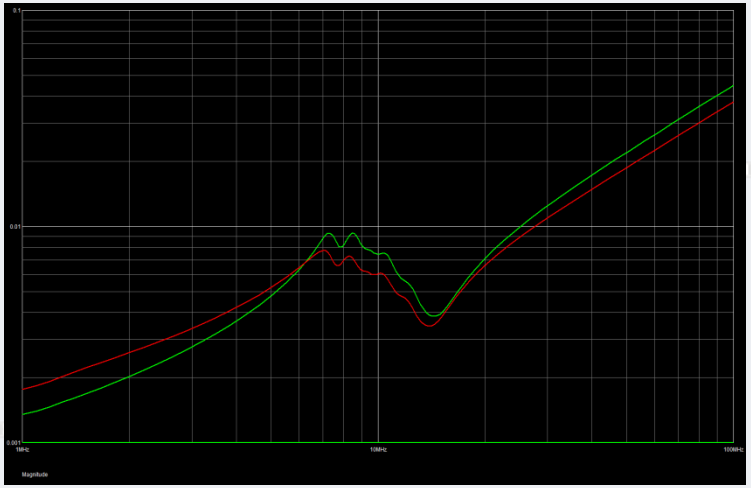
compared to the 2017 sCMOS

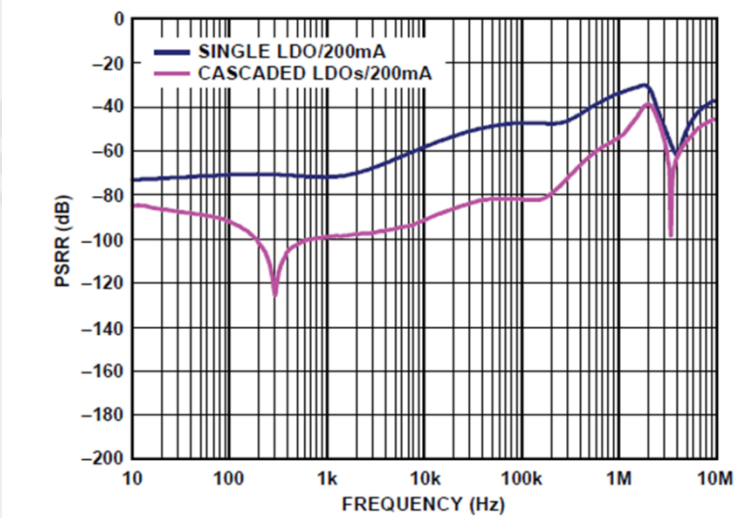
- Smaller Latency (only 300ns)
- Lower Noise (< 2e- RMS@14℃)
- Higher Speed (can reach 535fps)
- Larger Memory Buffer (32GB)

sCMOS Design: Extremely low noise

In critical parts, ripple smaller than 15uV. Extremely low noise made by:

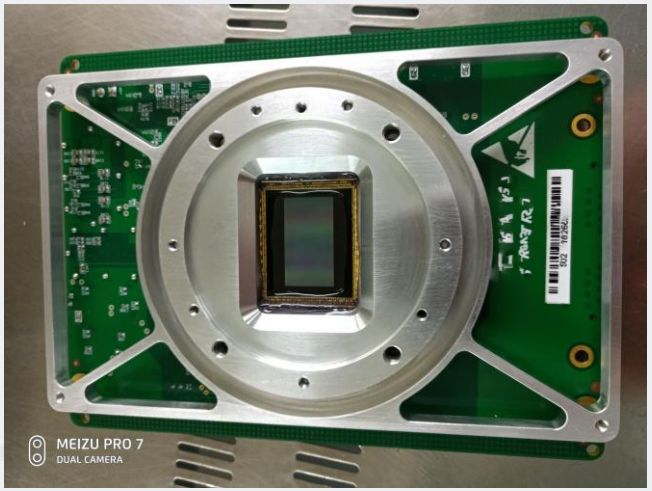
- Shielded DC-DC circuit to reduce ElectroMagnetic Interference
- Cascade LDO to improve PSRR
- Wider bandwidth in circuit for better frequency response

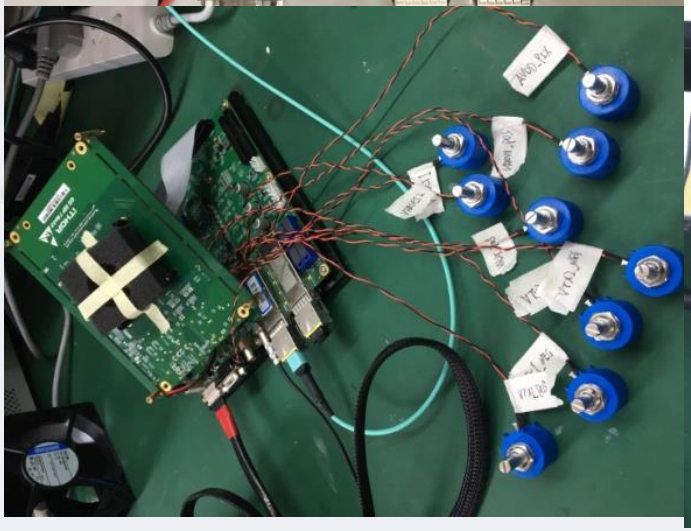




PSRR of a Single LDO and Cascaded LDOs

sCMOS Design: composition of sCMOS Module

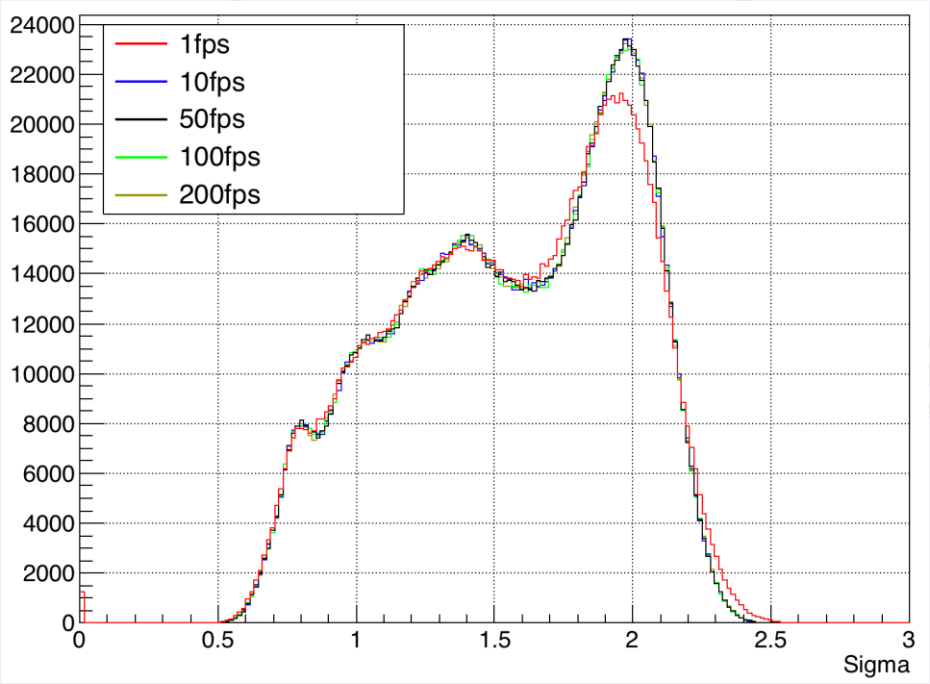


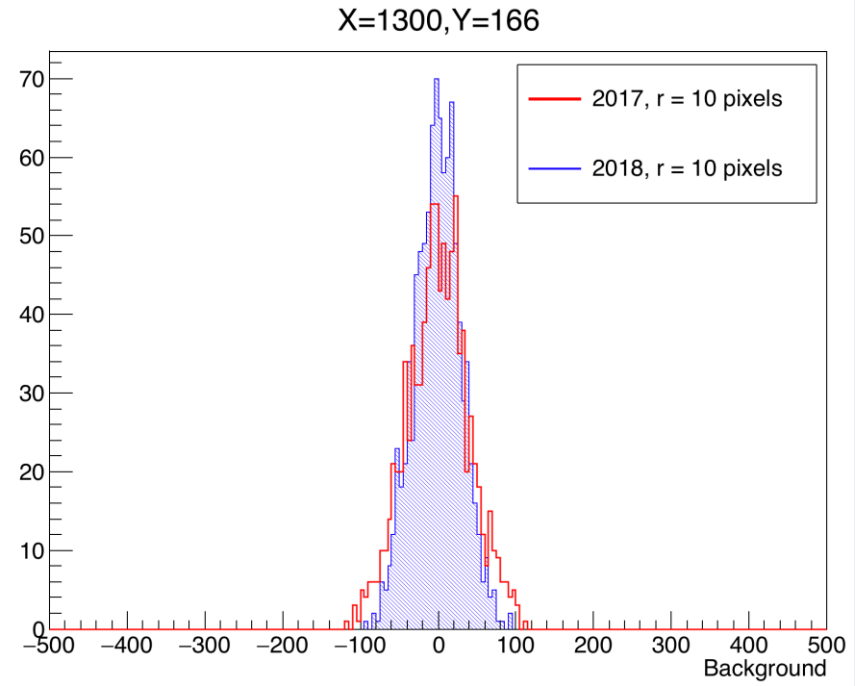


sCMOS Design: Extremely low noise

- Removed the noise in low frame rate by applied the upgrade sensor

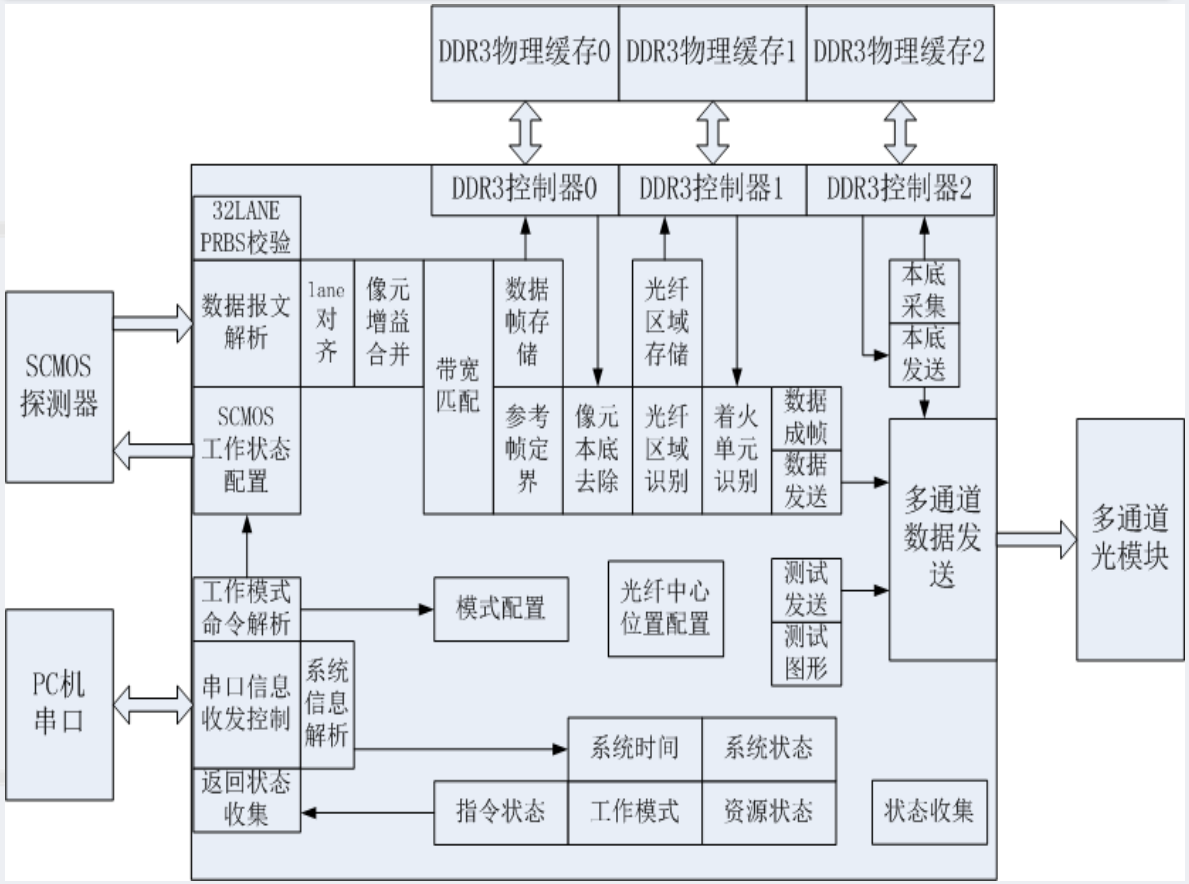
- Reduced the background noise and got a “slim figure” of baseline

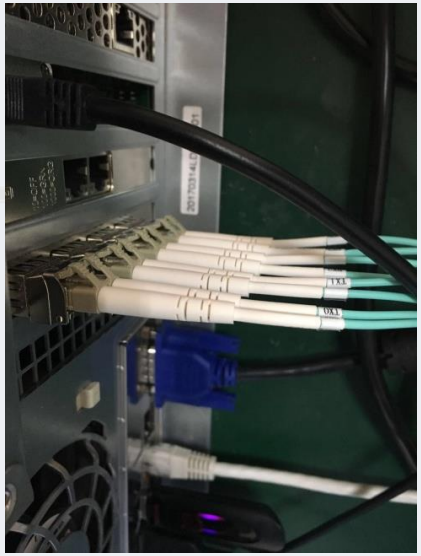




FPGA program upgrade

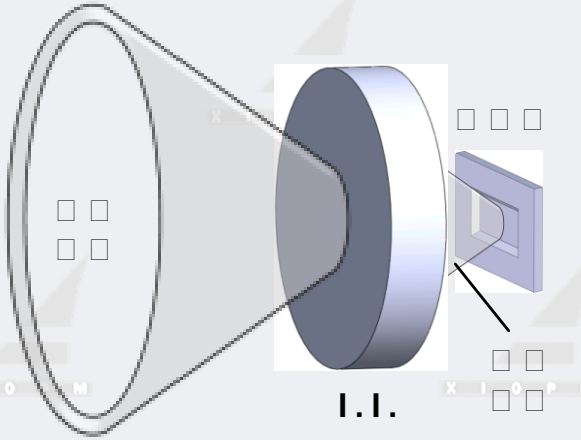
Original data coming out of the sCMOS is about 65Gbit per second. In the sCMOS module, it have to deal with such numerous data. After the processing logic and circuits, the data reduced to 10Gbit per second. Below is the architecture of the FPGA real time processor.





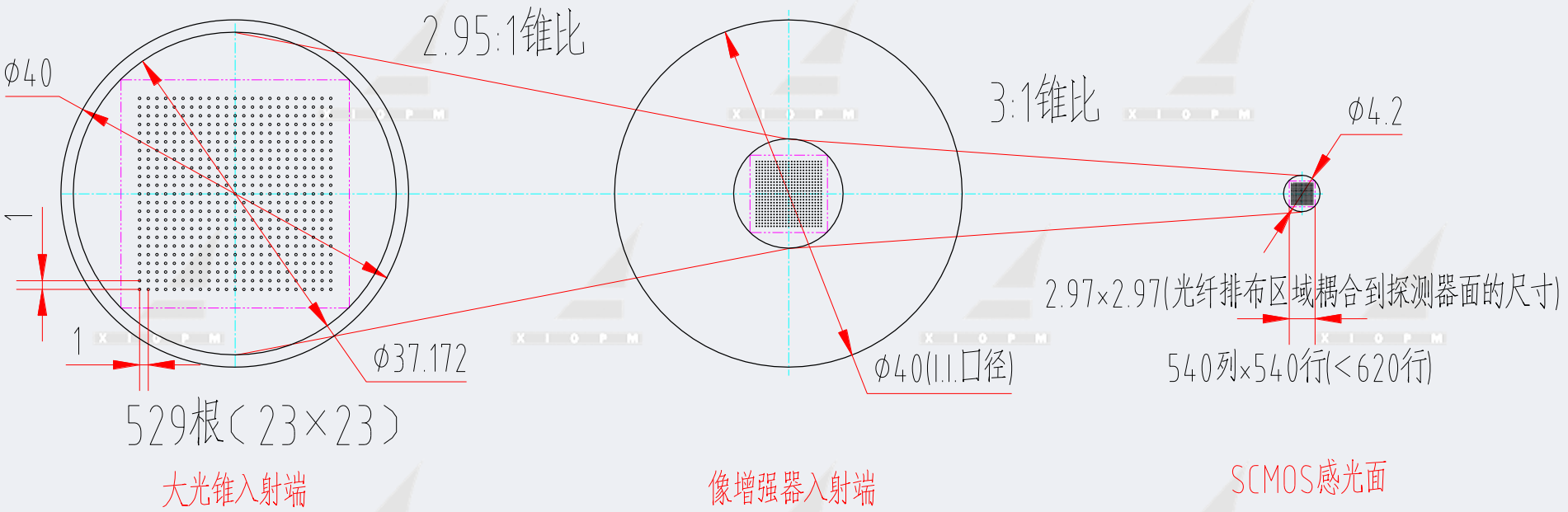
Fiber optic tapers of 2018

WLS fibers：500 channels per camera（250ch 2017）

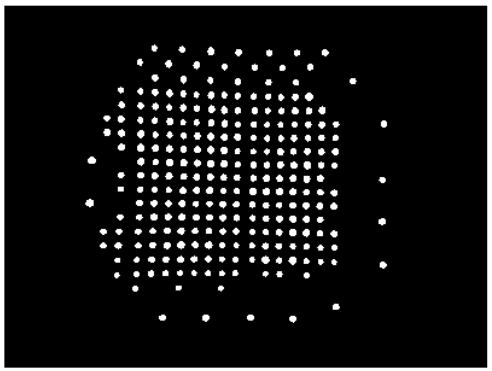


500 channels；光纤中心距1mm；丝径0.3mm	
Diameter of front FO taper (mm)	40
Front taper Ratio of large and small ends	2.95:1
Diameter of Image intensifier (mm)	40
Diameter of rear FO taper (mm)	40
rear taper Ratio of large and small ends	3:1
Pixels per channel	20*20pixel/ ch
Pixel size of sCMOS	5.5*5.5 um

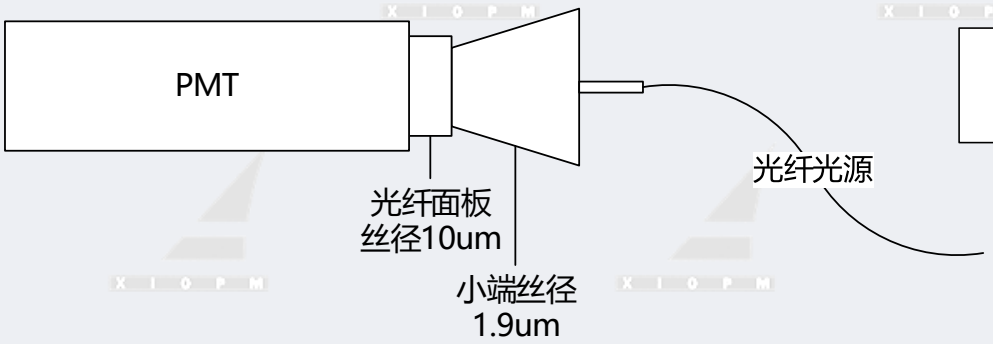
Fiber optic tapers of 2018

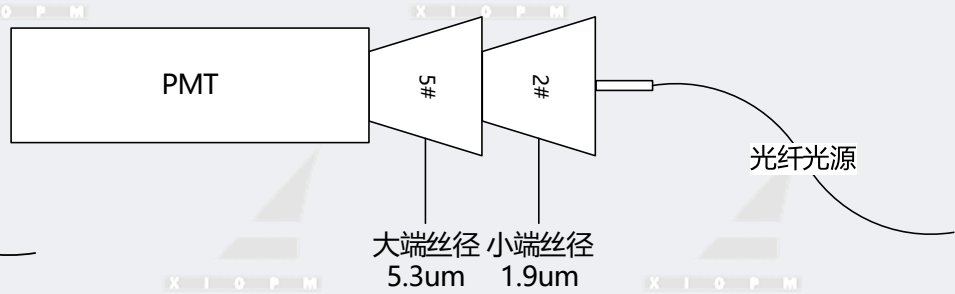


Φ40mm image intensifier, 500FPS(maxim 620 lines of sCMOS), 888 fibers can be arranged.



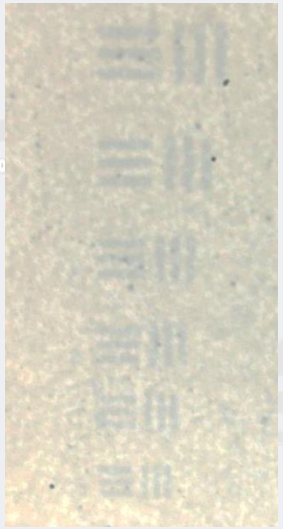
Transmission of FO taper

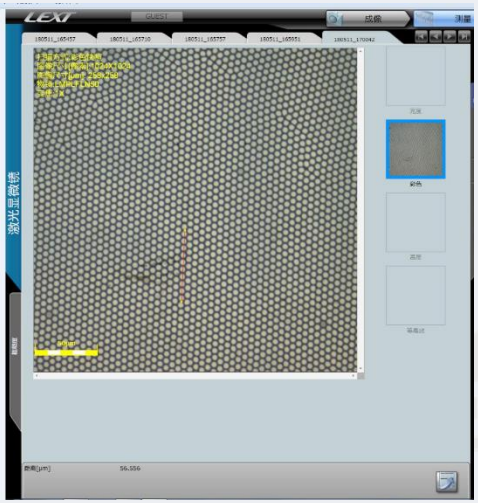




Series No.	Position1	Position2	Position3	Position4	Position5	Uniformity	LED Power	Trans.
1804161104	2.091	2.095	2.078	2.074	2.076	0.995427	5.933	0.351053
1804161105	1.957	1.968	1.951	1.955	1.962	0.99664	5.933	0.33012
1804161101	2.038	1.993	2.033	2.047	2.029	0.989799	5.933	0.341817
1805251101	1.877	1.893	1.889	1.894	1.898	0.995745	5.933	0.318591

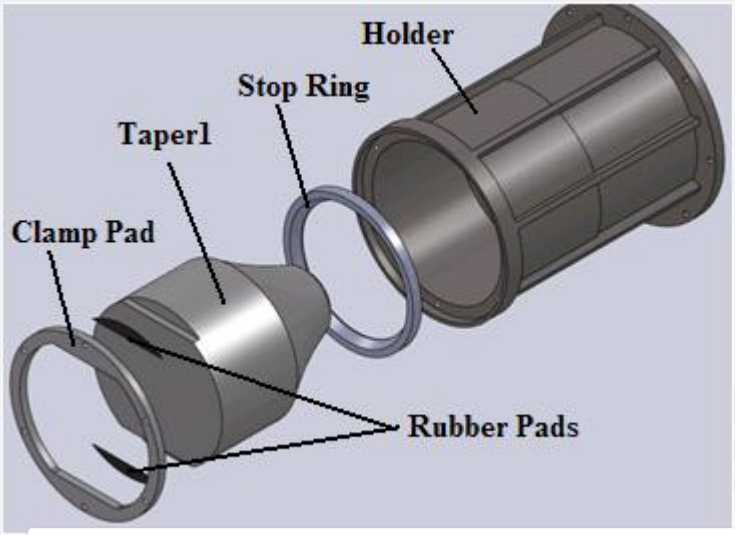
Imaging testing of FO tapers

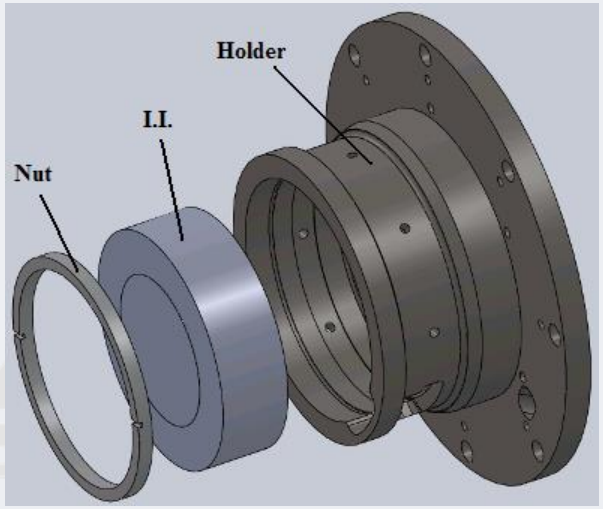


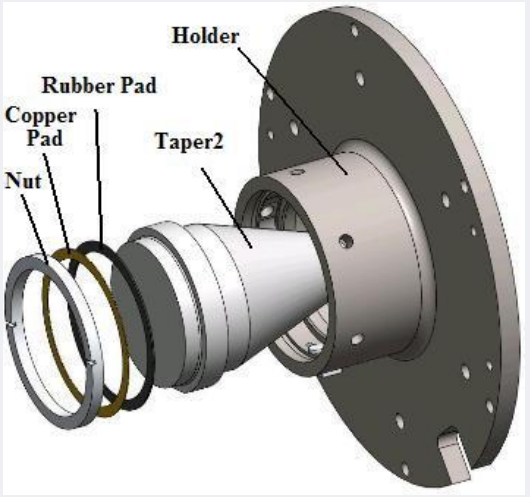


Series No.	Front to end spatial R lp/mm	end to front spatialR lp/mm	Front fiber Core um	End fiber core um	F2E ratio
GZ（W）1804161101	57	57	5.65	1.76	3.2：1
GZ（W）1804161102	57	57	5.5	1.9	2.9：1
GZ（W）1804161103	57	57	5.4	1.79	3.01: 1
GZ（W）1804161104	57	57	5.58	1.9	2.93: 1
GZ（W）1804161105	57	57	5.3	1.75	3.0：1

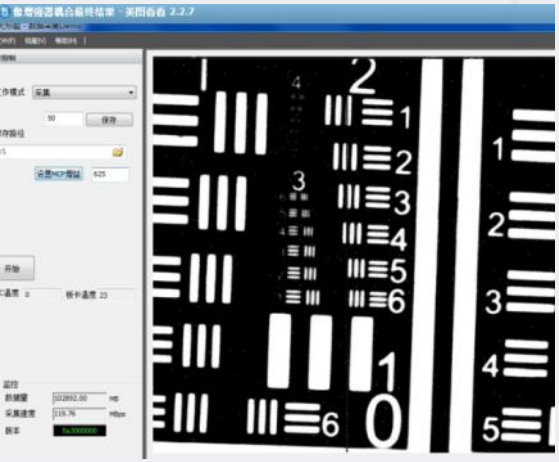
Taper Coupling

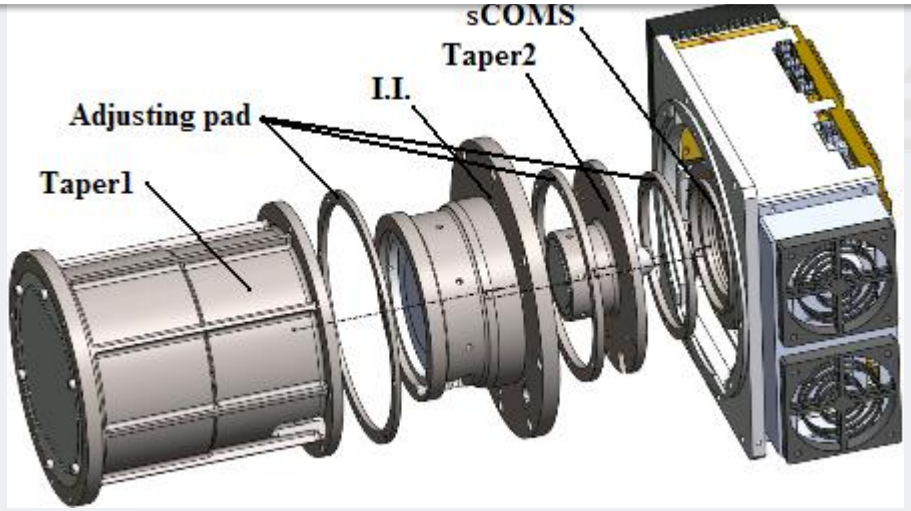


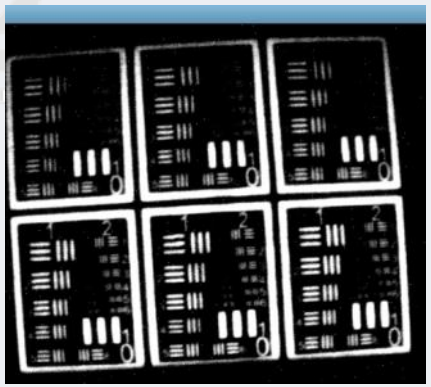




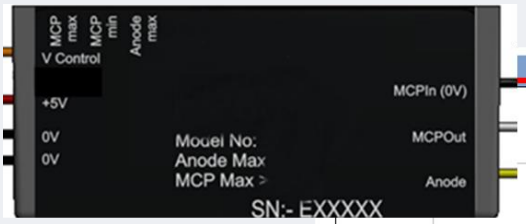
Coupling gap is about 10μm.



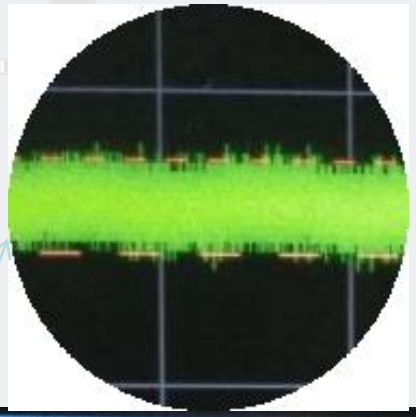


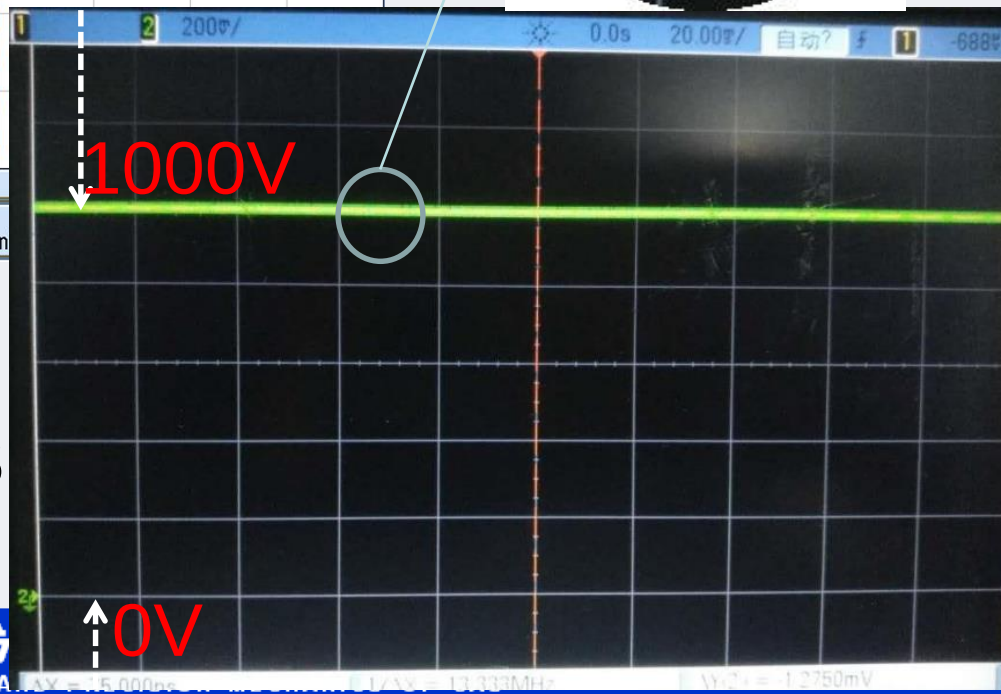


High Voltage PSU: MCP gain



2017





GainVoltage:1000V

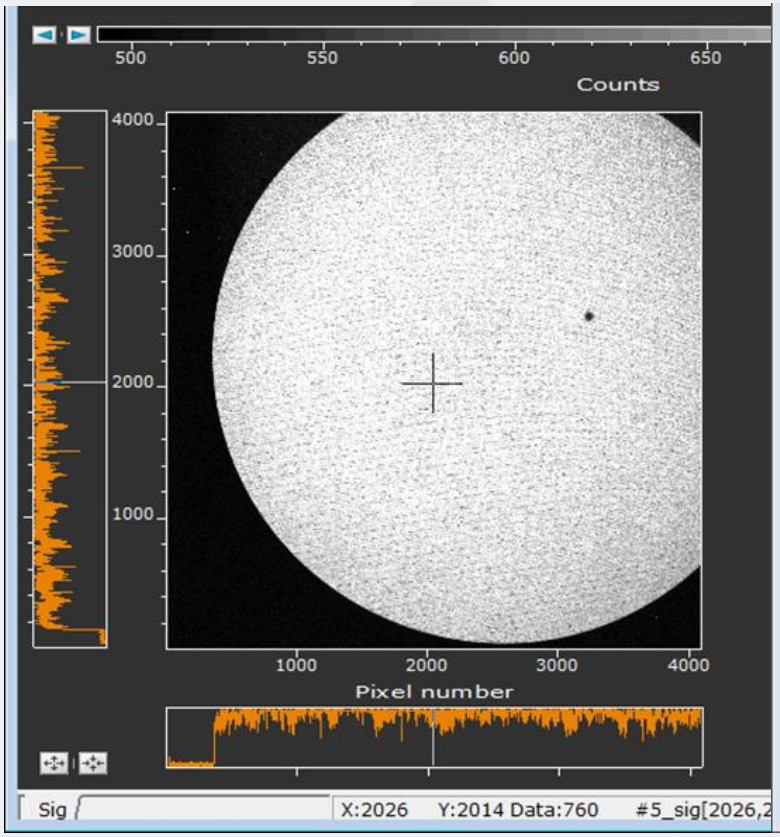
Voltage ripple:＜0.8V

2018

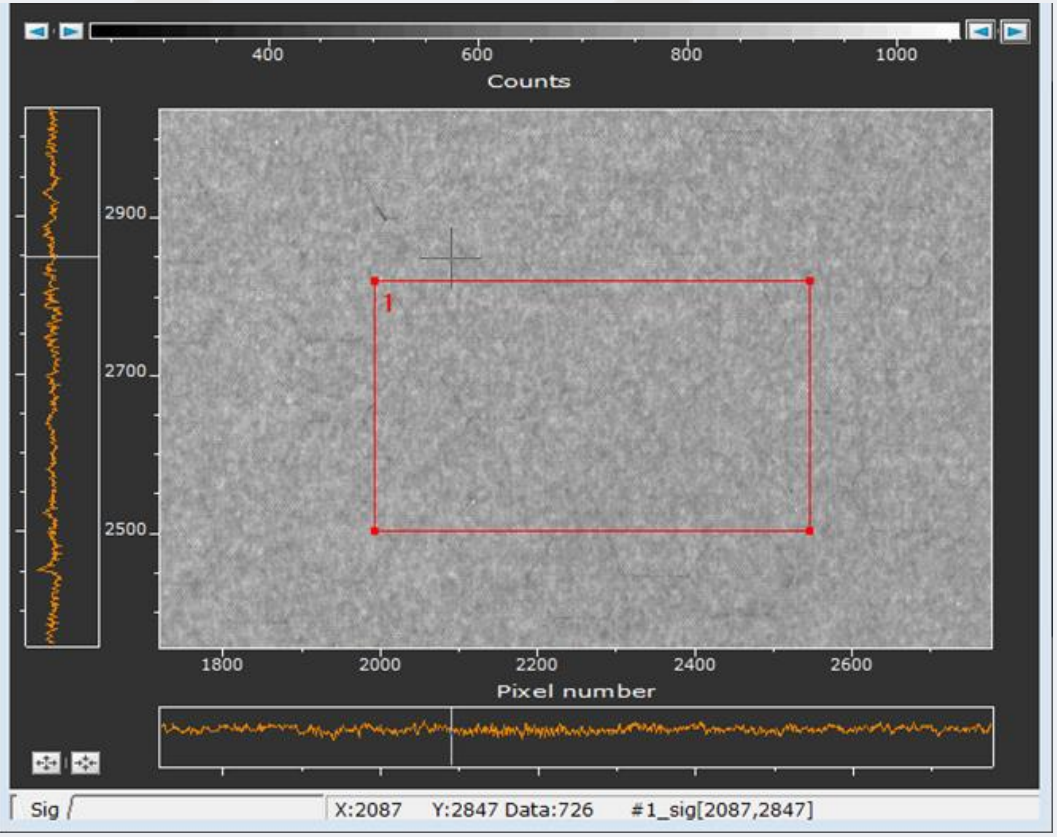
Nonuniformity of IsCMOS camera

XIOPM

Nonuniformity:2.1%-5.2%



Overall picture

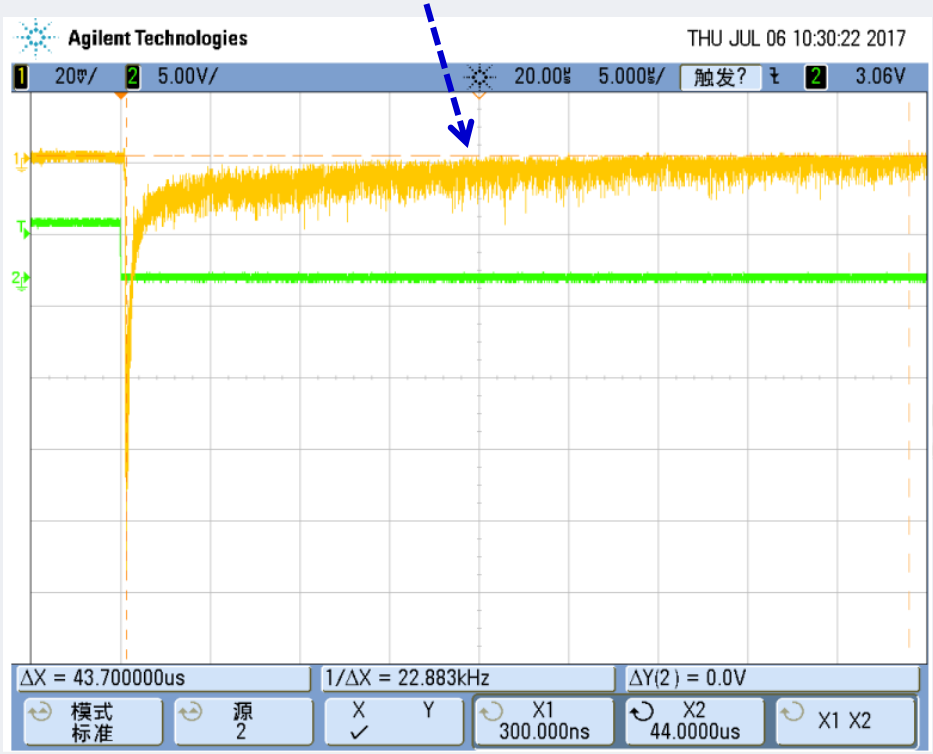


Partial magnification picture

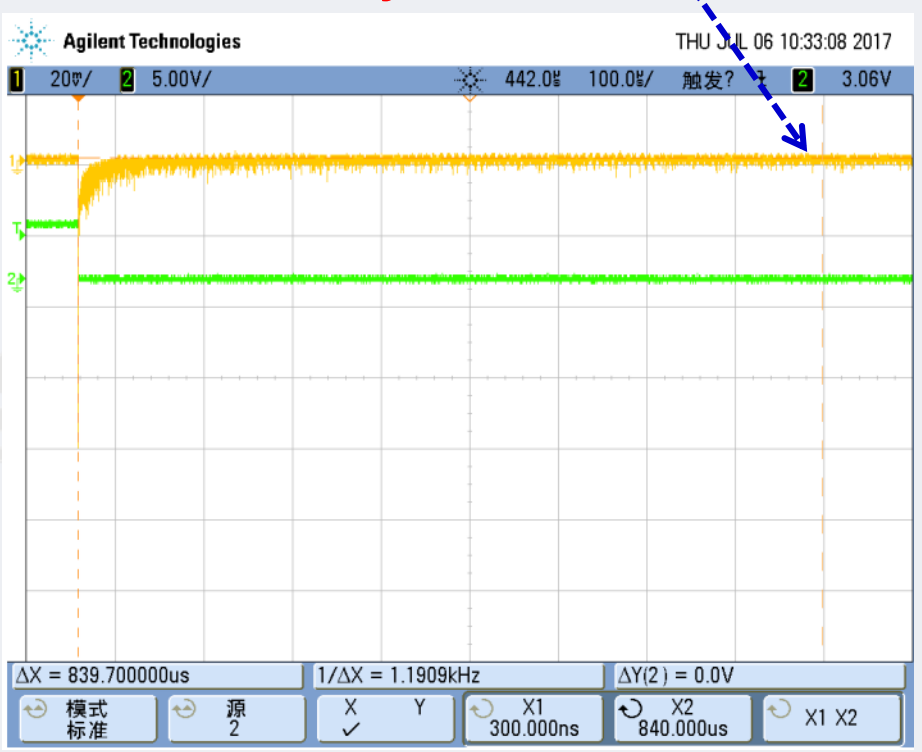
Phosphor screen: decay time

95% Energy is concentrated in 100us, and the 840us decay time match with sCMOS frame rate(500fps)

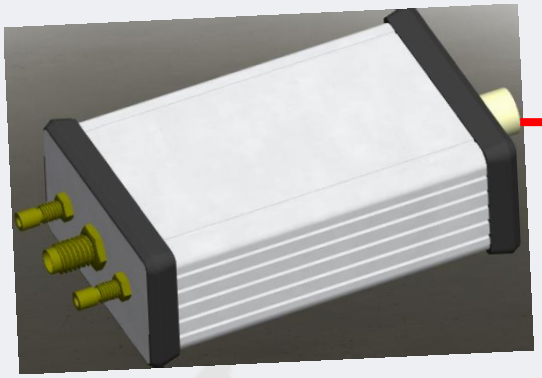
~100us

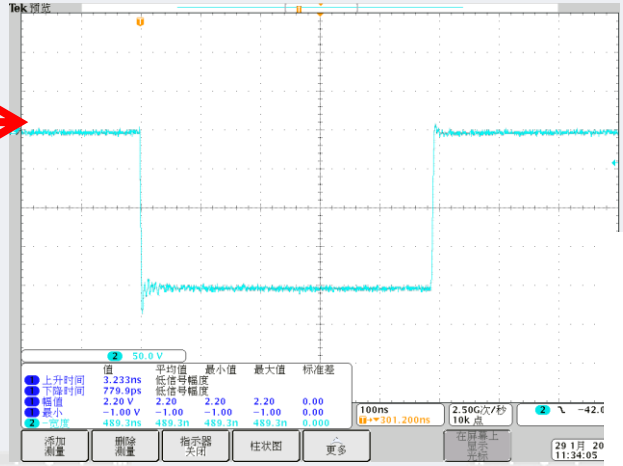


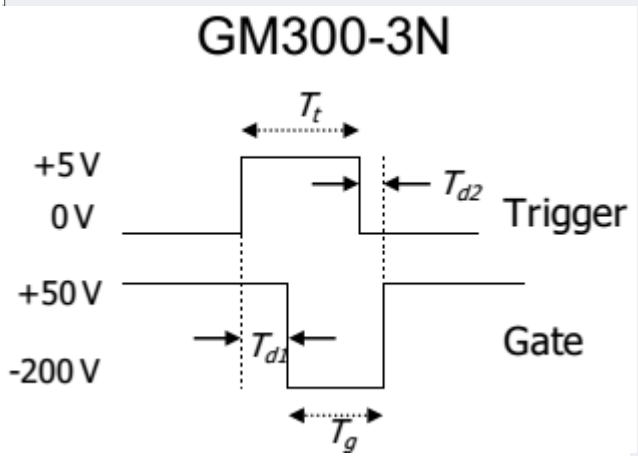
decay time ~840us



Gated Unite for photocathode



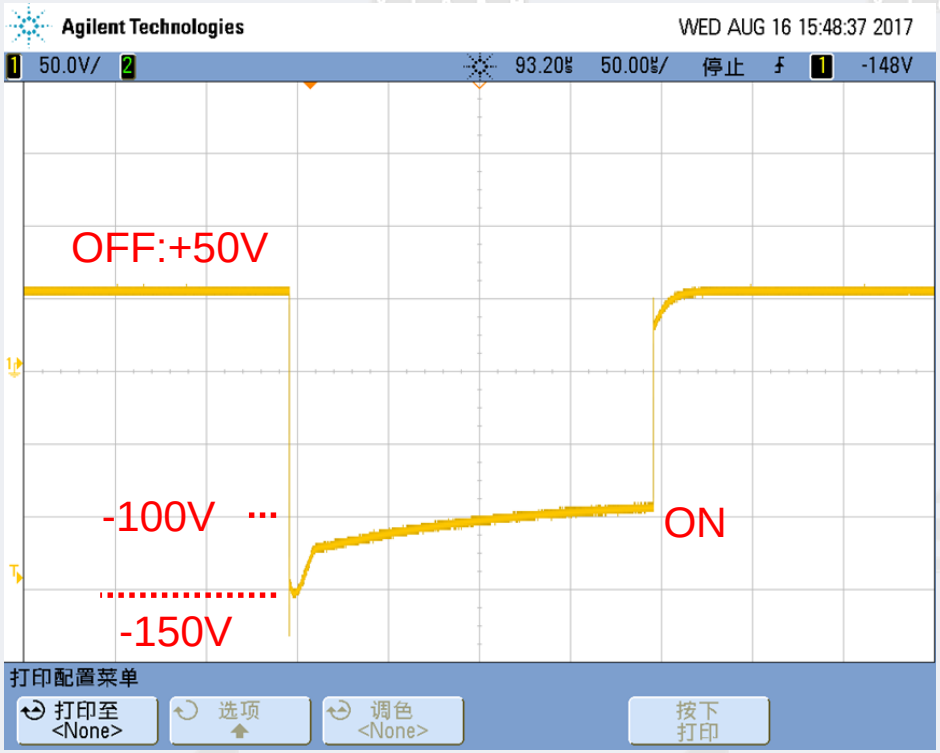


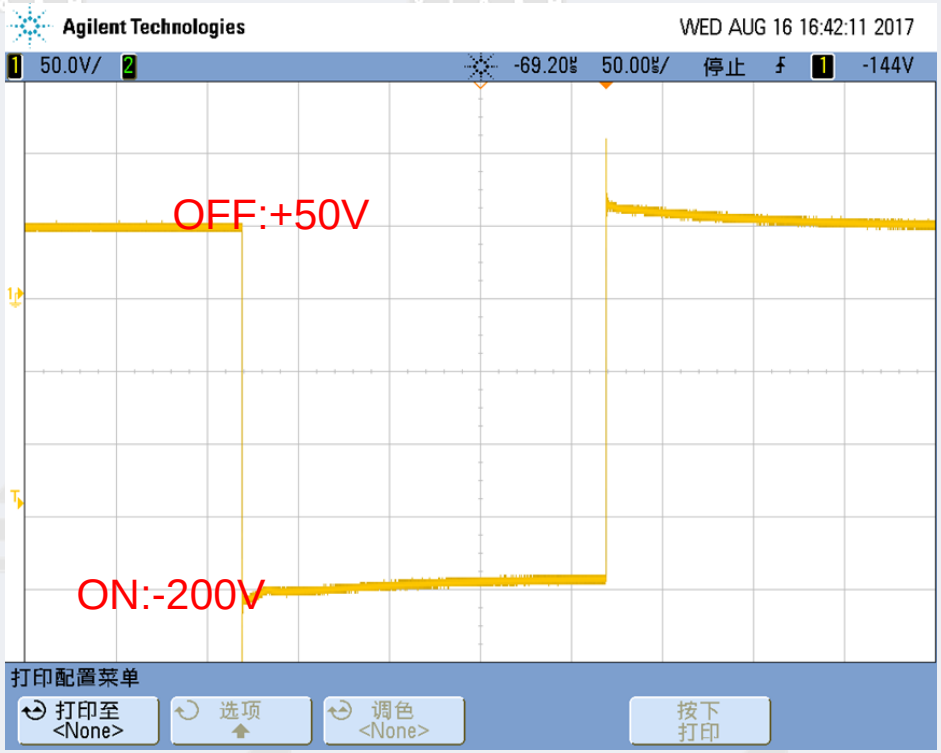


Typical Timing Parameters

Leading Edge Propagation Delay	T_{d1}	50 ns
Trailing Edge Propagation Delay	T_{d2}	40 ns
Trigger / Gate Offset Time Tt - Tg	T_{d1} - T_{d2}	10 ns
Minimum Gate Width in Inverted Mode	T_g	50 ns
Propagation Delay Temperature Co-efficient		40 (± 5) ps / °C
Gate Width Temperature Co-efficient		± 10 ps / °C

Gated Unite for photocathode

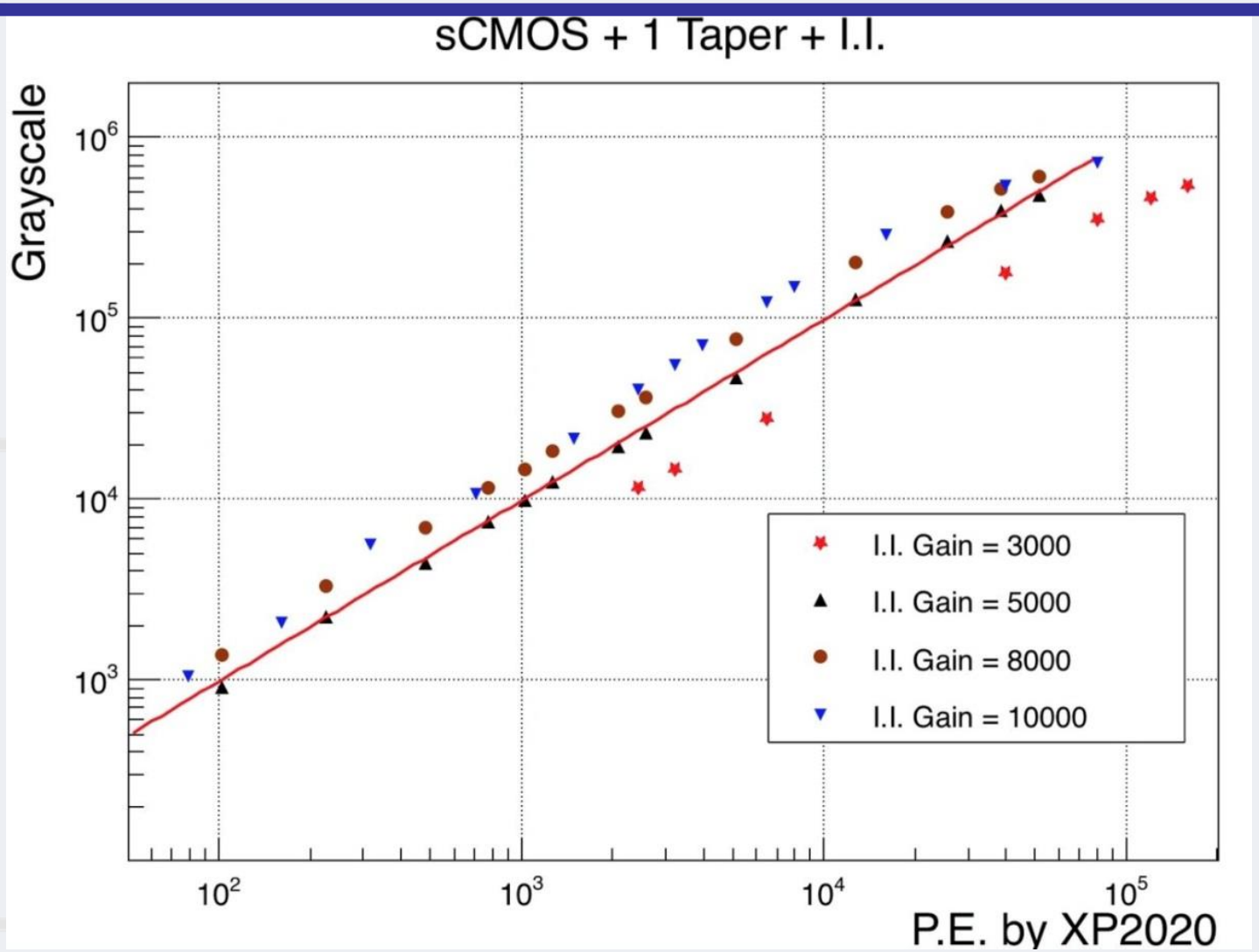




Impedance mismatching

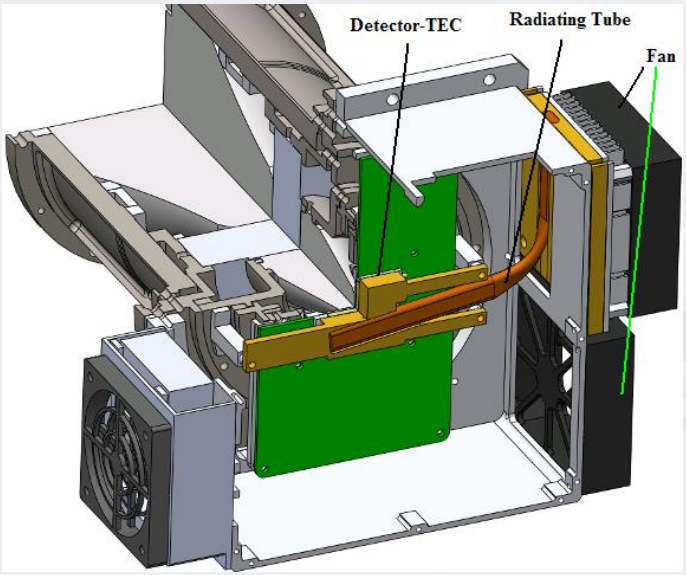
Impedance matching

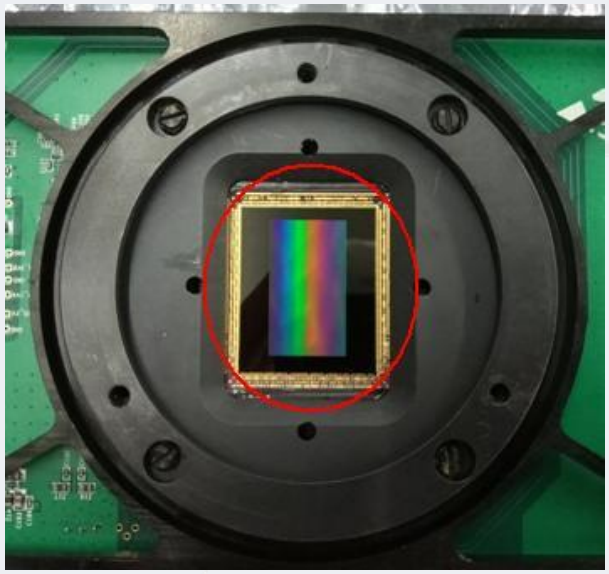
Dynamic range

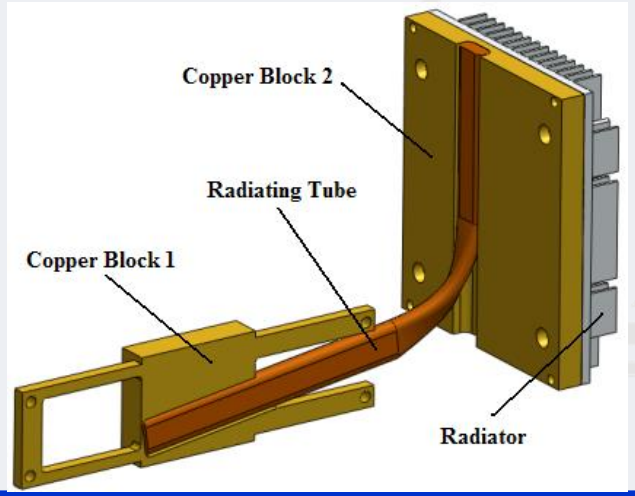


Dynamic range: ~1000:1

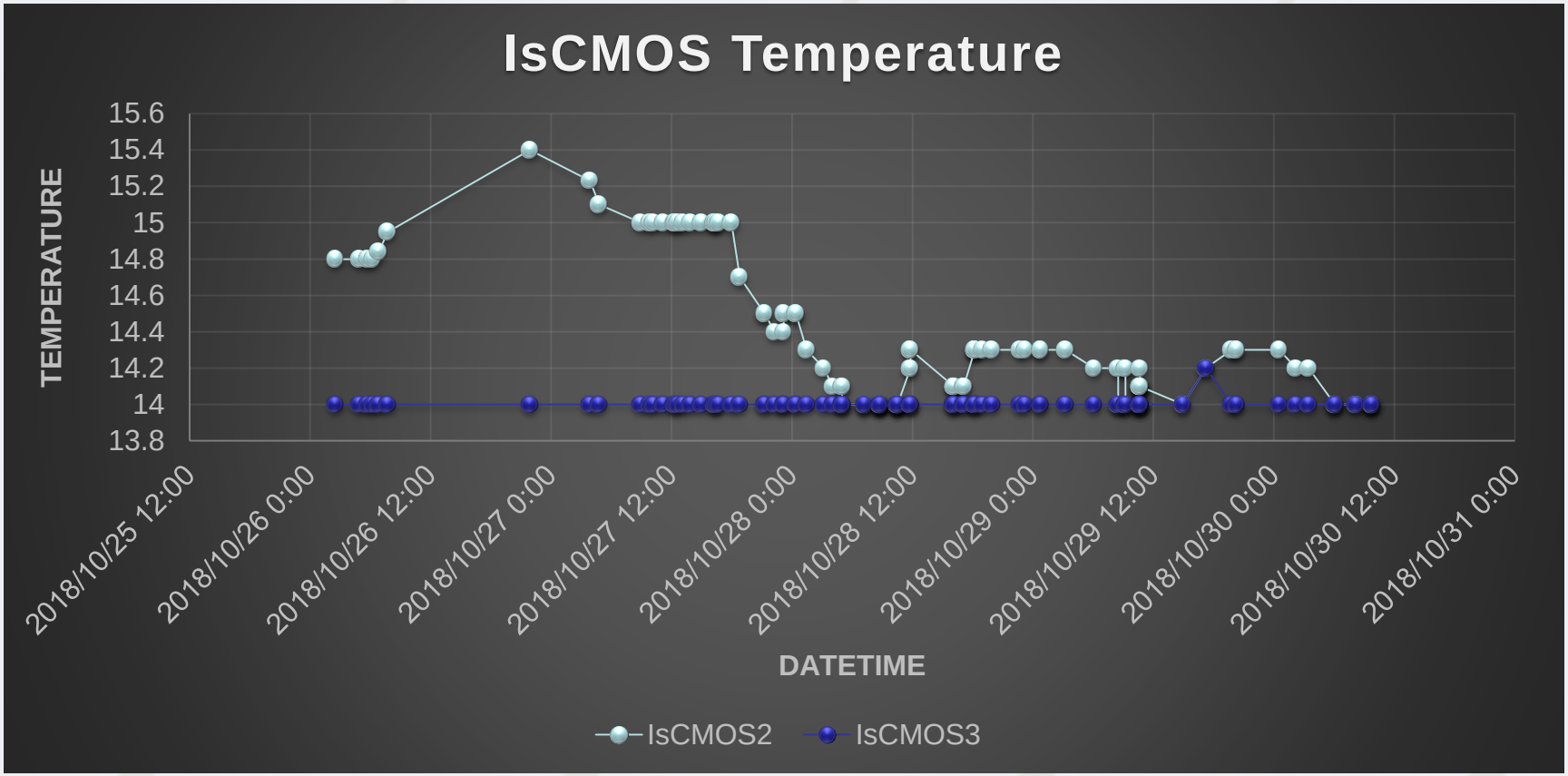
Cooling Design



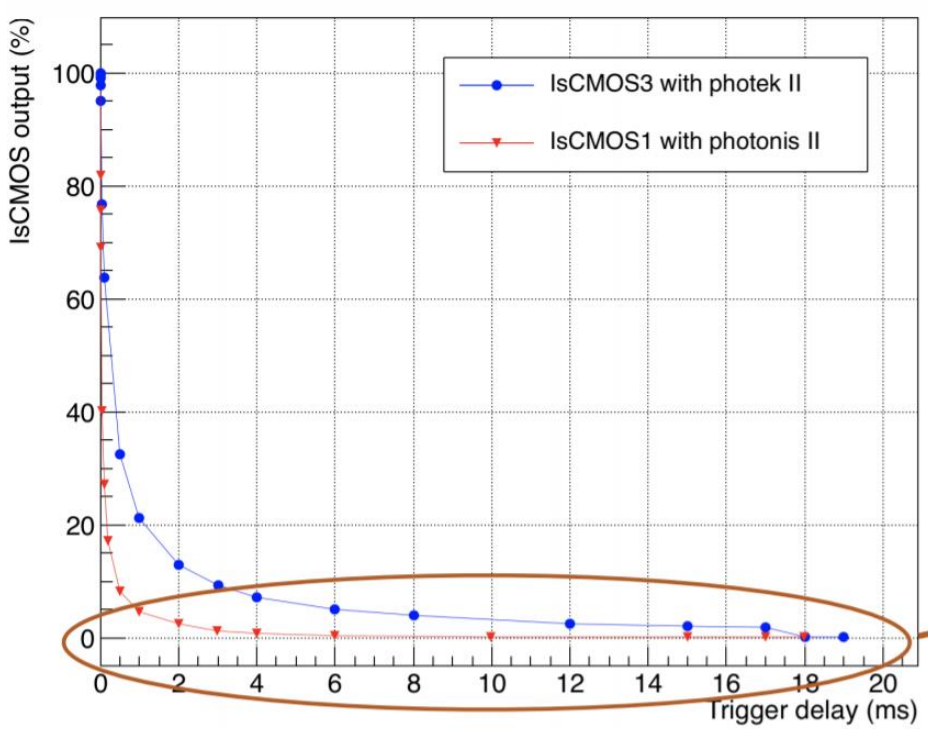


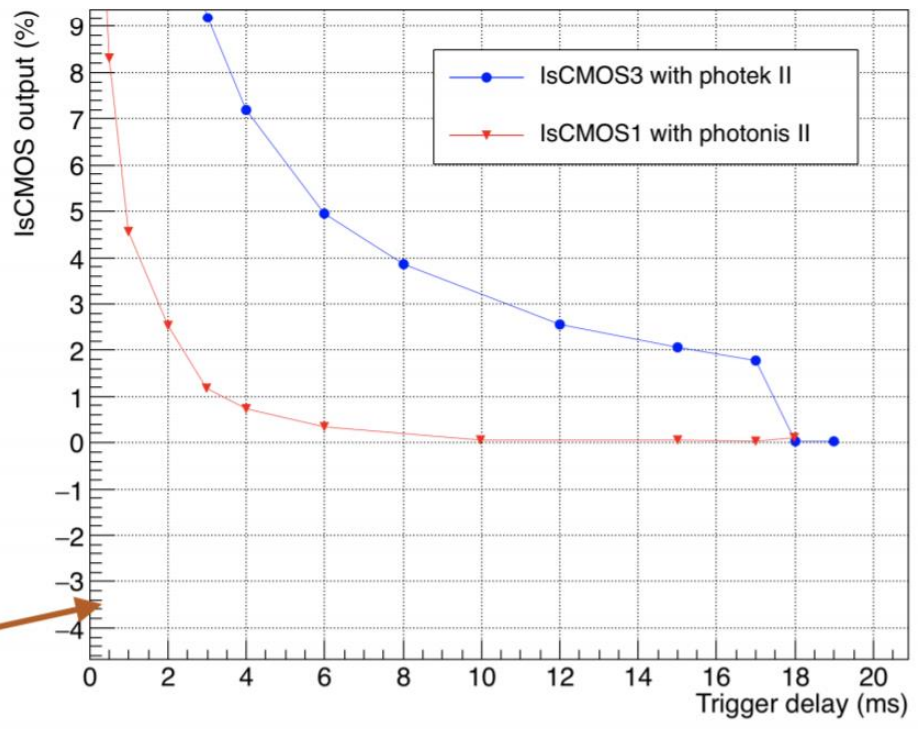


sCMOS chip temperature

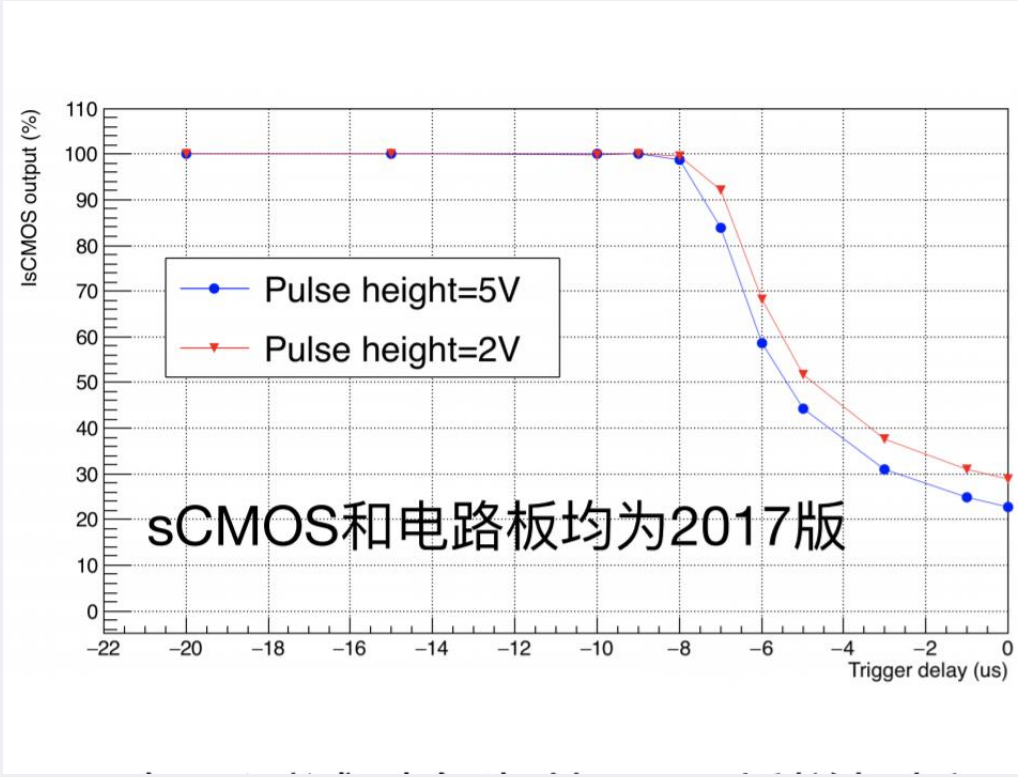


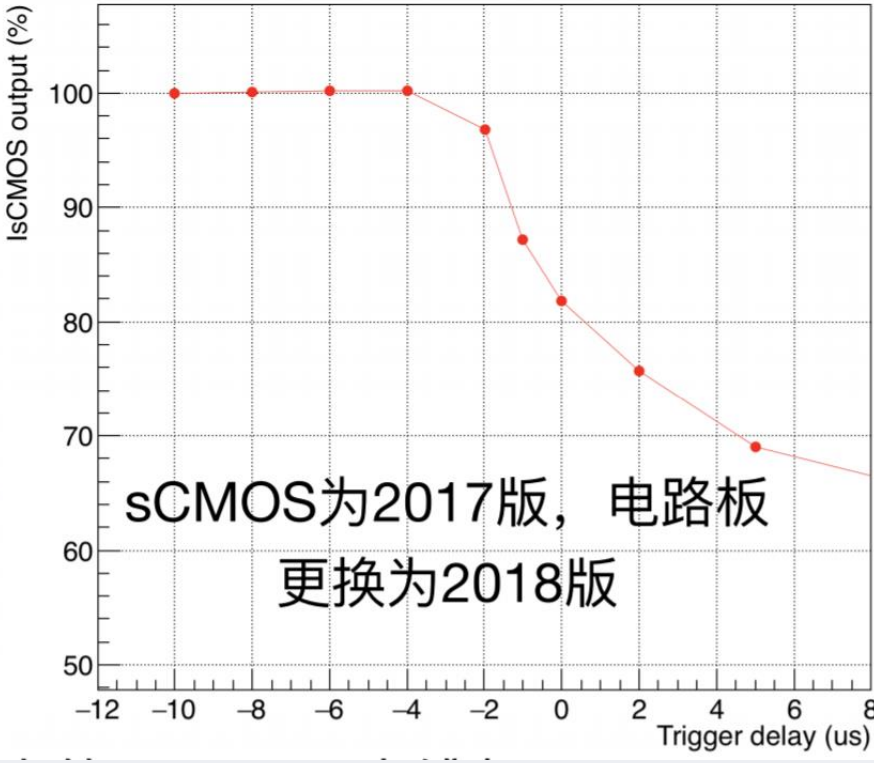
The afterglow of IIT



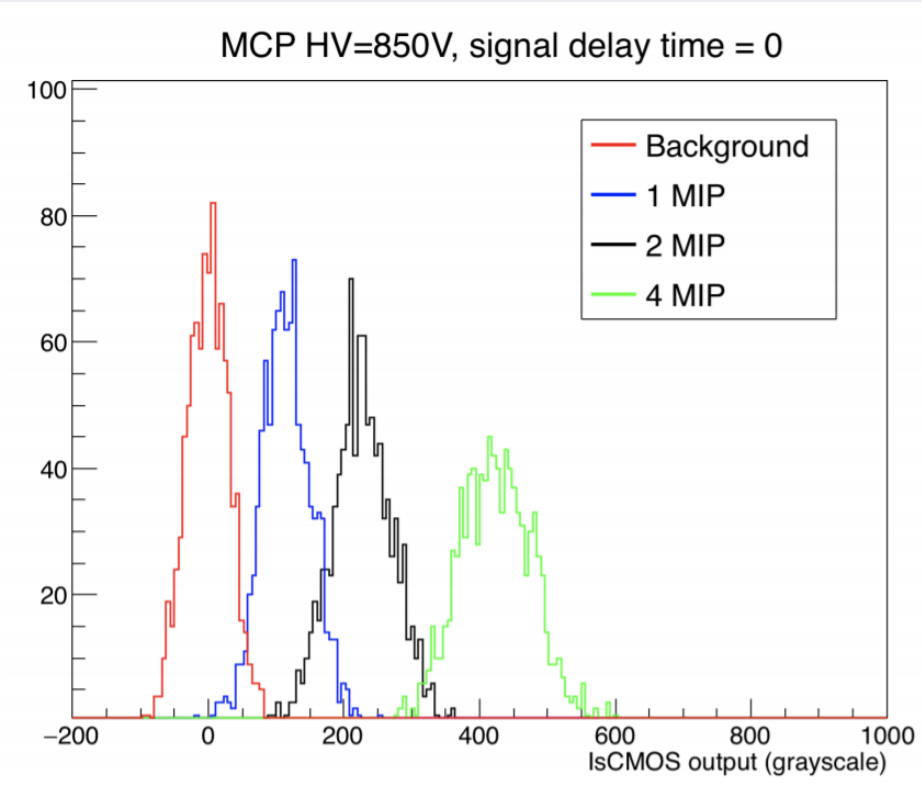


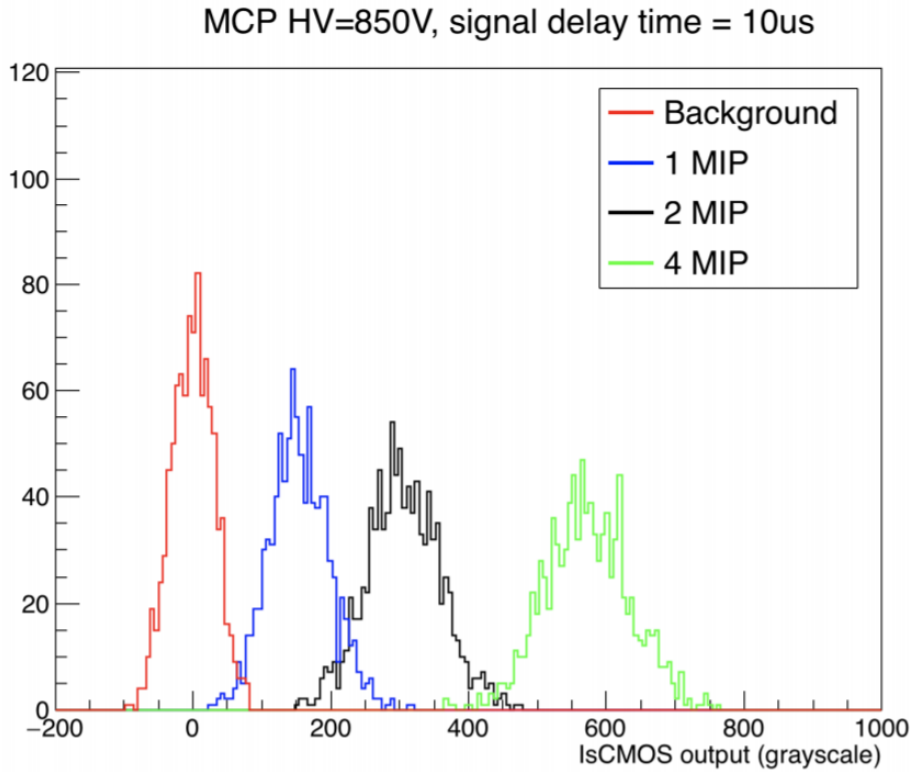
The Trigger On delay of sCMOS





The MIP signal response of IsCMOS camera





Conclusion

XIOPM

We have developed I.I. which satisfies most of our requirements

- sensitivity
- dynamic range improvement
- trigger off/on delay time
- Gain stability

Thanks for your attention