NEW CALOCUBE READ-OUT SYSTEM

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CIEMAT

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HiDRA2 Chip

INFN Istituto Nazionale di Fisica Nucleare

HiDRA2 DATASHEET

Revision 1.0 – March 19th, 2018

Gianluigi Zampa

HiDRA2: High Dynamic Range Amplifier frontend ASIC

Specifications

Number of channels: 16

Supply voltage: 3.3 V

Analog functions: automatic double-gain pulse reset Charge Sensitive Amplifier (CSA), calibration circuitry (registers and capacitors), Correlated double sampling, Self-triggering circuitry, and output multiplexer

Power consumption: 3.75 mW/ch (common circuitry included), typical corner

Dynamin range:

- High gain: ≈ 2.7 pC (560 MIP on 380 µm Si sensors)
- Low gain: ≈ 52.6 pC (11000 MIP on 380 µm Si sensors)

Linearity

- High gain: ± 0.3 %
- Low gain: ± 0.6 %

Calibration capacitance: 1.6 pF

Equivalent noise charge: 2280 e^- + 7.5 e^-/pF RMS (CDS time constant of 10 us)

CSA minimum reset pulse duration: t_{CSA_reset} = 150 ns

CSA settling time (1 %): $t_{S\_CSA,1\%}$ = 400 ns @ C_D = 300 pF

CDS external pedestal reference: 900 mV

CDS reset duration: t_{CDS_reset} = t_{CSA_reset} + 400 ns @ C_D = 300 pF

Self-trigger gain: ×10

Self-trigger threshold: set by an external resistor, 2 adjustment bits (≈ ×1, ×1.5, ×2, and ×2.5)

Self-trigger comparator hysteresis: 16 mV ± 2.3 mV r.m.s.

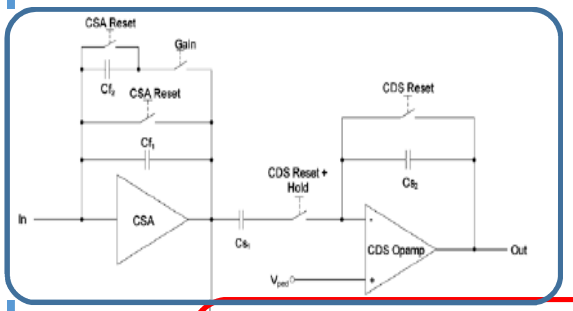
Self-trigger response time: ≤ 500 ns for signals 10 mV larger than the effective threshold (equal to the threshold voltage plus the comparator hysteresis)

Output buffer driving capability: 20 kΩ // 100 pF

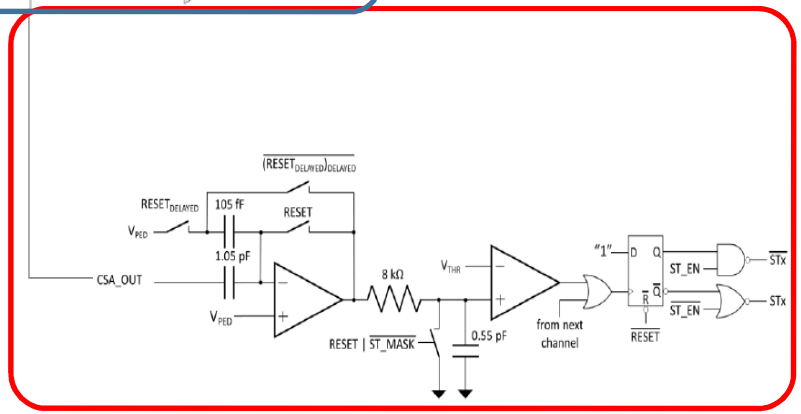
Output settling time (1 %): $t_{S\_OUT,1\%}$ = 80 ns @ C_L = 100 pF

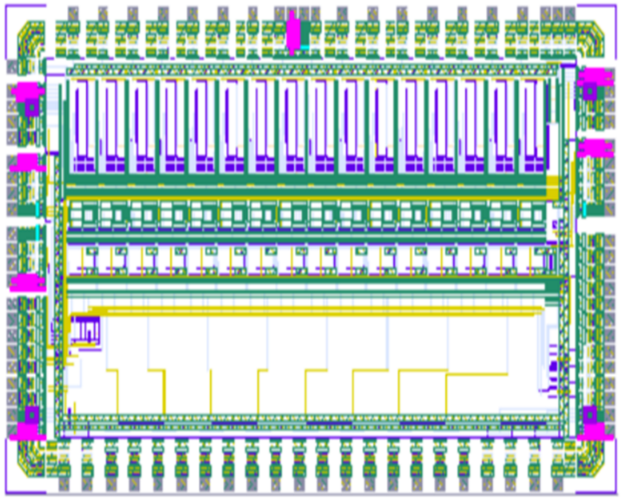
Package: CQFP100 (CQZ10001)

Current System Architecture



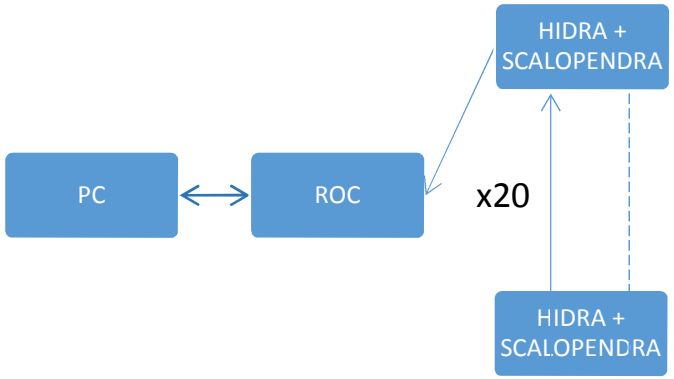
New Self Trigger Stage



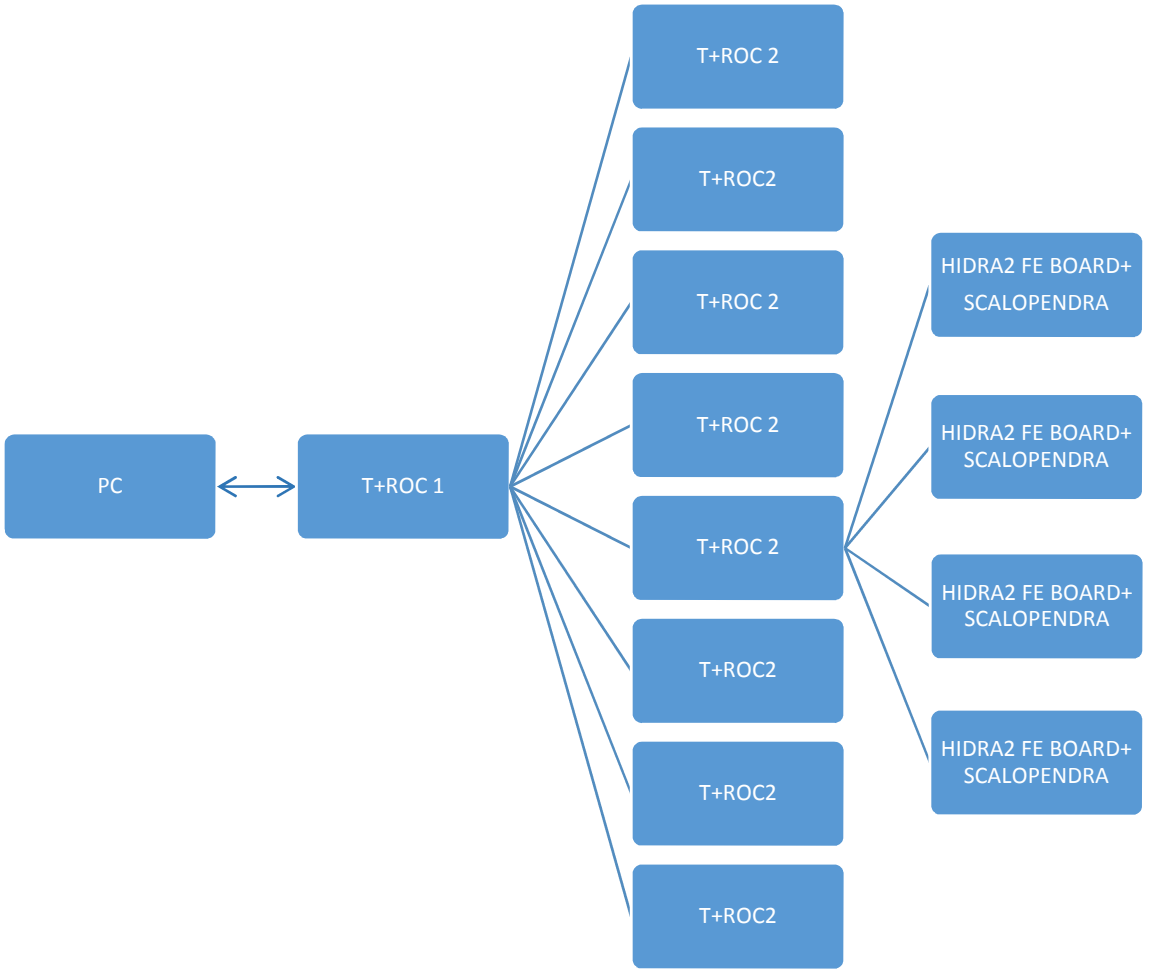


Calocube read-out diagram

Current System Architecture



New System Architecture



COMMAND DISTRIBUTION & CONFIGURATION & TRIGGER IN

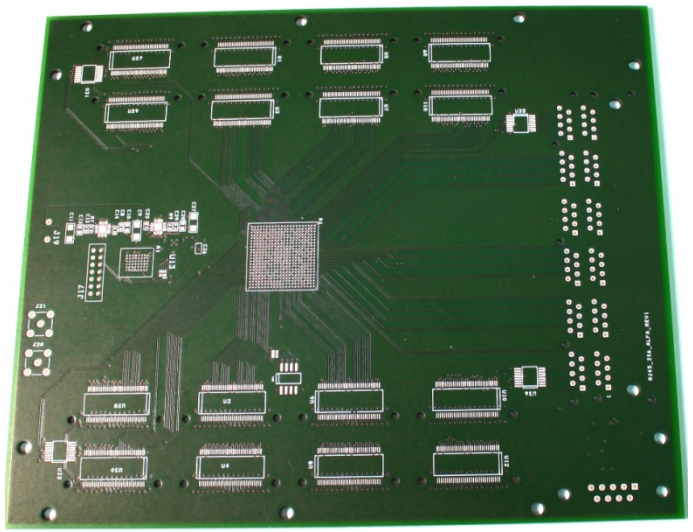
DATA COLLECTION & TRIGGER OUT

Read-out summary

System Characteristic:

- 1 T+ROC1.
- Up to 8 T+ROC2 max.
- Up to 4 Hidra2 FEB/T+ROC2 max.
- 4 Hidra2 ASIC/Hidra2 FEB
- 16 data channels/Hidra2 ASIC
- 8 Trigger channels/Hidra2 ASIC
- 3 Scalopendra Kapton cables / Hidra2 FEB
- LVDS interface between boards.
- Common acquisition sequence to all 4 Hidra2 FEB.
- Single digital read-out (ADC) output per Hidra2 FEB.
- Trigger & calibration masks Daisy-Chained inside each Hidra2 FEB.

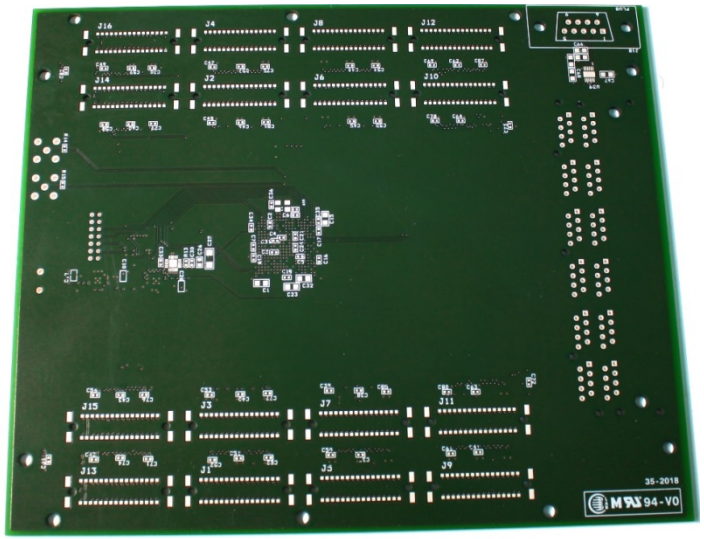
T+ROC2 Description

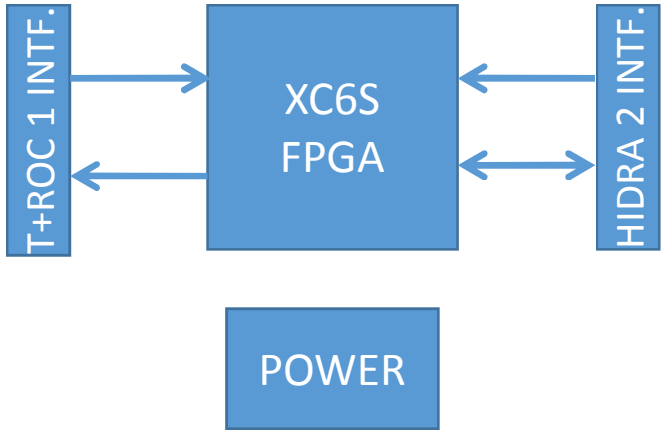


- 15cm x 17cm.
- 6 Layers.
- PCB layout cross-checked with Hidra2 FEB design.
- Firmware developed in a test-board and almost finished.
- XC6S45 Xilinx FPGA.
- Fast Serial link connection to T+ROC 1.
- LVDS connections to HIDRA2 & T+ROC1.

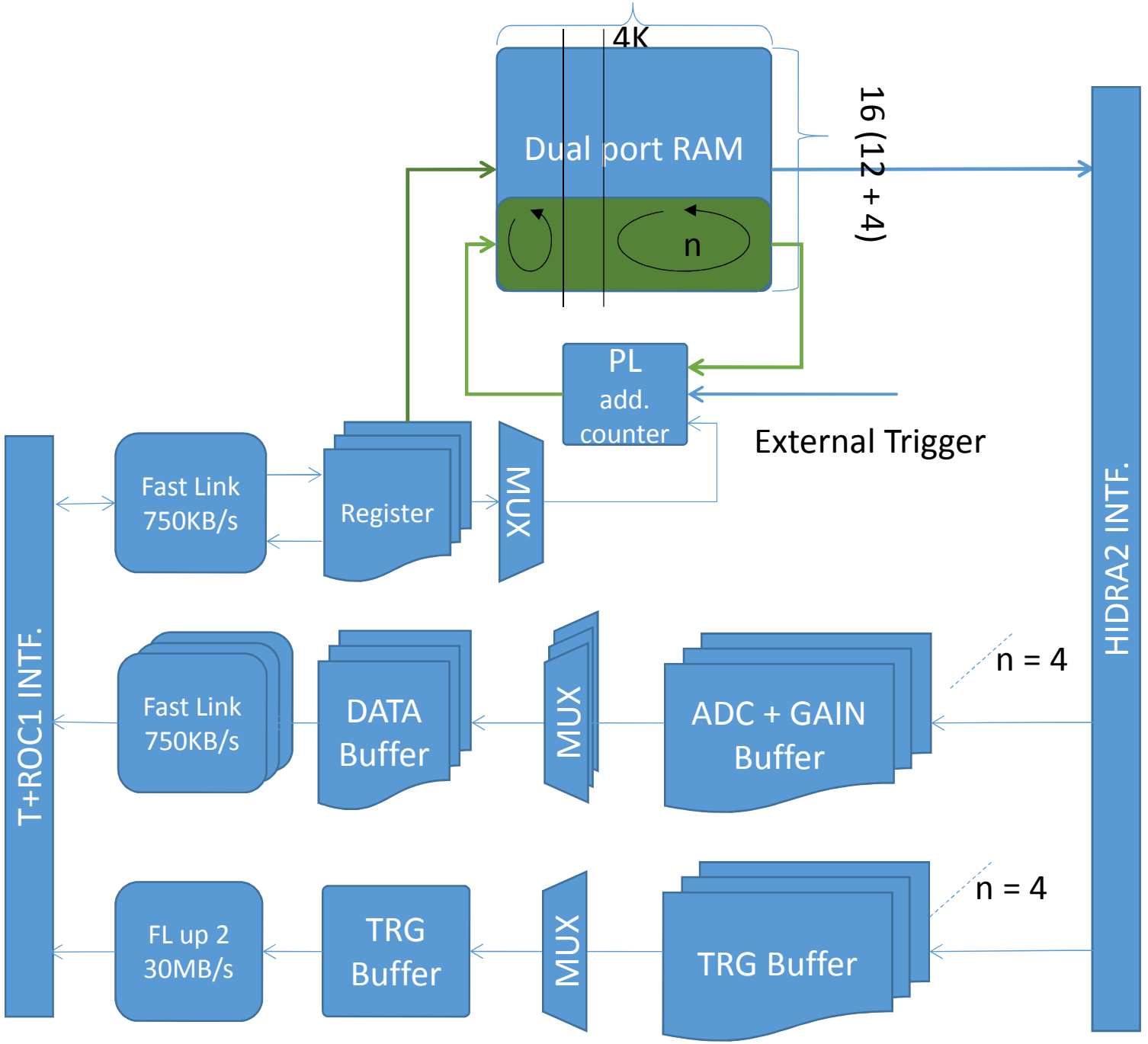
T+ROC2 main functions:

- HIDRA control sequence generation
- Communication protocol implementation
- Acquisition
- Buffering

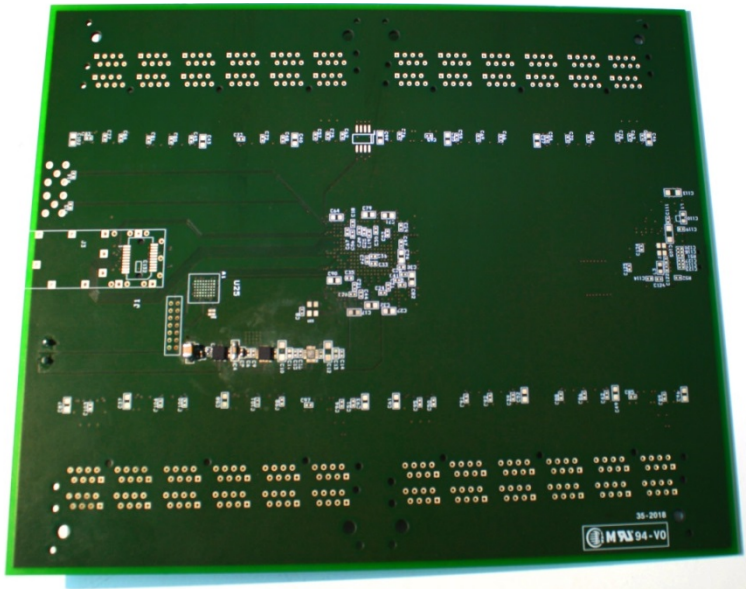


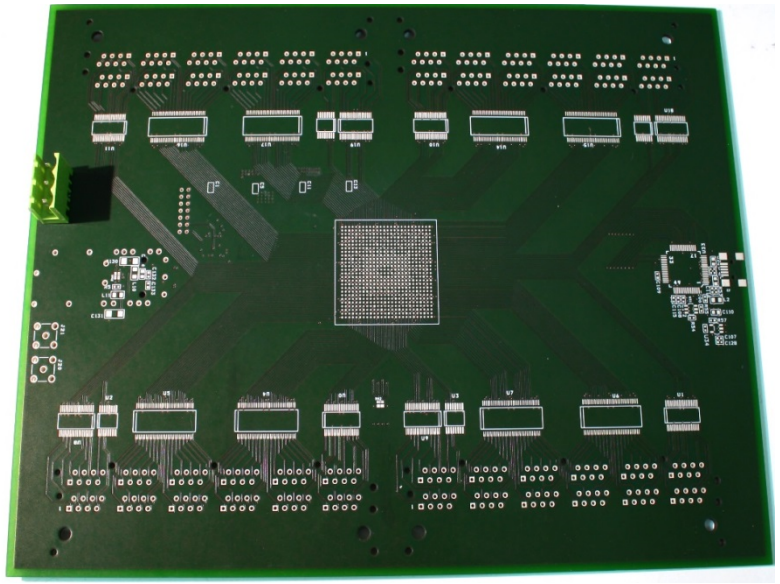


T+ROC2 CONTROL SEQUENCE GENERATION + DATA ADQUISITION



T+ROC1 description:

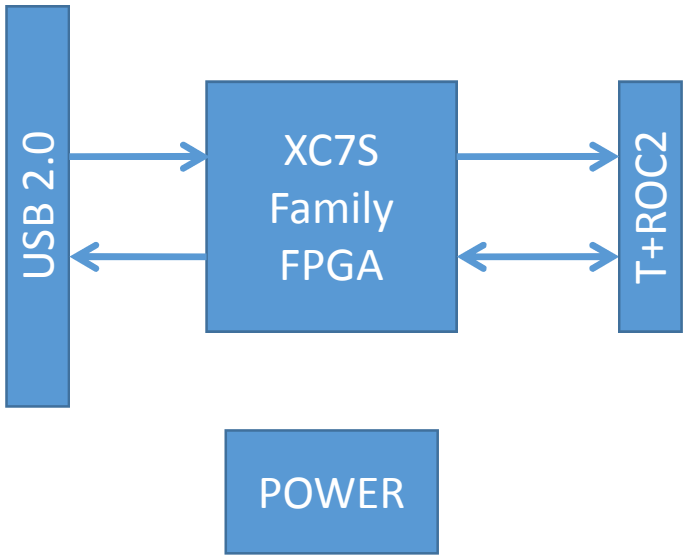




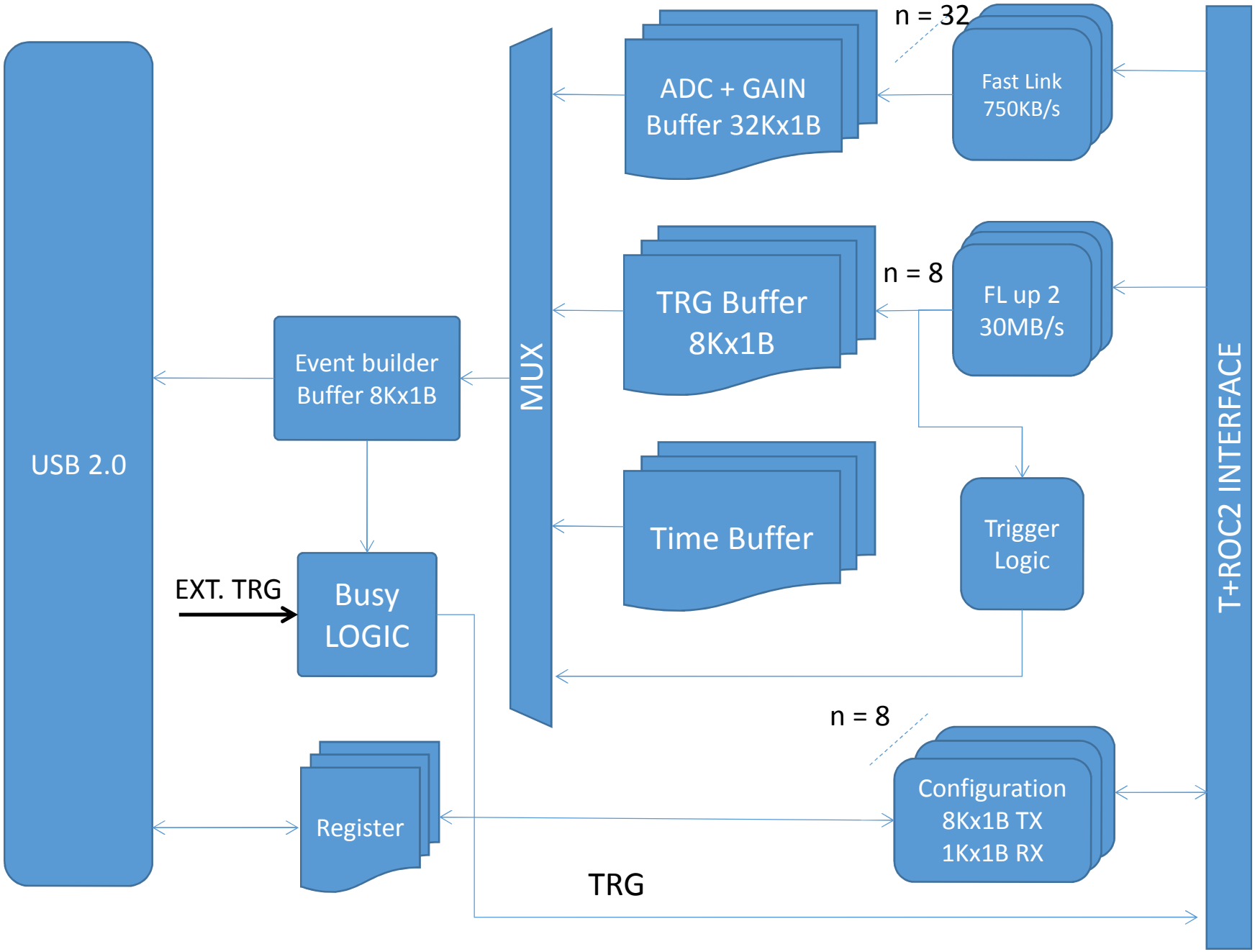
- 20cm x 17cm
- 6 Layers
- Firmware almost finished
- XC7S Xilinx FPGA
- USB 2.0 Interface

T+ROC1 main functions:

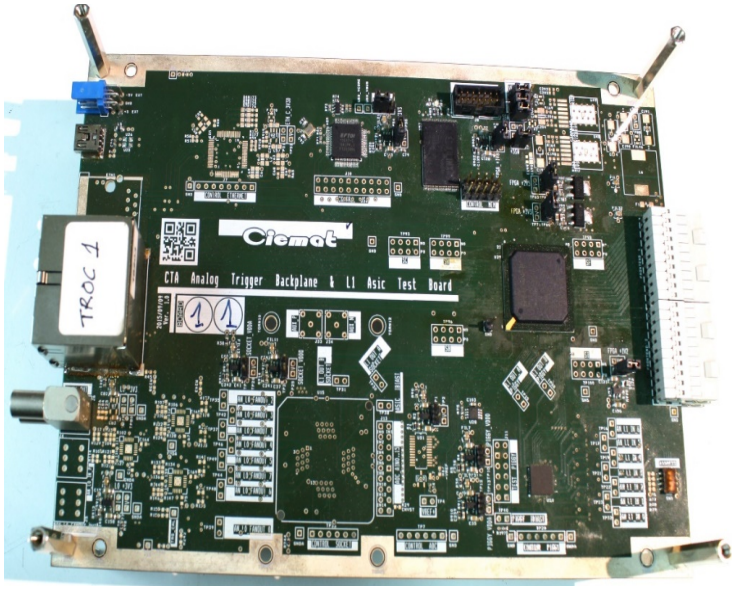
- Event builder
- Busy management
- Communication protocol
- Trigger logic
- Configuration
- Buffering

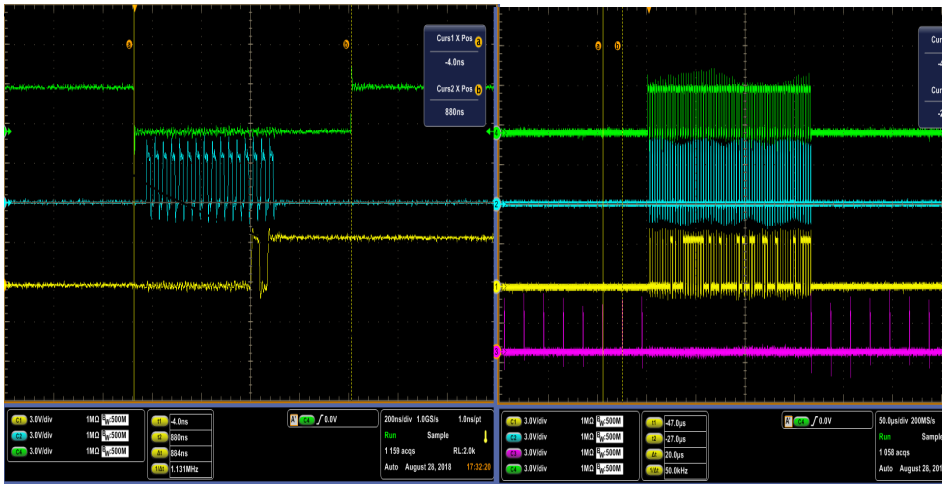


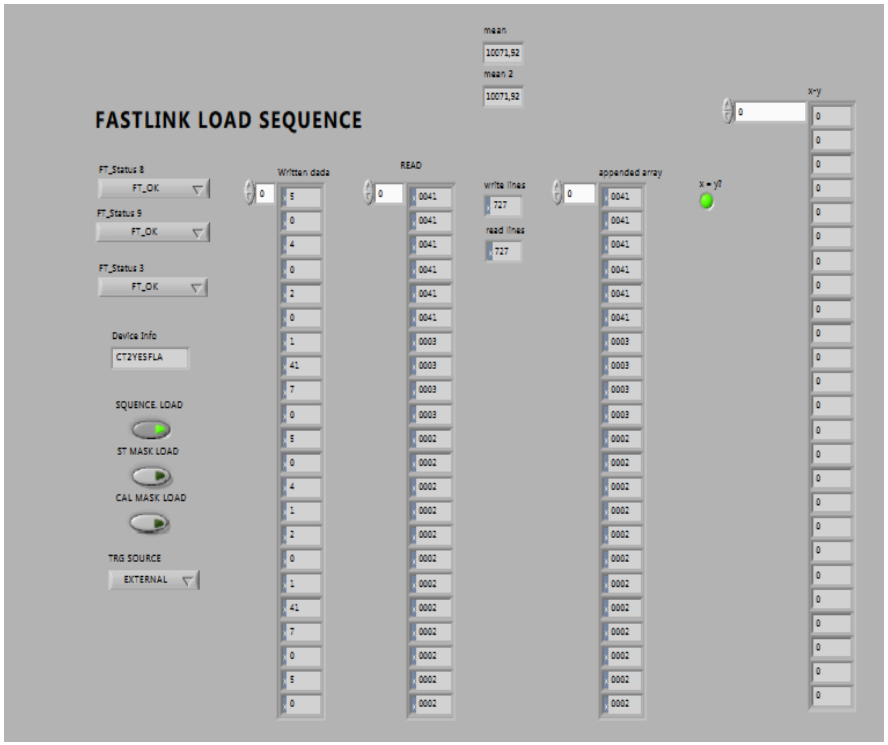
T+ROC1 EVENT GENERATION + CONFIGURATION

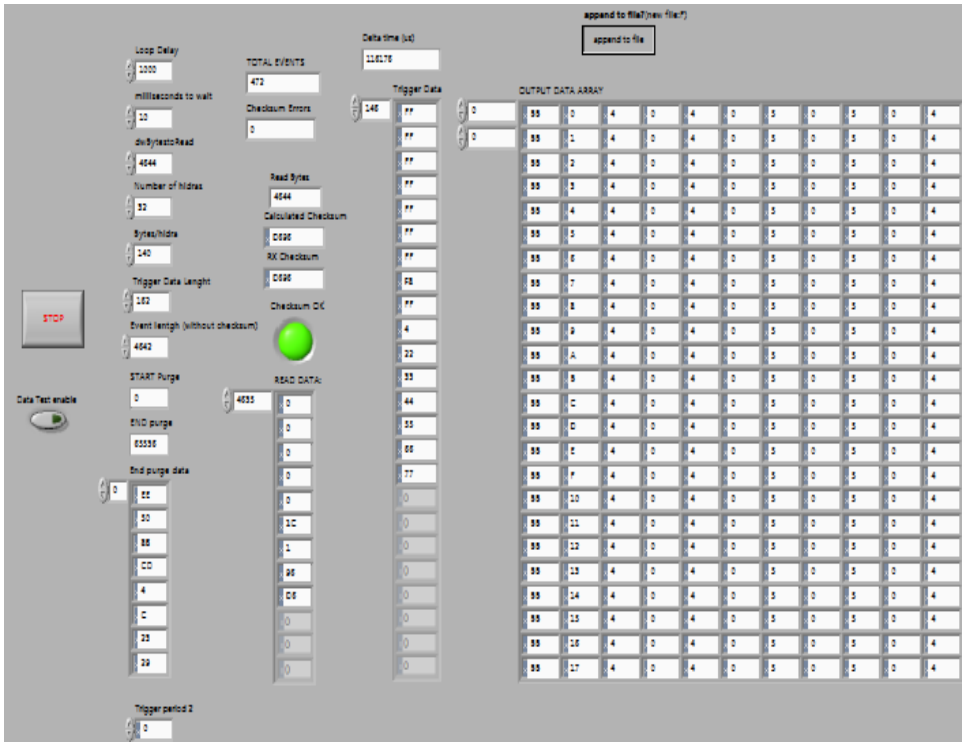


T+ROC1 & T+ROC2 tests









Workplan & Schedule

- Tests of new Kapton cables to be performed in Florence in November.
- HiDRA2 boards tested in Trieste in November and delivered to CIEMAT for tests with new T+ROCs in December.
- Standalone tests of T+ROC1 & T+ROC2 boards at CIEMAT in December.
- HiDRA2 & T+ROCs system to be tested at CIEMAT in January.
- Test of Calocube with the new electronics in Florence in February.
- Beam test at Frascati (BTF) will follow.