

# NEW CALOCUBE READ- OUT SYSTEM

J. Marín, G. Martínez, C. Cruz, J. Casaus

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# HiDRA2 Chip



## HiDRA2 DATASHEET

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Gianluigi Zampa

### HiDRA2: High Dynamic Range Amplifier frontend ASIC

#### Specifications

Number of channels: 16

Supply voltage: 3.3 V

Analog functions: automatic double-gain pulse reset Charge Sensitive Amplifier (CSA), calibration circuitry (registers and capacitors), Correlated double sampling, Self-triggering circuitry, and output multiplexer

Power consumption: 3.75 mW/ch (common circuitry included), typical corner

Dynamim range:

- High gain:  $\approx 2.7$  pC (560 MIP on 380  $\mu\text{m}$  Si sensors)
- Low gain:  $\approx 52.6$  pC (11000 MIP on 380  $\mu\text{m}$  Si sensors)

Linearity

- High gain:  $\pm 0.3$  %
- Low gain:  $\pm 0.6$  %

Calibration capacitance: 1.6 pF

Equivalent noise charge:  $2280 e^- + 7.5 e^-/\text{pF}$  RMS (CDS time constant of 10  $\mu\text{s}$ )

CSA minimum reset pulse duration:  $t_{\text{CSA\_reset}} = 150$  ns

CSA settling time (1 %):  $t_{\text{S\_CSA,1\%}} = 400$  ns @  $C_D = 300$  pF

CDS external pedestal reference: 900 mV

CDS reset duration:  $t_{\text{CDS\_reset}} = t_{\text{CSA\_reset}} + 400$  ns @  $C_D = 300$  pF

Self-trigger gain:  $\times 10$

Self-trigger threshold: set by an external resistor, 2 adjustment bits ( $\approx \times 1, \times 1.5, \times 2, \text{ and } \times 2.5$ )

Self-trigger comparator hysteresis:  $16$  mV  $\pm 2.3$  mV r.m.s.

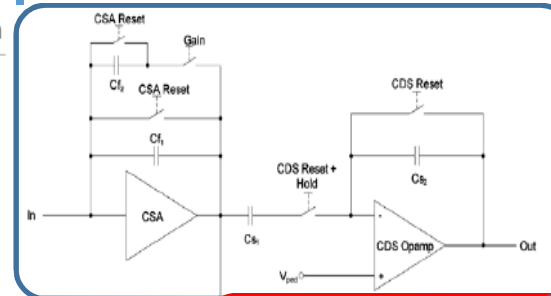
Self-trigger response time:  $\leq 500$  ns for signals 10 mV larger than the effective threshold (equal to the threshold voltage plus the comparator hysteresis)

Output buffer driving capability:  $20$  k $\Omega$  //  $100$  pF

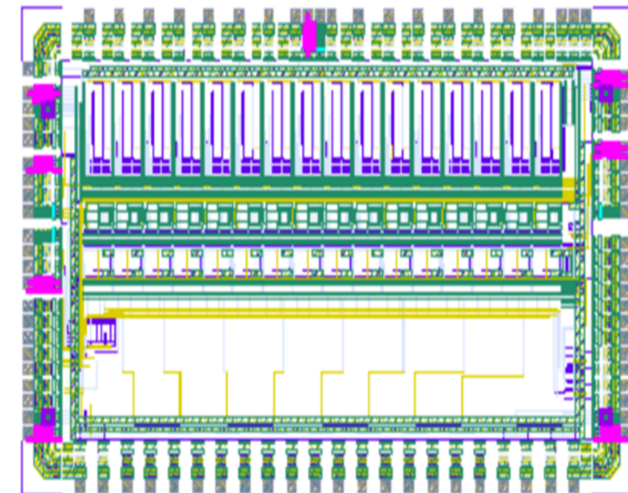
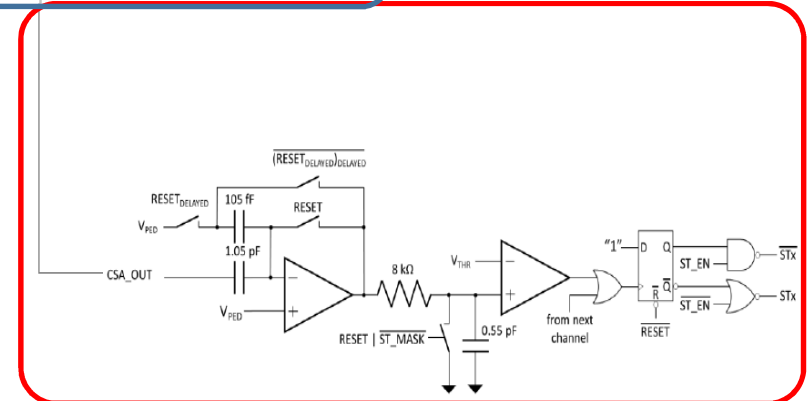
Output settling time (1 %):  $t_{\text{S\_OUT,1\%}} = 80$  ns @  $C_L = 100$  pF

Package: CQFP100 (CQZ10001)

### Current System Architecture

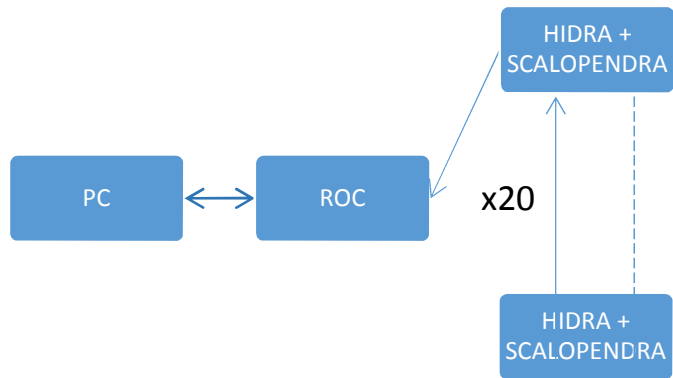


### New Self Trigger Stage

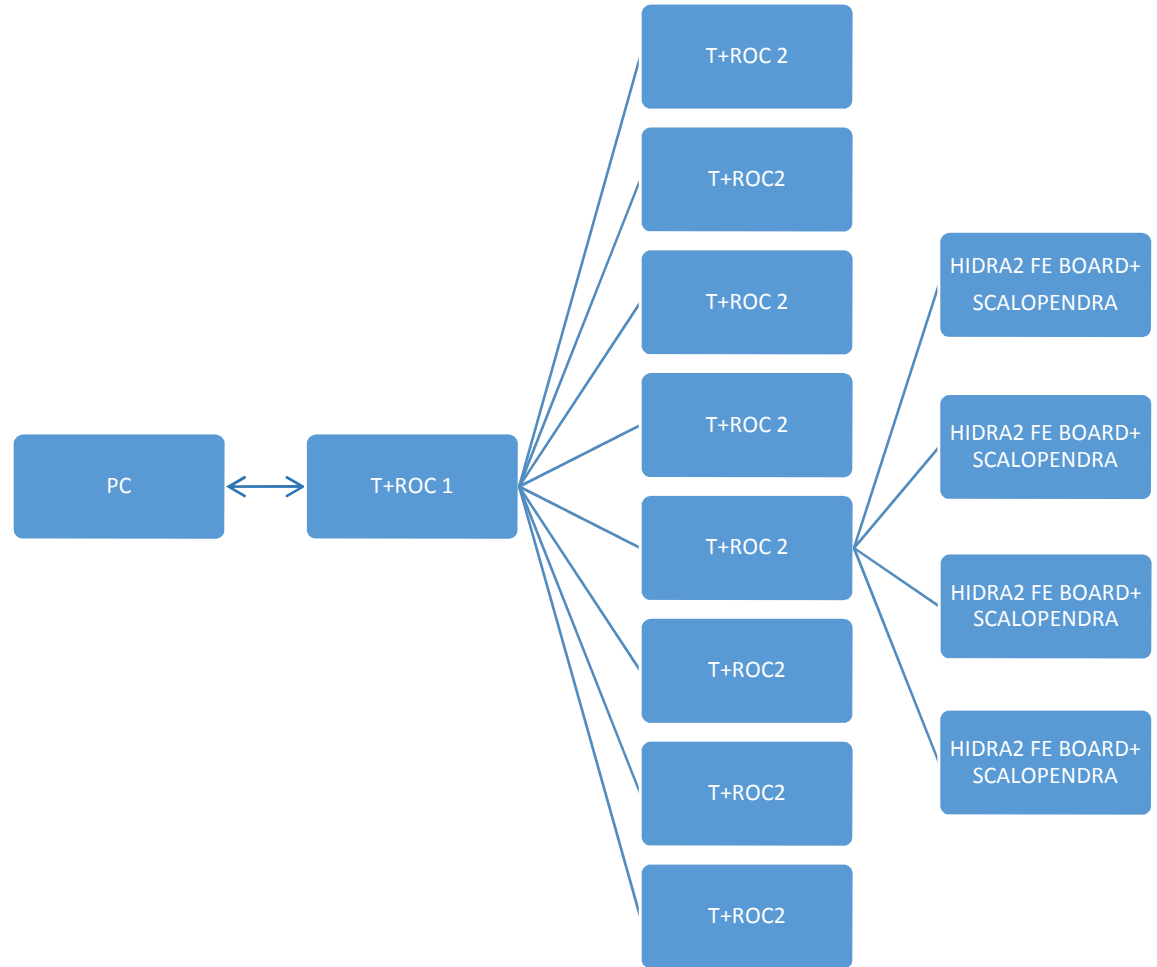


# Calocube read-out diagram

## Current System Architecture



## New System Architecture



COMMAND DISTRIBUTION & CONFIGURATION & TRIGGER IN



DATA COLLECTION & TRIGGER OUT

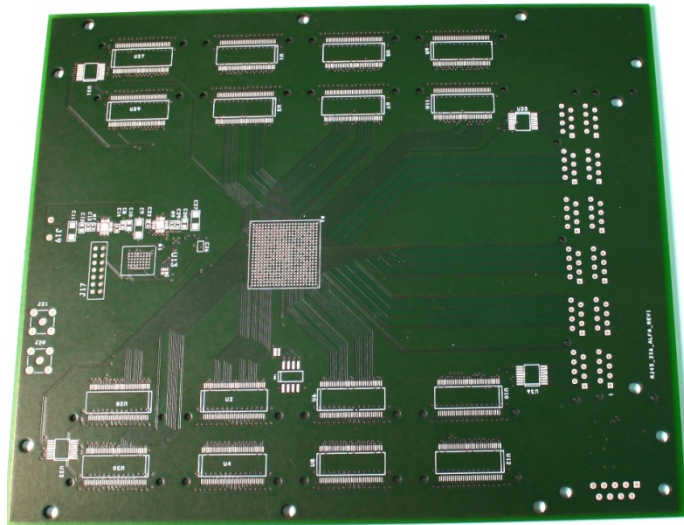


# Read-out summary

## System Characteristic:

- 1 T+ROC1.
- Up to 8 T+ROC2 max.
- Up to 4 Hidra2 FEB/T+ROC2 max.
- 4 Hidra2 ASIC/Hidra2 FEB
- 16 data channels/Hidra2 ASIC
- 8 Trigger channels/Hidra2 ASIC
- 3 Scalopendra Kapton cables / Hidra2 FEB
- LVDS interface between boards.
- Common acquisition sequence to all 4 Hidra2 FEB.
- Single digital read-out (ADC) output per Hidra2 FEB.
- Trigger & calibration masks Daisy-Chained inside each Hidra2 FEB.

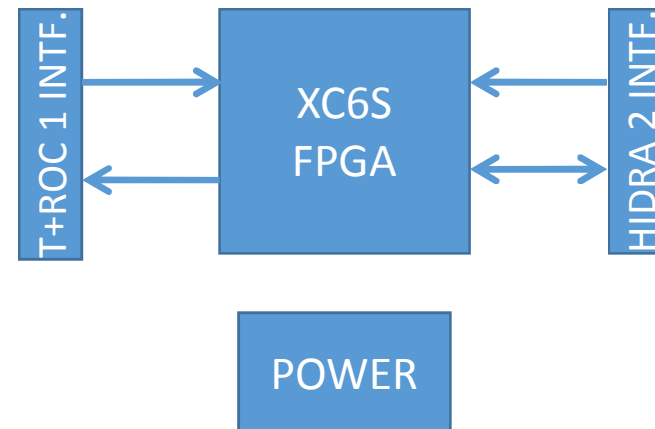
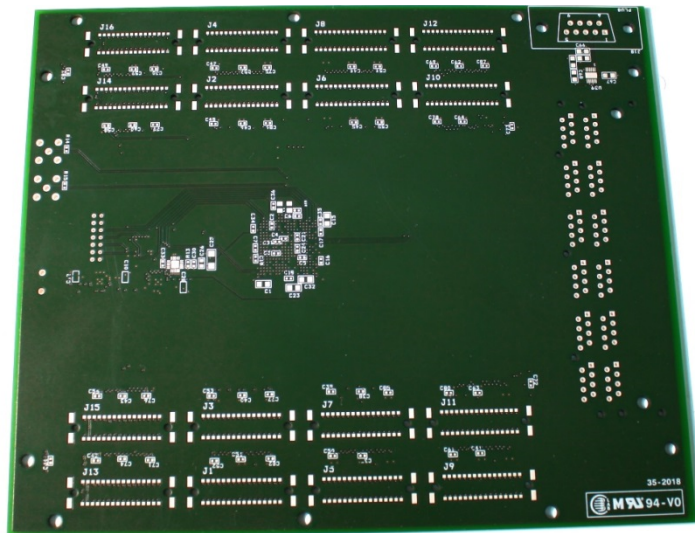
## T+ROC2 Description



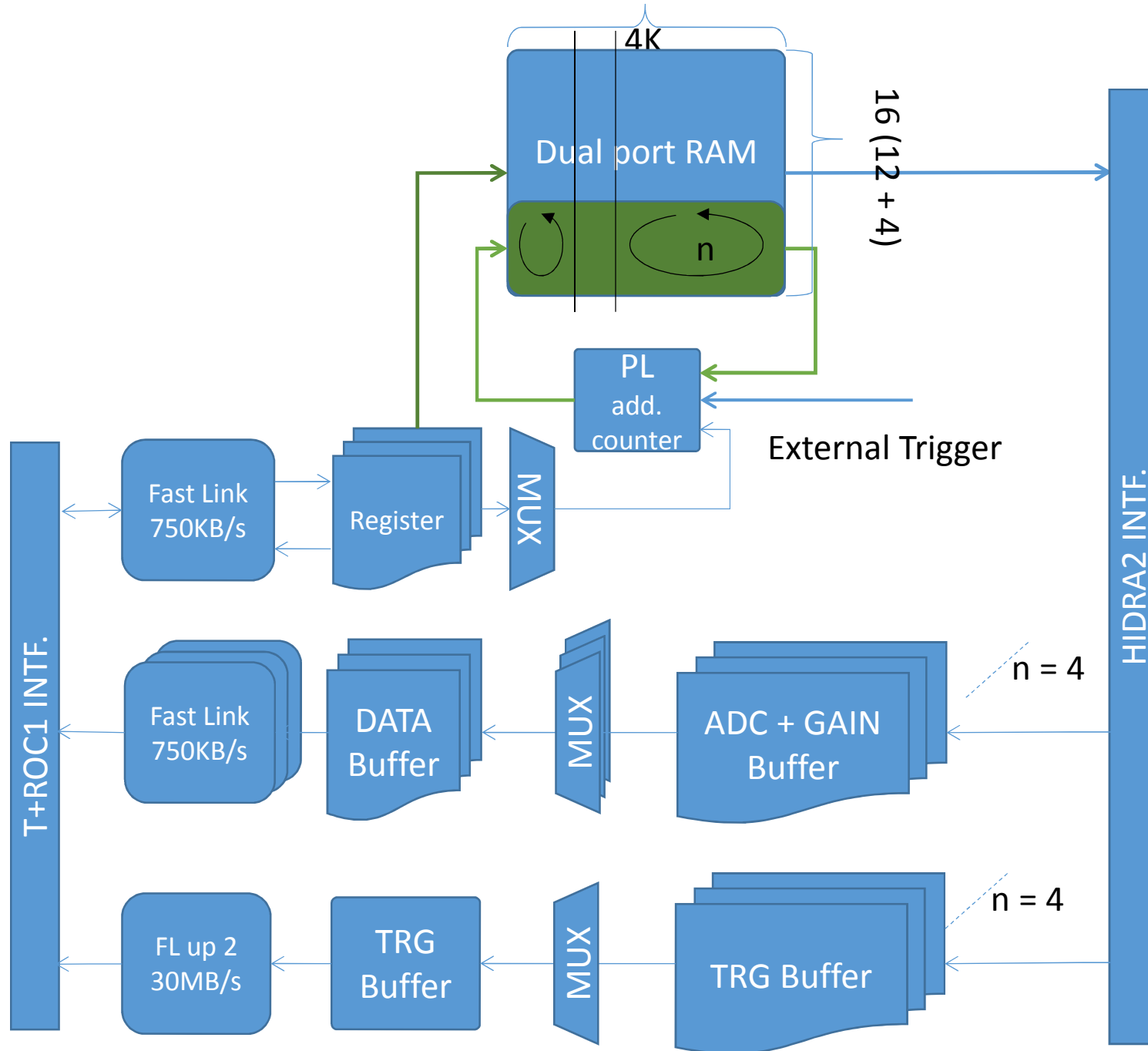
- 15cm x 17cm.
- 6 Layers.
- PCB layout cross-checked with Hidra2 FEB design.
- Firmware developed in a test-board and almost finished.
- XC6S45 Xilinx FPGA.
- Fast Serial link connection to T+ROC 1.
- LVDS connections to HIDRA2 & T+ROC1.

## T+ROC2 main functions:

- HIDRA control sequence generation
- Communication protocol implementation
- Acquisition
- Buffering



# T+ROC2 CONTROL SEQUENCE GENERATION + DATA ACQUISITION

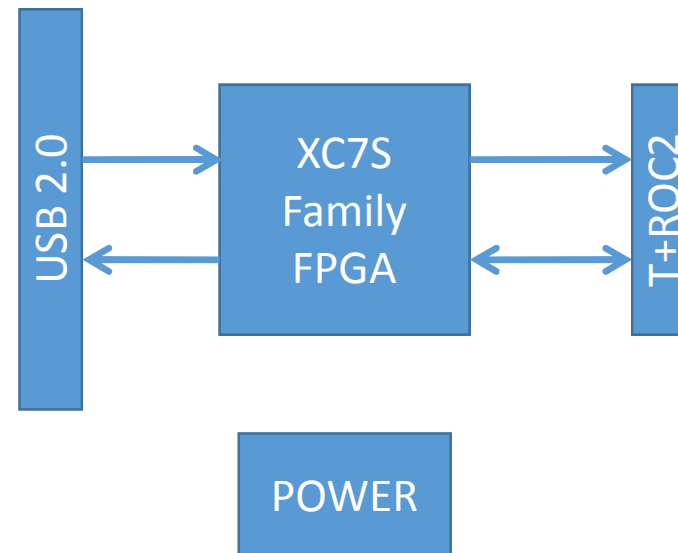
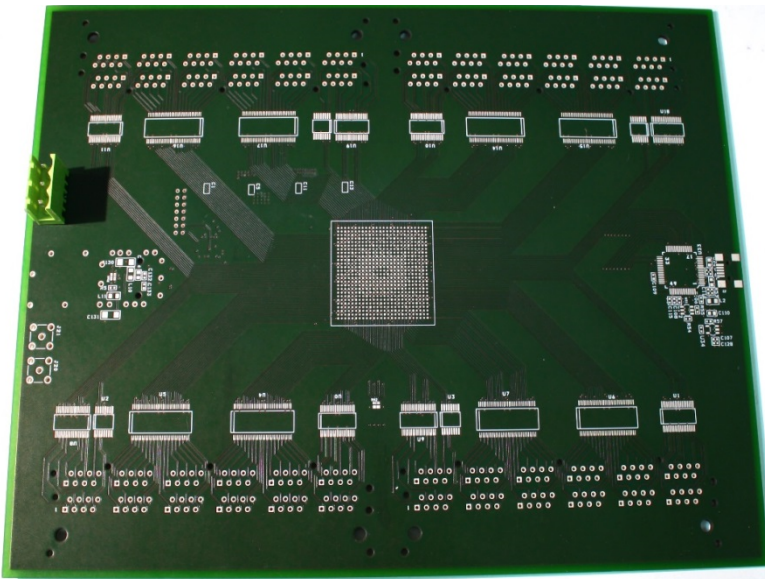
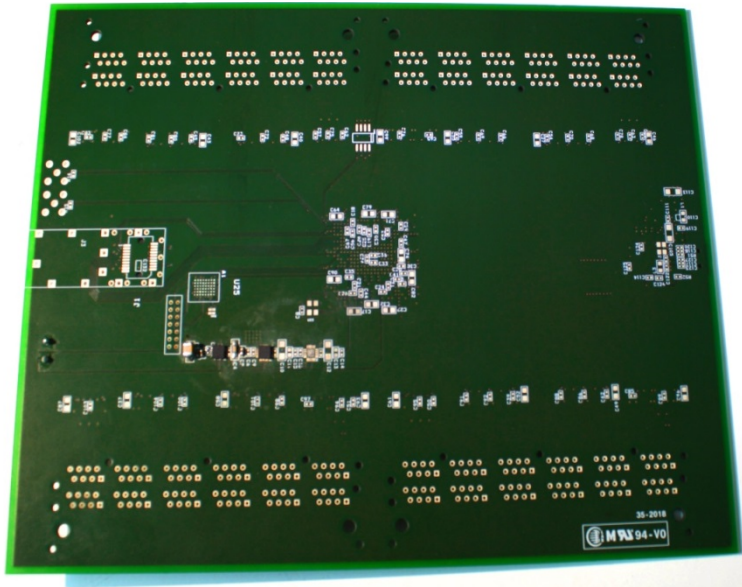


## T+ROC1 description:

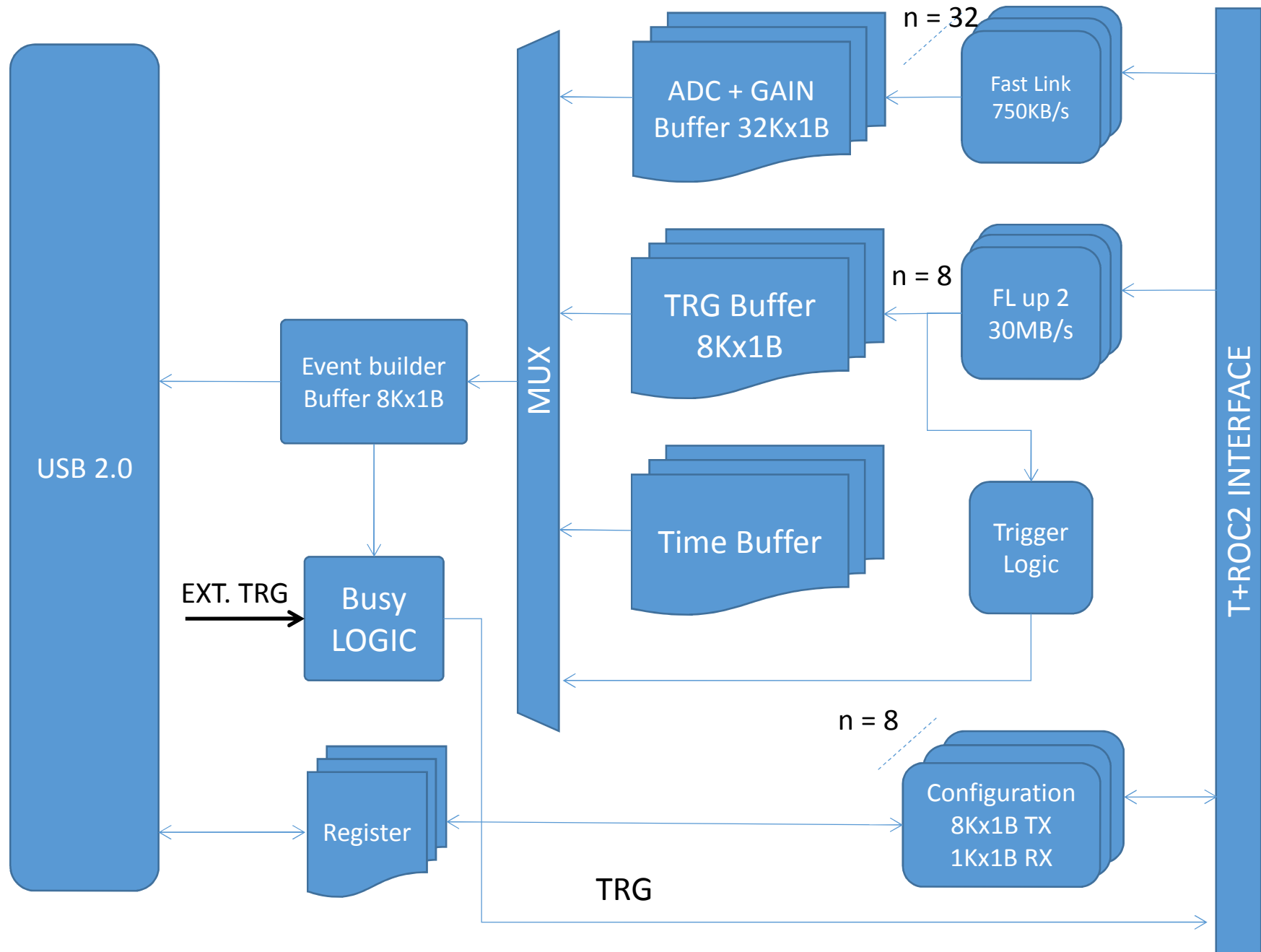
- 20cm x 17cm
- 6 Layers
- Firmware almost finished
- XC7S Xilinx FPGA
- USB 2.0 Interface

## T+ROC1 main functions:

- Event builder
- Busy management
- Communication protocol
- Trigger logic
- Configuration
- Buffering

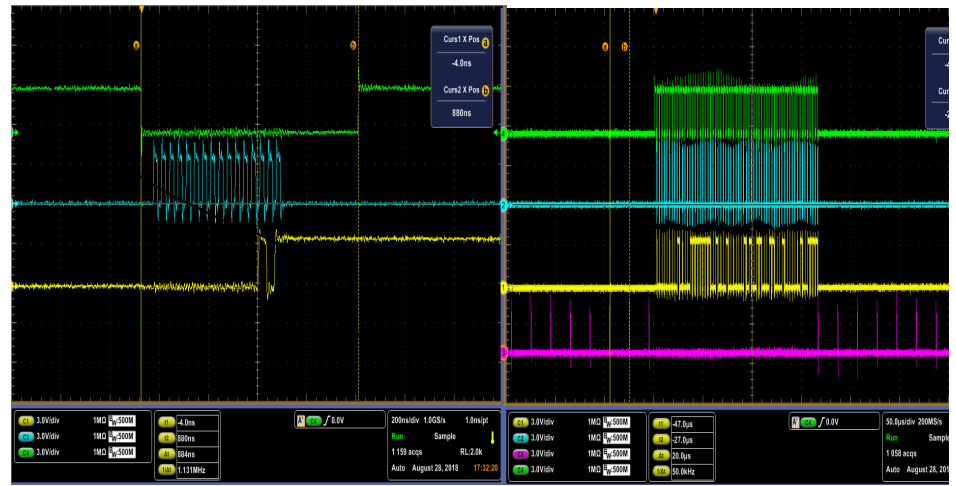
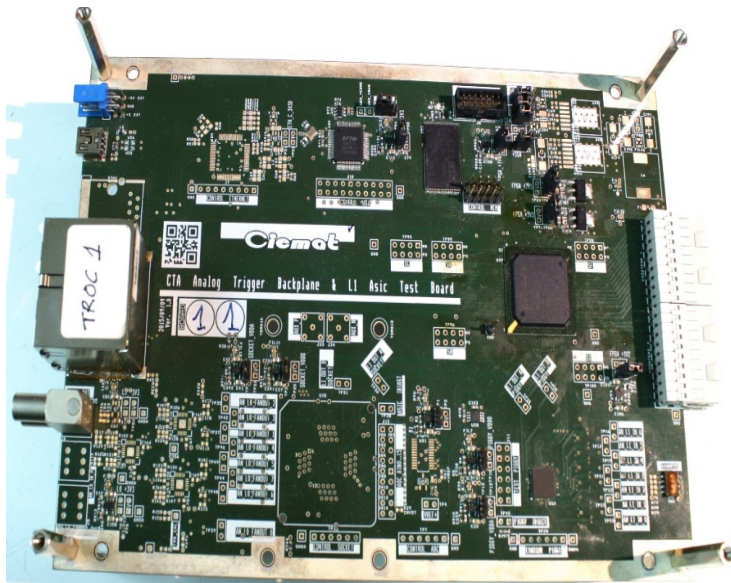


# T+ROC1 EVENT GENERATION + CONFIGURATION





# T+ROC1 & T+ROC2 tests



### FASTLINK LOAD SEQUENCE

mean: 10071.92  
mean 2: 10071.92

FT\_Status 8: FT\_OK  
FT\_Status 9: FT\_OK  
FT\_Status 3: FT\_OK

Device Info: CT2VESFLA

SEQUENCE LOAD:   
ST MASK LOAD:   
CAL MASK LOAD:   
TRIG SOURCE: EXTERNAL

Written data	READ	write lines	read lines	appended array	x-y
0	0	727	727	0	0
5	0041	0041	0041	0	0
0	0041	0041	0041	0	0
4	0041	0041	0041	0	0
0	0041	0041	0041	0	0
2	0041	0041	0041	0	0
0	0041	0041	0041	0	0
1	0009	0009	0009	0	0
41	0009	0009	0009	0	0
7	0009	0009	0009	0	0
0	0009	0009	0009	0	0
5	0002	0002	0002	0	0
0	0002	0002	0002	0	0
4	0002	0002	0002	0	0
1	0002	0002	0002	0	0
2	0002	0002	0002	0	0
0	0002	0002	0002	0	0
1	0002	0002	0002	0	0
41	0002	0002	0002	0	0
7	0002	0002	0002	0	0
0	0002	0002	0002	0	0
5	0002	0002	0002	0	0
0	0002	0002	0002	0	0

append to file? (new file?)  
 append to file

Loop Delay: 1000  
milliseconds to wait: 10  
DivByZeroRead: 4544  
Number of Hiras: 32  
Bytes/Hiras: 140  
Trigger Data Length: 132  
Event length (without checksum): 4542  
START Purge: 0  
SVD purge: 65536  
End purge data: 0

Delta time (μs): 116176  
TOTAL E/EVENTS: 472  
Checksum Errors: 140  
Read Bytes: 4544  
Calculated Checksum: 6556  
RX Checksum: 6556  
Checksum OK:

Trigger Data: 140  
Checksum OK:

OUTPUT DATA ARRAY

Row	Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	Col 12	Col 13	Col 14	Col 15	Col 16	Col 17	Col 18	Col 19	Col 20
00	0	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
01	1	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
02	2	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
03	3	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
04	4	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
05	5	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
06	6	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
07	7	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
08	8	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
09	9	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
10	A	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
11	B	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
12	C	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
13	D	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
14	E	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
15	F	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
16	10	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
17	11	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
18	12	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
19	13	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
20	14	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
21	15	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
22	16	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4
23	17	4	0	4	0	5	0	5	0	4	0	4	0	4	0	4	0	4	0	4

# Workplan & Schedule

- Tests of new Kapton cables to be performed in Florence in November.
- HiDRA2 boards tested in Trieste in November and delivered to CIEMAT for tests with new T+ROCs in December.
- Standalone tests of T+ROC1 & T+ROC2 boards at CIEMAT in December.
- HiDRA2 & T+ROCs system to be tested at CIEMAT in January.
- Test of Calocube with the new electronics in Florence in February.
- Beam test at Frascati (BTF) will follow.

