# HERD Si STK design: open issue

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HERD workshop – CERN, November 2018

# STK tasks:

- Tracking: spatial resolution of 50 um
- Charge ID: dE/dx range up to Z=?
  - is Z=14 enough? do we need/want Z=26?

- ‘complete’ acceptance coverage

# Silicon TracKer for HERD

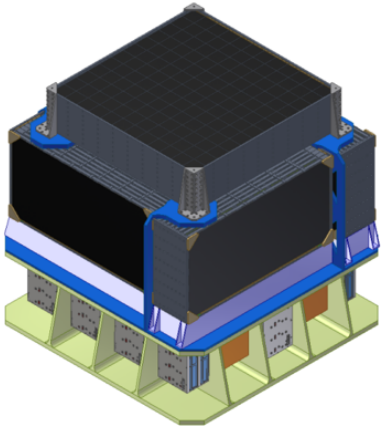
## STK Layout and configuration

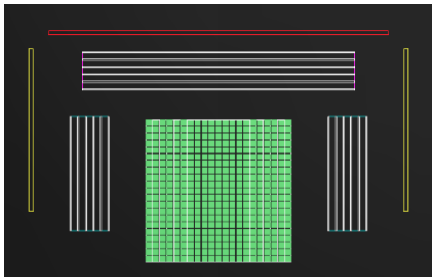
- **Top_STK**

**6 Layers of X&Y SSDs with LYSO**

**133cm*133cm (active area)**

**28 ladders on each X or Y plane and each ladder has 7 SSDs**





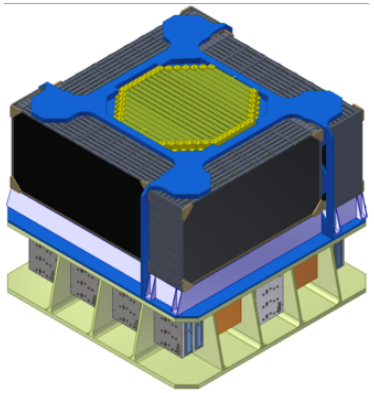
- **4*Lateral_STK**

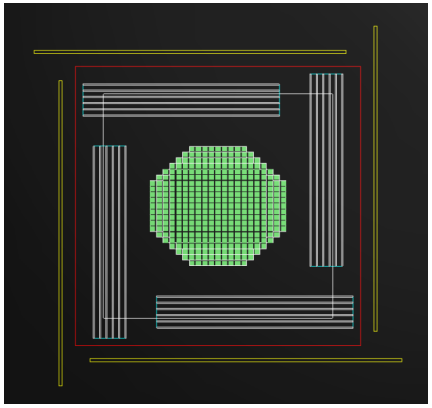
**3 Layers of X&Z or Y&Z SSD**

**95cm*66.5cm (active area)**

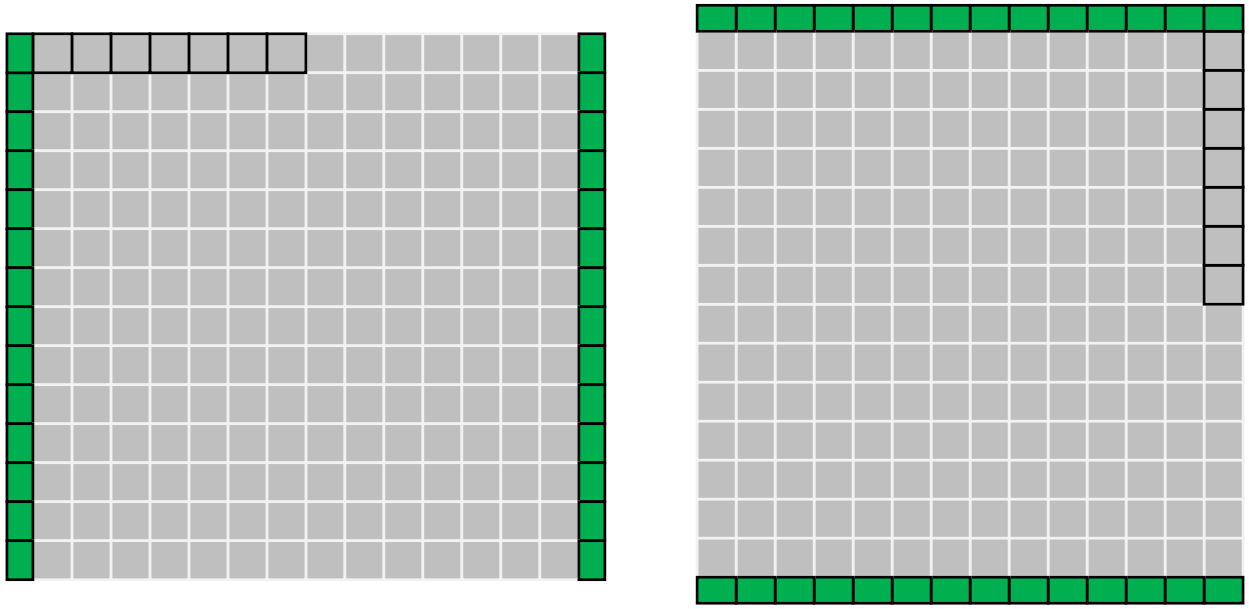
***10 ladders on X or Y plane and each ladder has 7 SSDs**

***14 ladders on Z plane and each ladder has 5 SSDs**



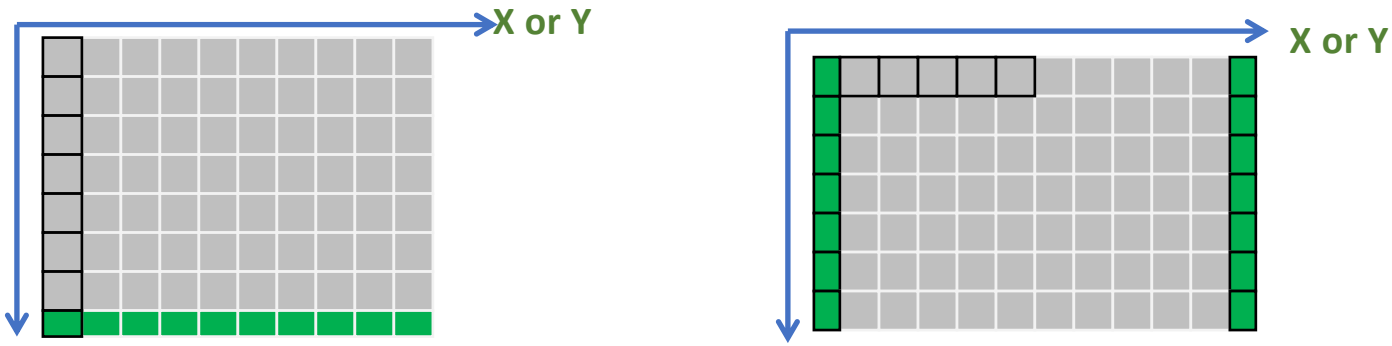


# Top STK



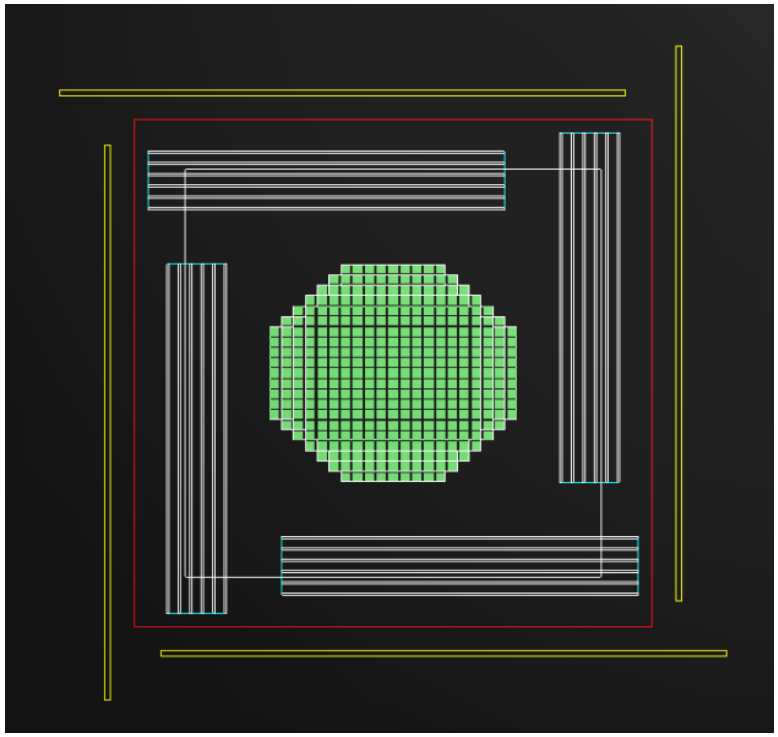
- Top STK: 6 layers, 1 layer has 2 planes, 1 plane has 28 ladders, 1 ladder has 7 wafers:
  - Total of 336 ladders, 2352 SSD, 2016 front end chips

# Side STK




- Side STK: 3 layers, 1 layer has 2 planes, 1 plane has 10+14 ladders, 1 ladder has 7 or 5 wafers:
  - Total of 120+168 ladders, 1680 SSD, 1728 front end chips

# octagonal shape for the side STK



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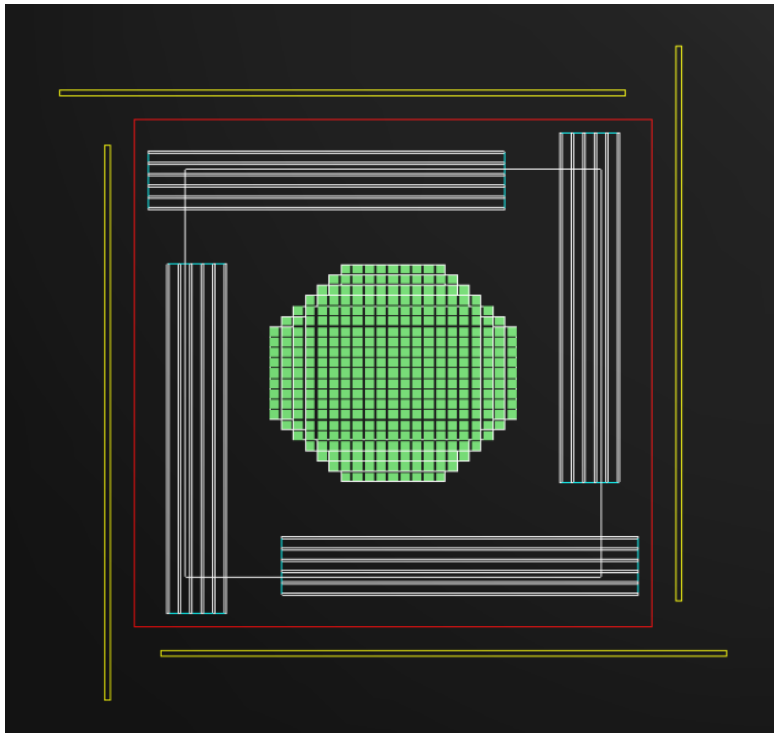
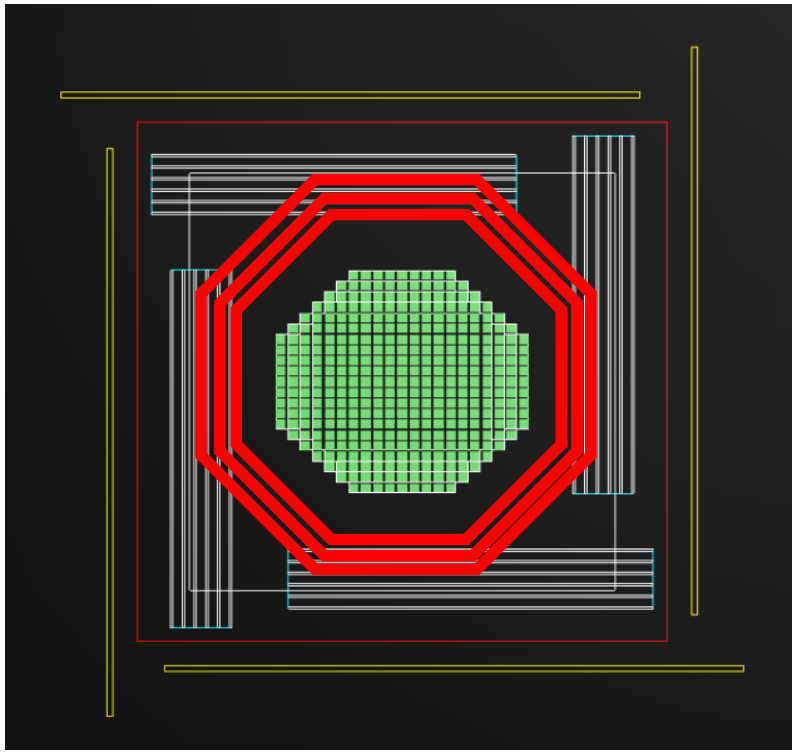
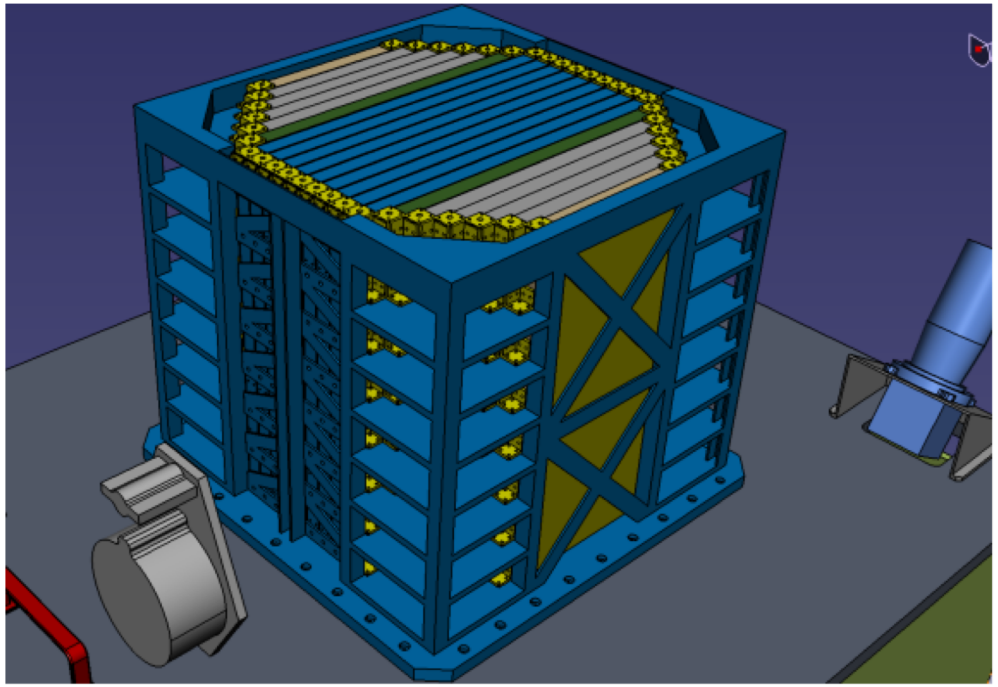
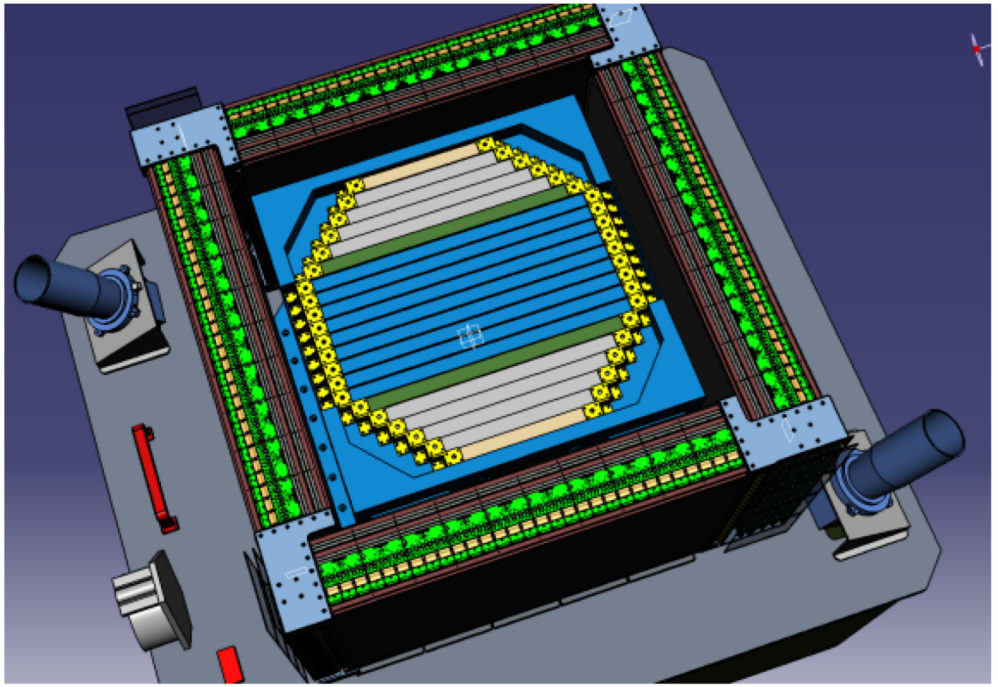




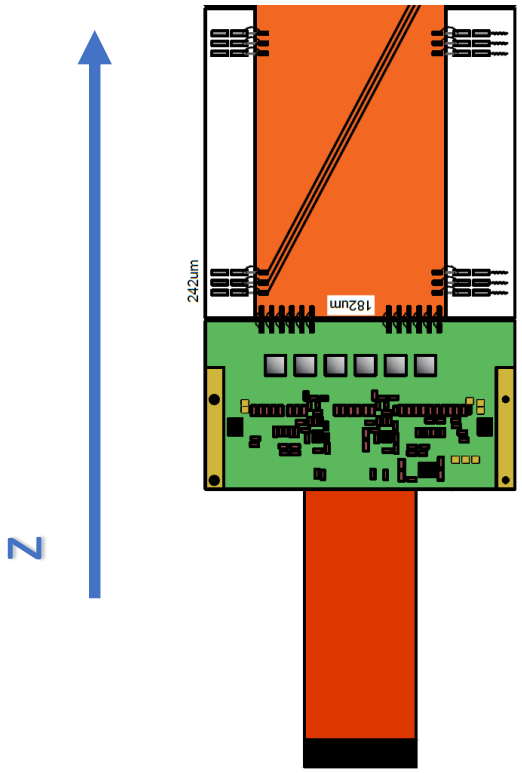
# cut the corner …

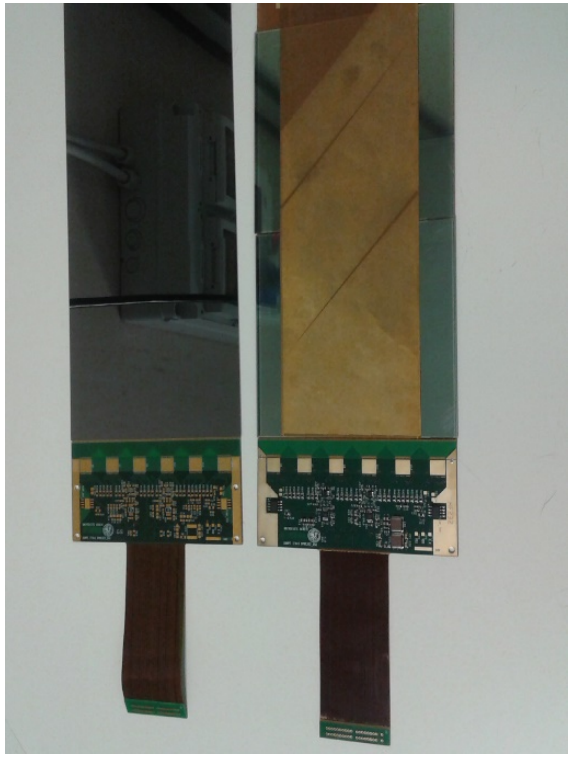


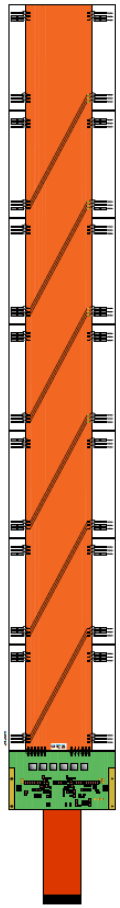


- benefits: better acceptance coverage
  possibility to have only one ladder type, 7*

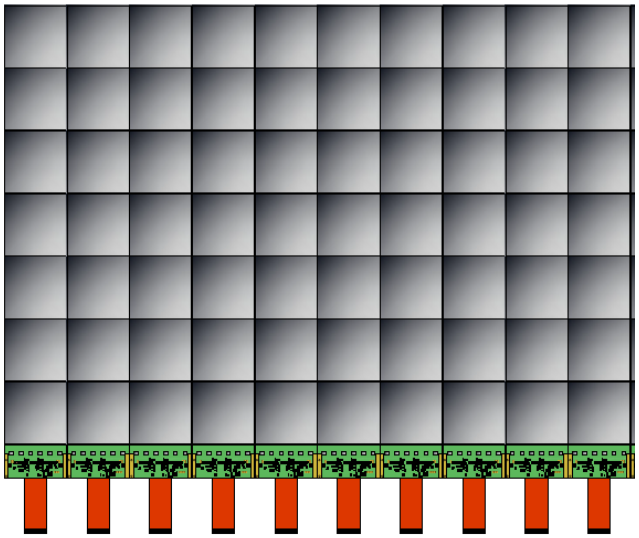
# signal re-routing for Z coordinate readout

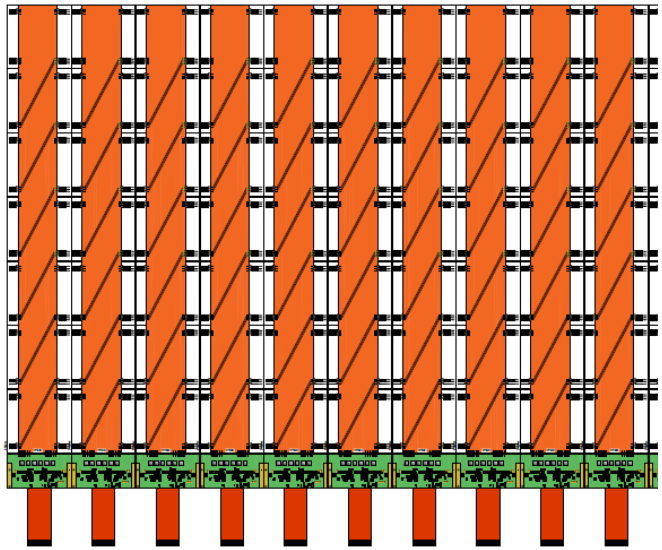




# Side STK





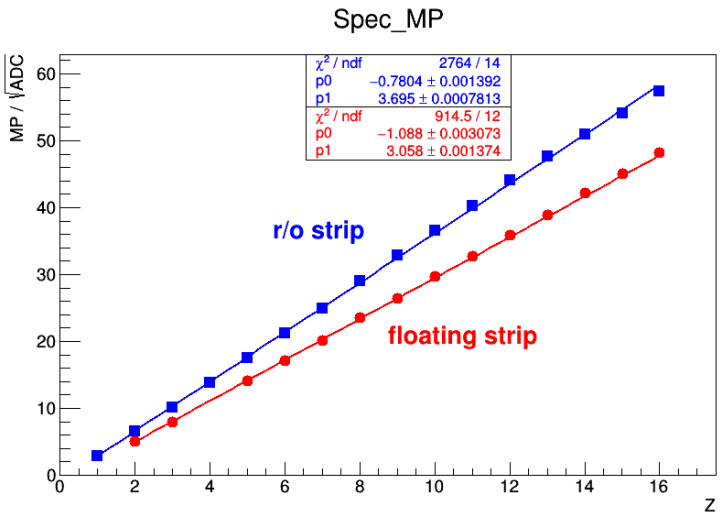
- Side STK: 3 layers, 1 layer has 2 planes, 1 plane has 32 – 34 – 38 ladders, 1 ladder has 7 wafers
  - total of 206 ladders, 1442 SSD, 1236 front end chips

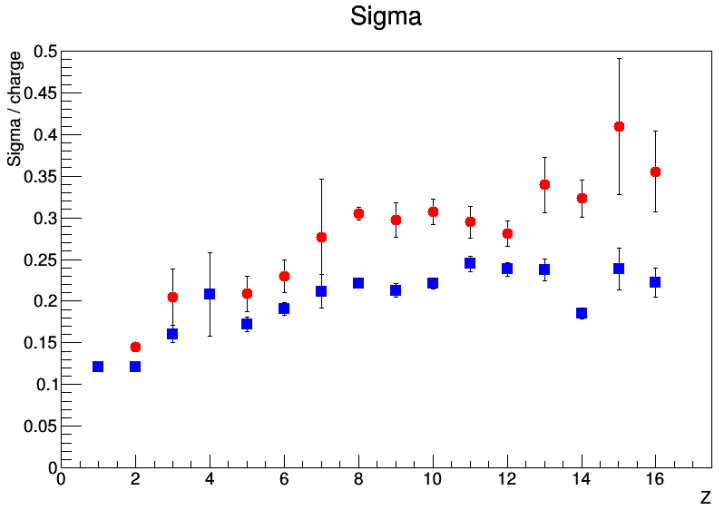
# some numbers

| | DAMPE | HERD | AMS-02 |
|---|---|---|---|
| SSD | 768 | 3794 | 2284 |
| ladders | 192 | 542 | 192 |
| Front end chips | 1152 (22 W) | 3252 (62 W) | 3072 (190 W) |
| | | 4336 (83 W) | |
| | | 5420 (104 W) | |

# DAMPE SSD with high dynamic range chip

Gong Ke, HERD VI workshop



# to be done:

- define the detailed SSD geometry (~ 95x95 mm2)
  - to match the overal layer/plane geometry
  - to optimise the strip/readout pitch and strip geometry
  - to possibly use only one type of ladders for both TOP and SIDE STK
  - to match the TIC needs
- identify the front end chip
  - industrial chip (VA1140 or similar from IDEas)
  - in house development (based on TIGER chip, INFN/IHEP development)
  - self trigger would be a great advantage

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  - self trigger would be a great advantage
- find enough money!