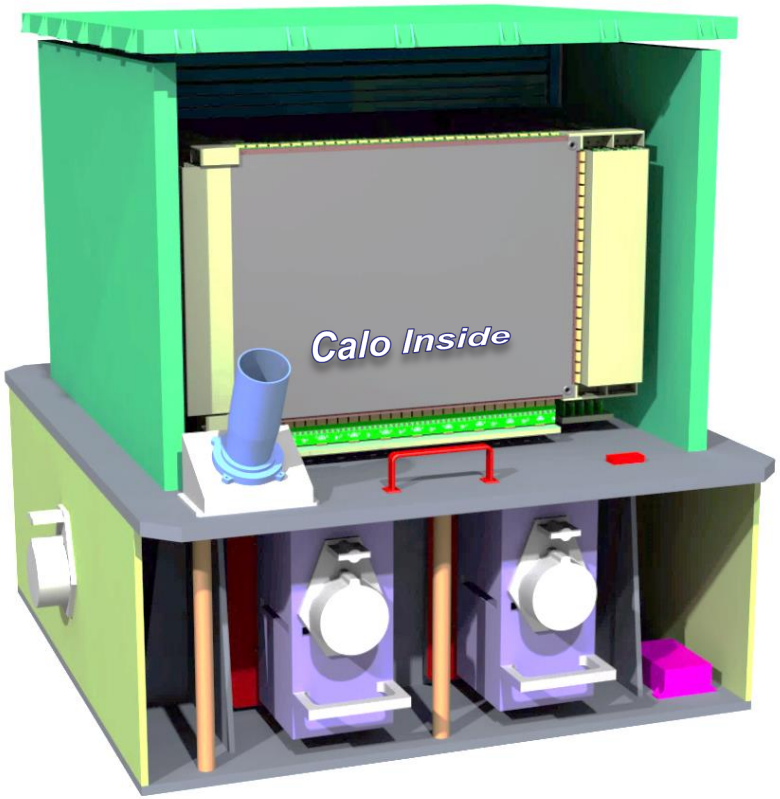
UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

# HERD Collaboration meeting

## *Fiber Tracker (FIT)*
## *Mechanics and Electronics Designs*




Philipp Azzarello, Franck Cadoux, Yannick Favre, Daniel La Marra, Chiara Perrina, Junjing Wang, Xin Wu

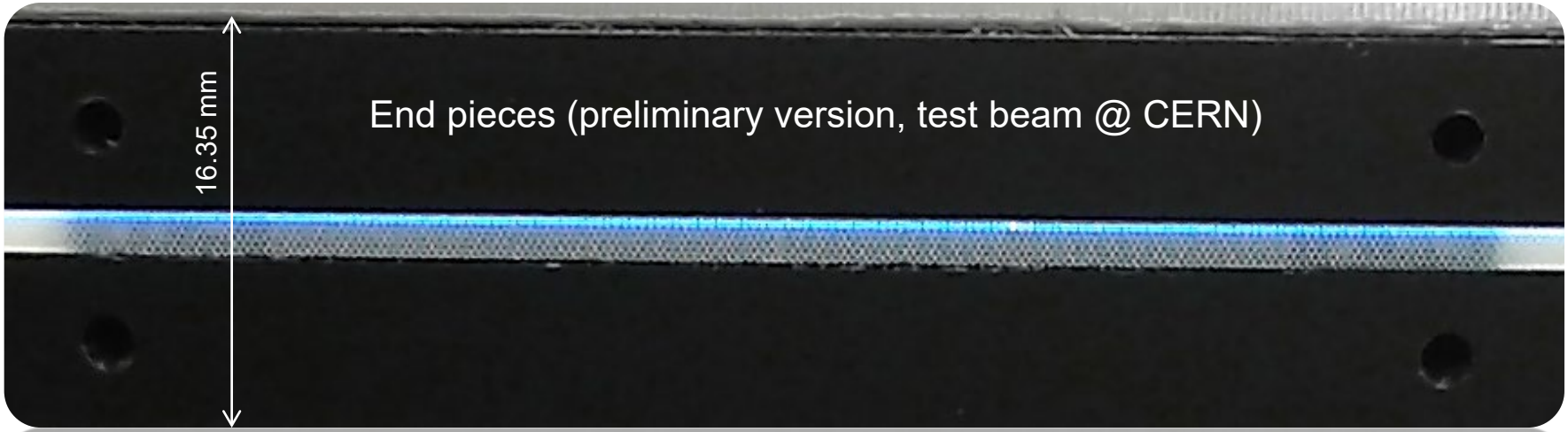
# Mechanics designs

- FIT Design overview (6 TRAYS design)
- Latest version of FEB
- FEA on TRAY assembly
- FIT weight status

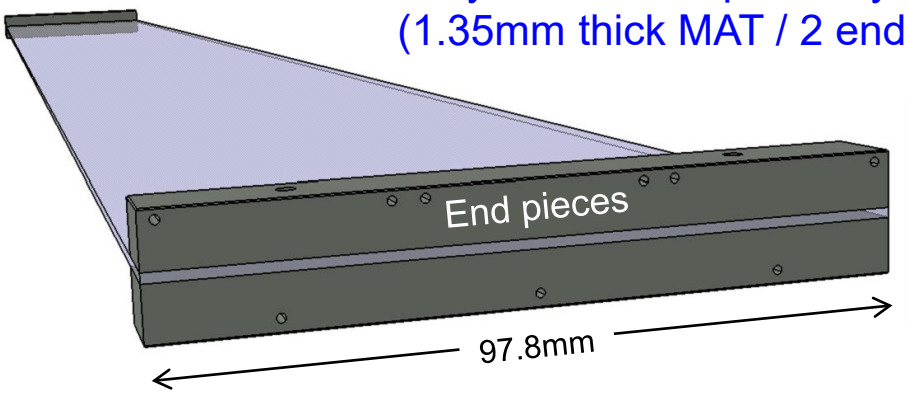
Franck Cadoux

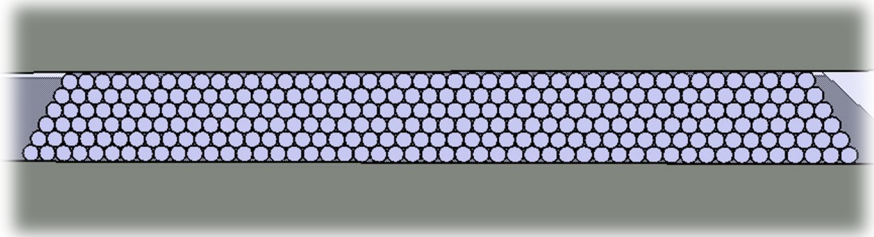
# FIT Design overview

**The Fiber MAT** (stacking of 6 layers of 0.25mm diameter fibers)

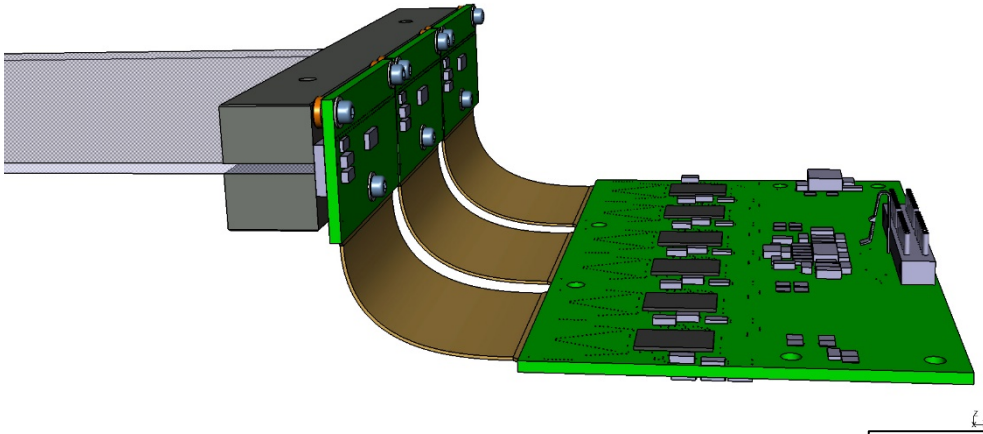


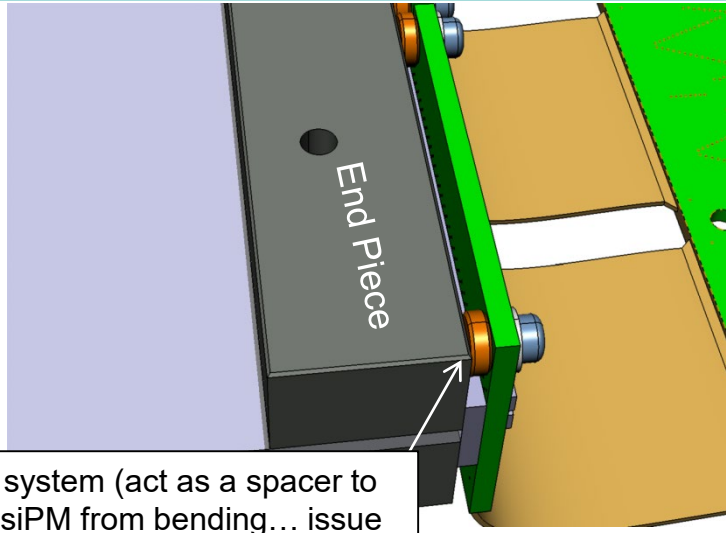

6 layers of fibers precisely lined up & glued via a tooling at EPFL
(1.35mm thick MAT / 2 end pieces for SiPM read out)



# FIT Design overview

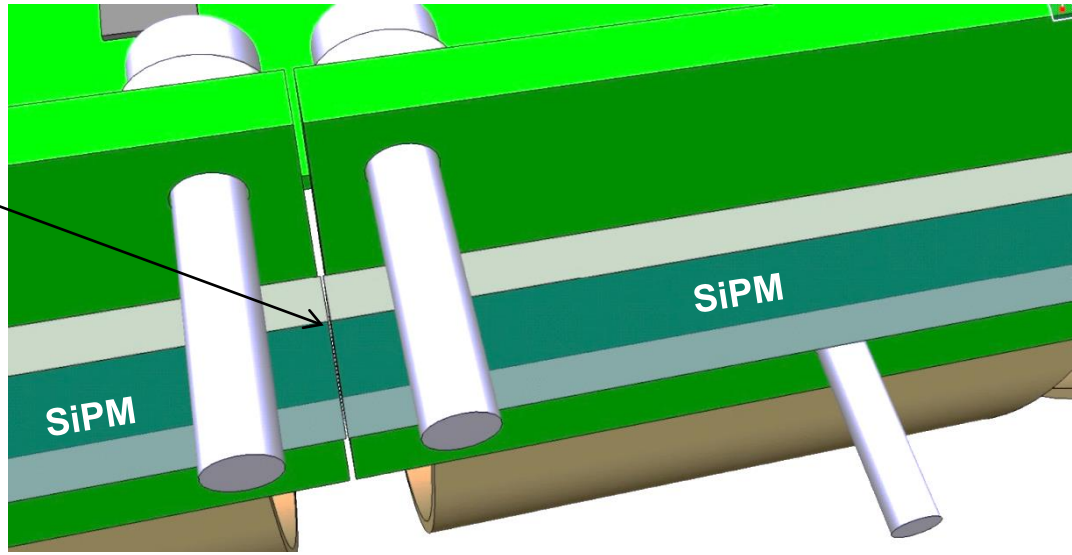





Self locking system (act as a spacer to prevent the siPM from bending… issue seen at last Test beam!)

Clearance between SiPM ( < 50 microns)

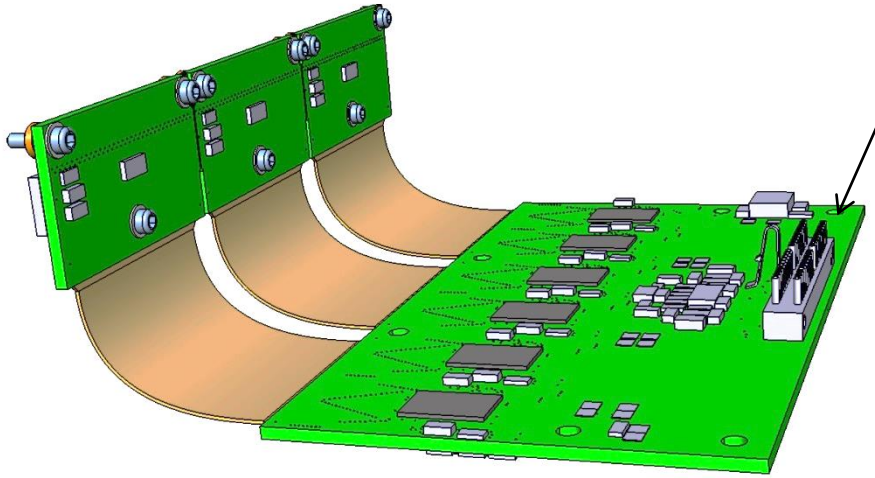
**Highly precise SiPM assembly on PCB**

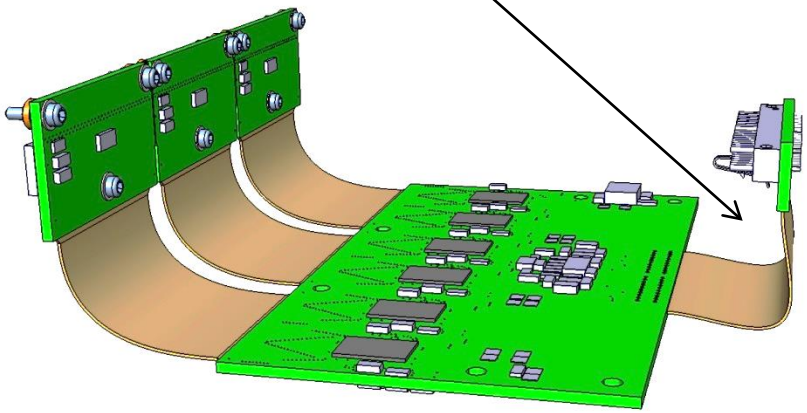


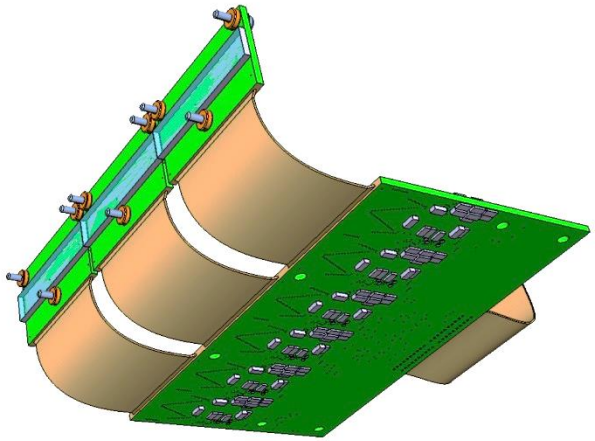
# FIT Design overview

## FEB Latest design (from the electronics designers @UNIGE)

2 options for back side connections (direct connector vs Flex…)



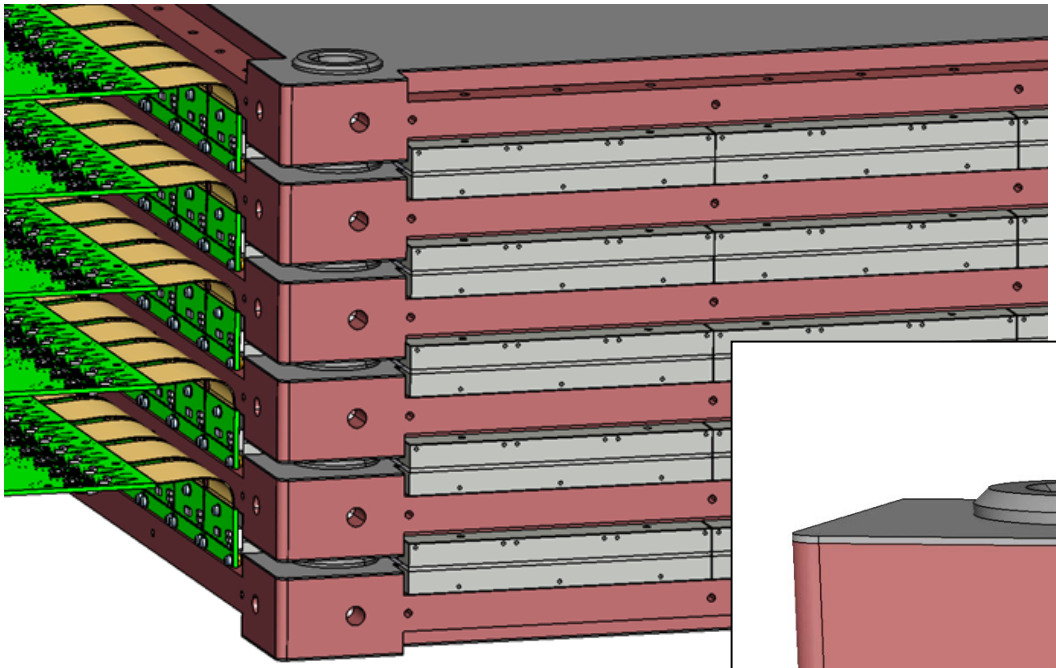




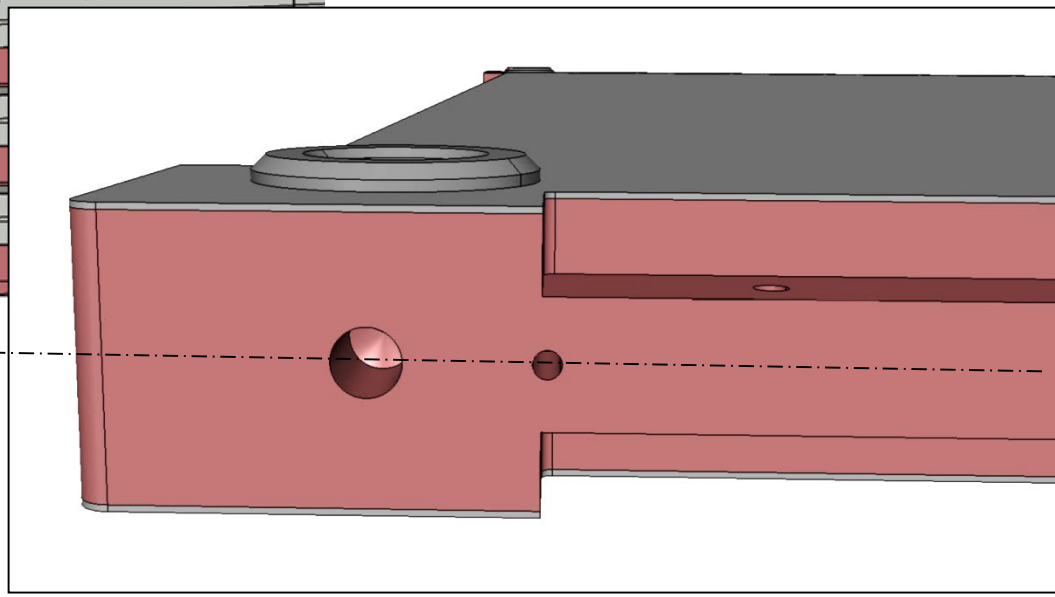
- FEB board is populated on both sides
- SiPM alignment thru 3 M1,6 screws
- A first prototype is available
- The options depends on the FRB design & accessibility issues (see next slides)

# FIT Design overview

**New Design: 6 TRAYS (5X / 5Y active planes… single READ OUT)**



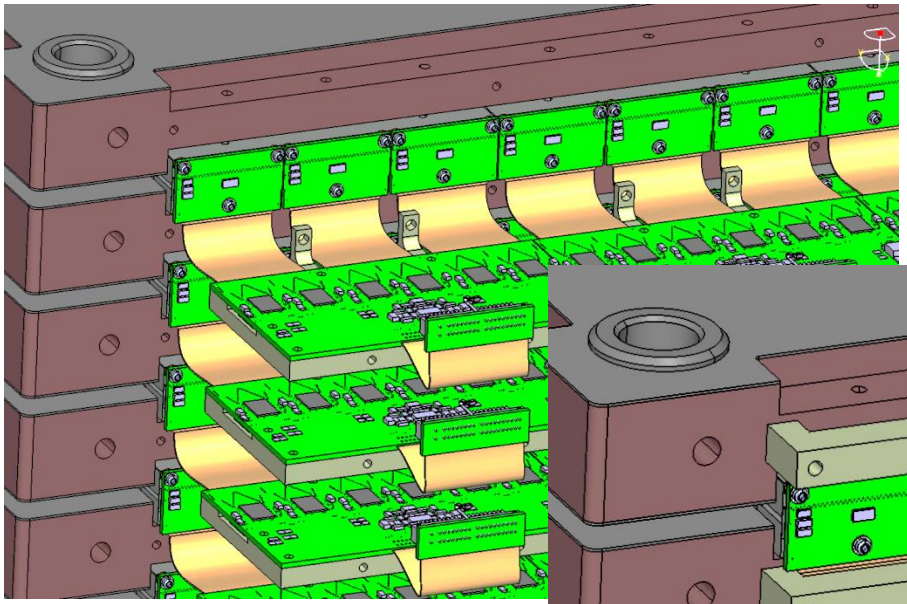
From 20mm to 25 mm thick core



- TRAY is now symmetrical / XY plane
- Mechanical stability is enhanced
- Manufacturing is simplified

# FIT Design overview

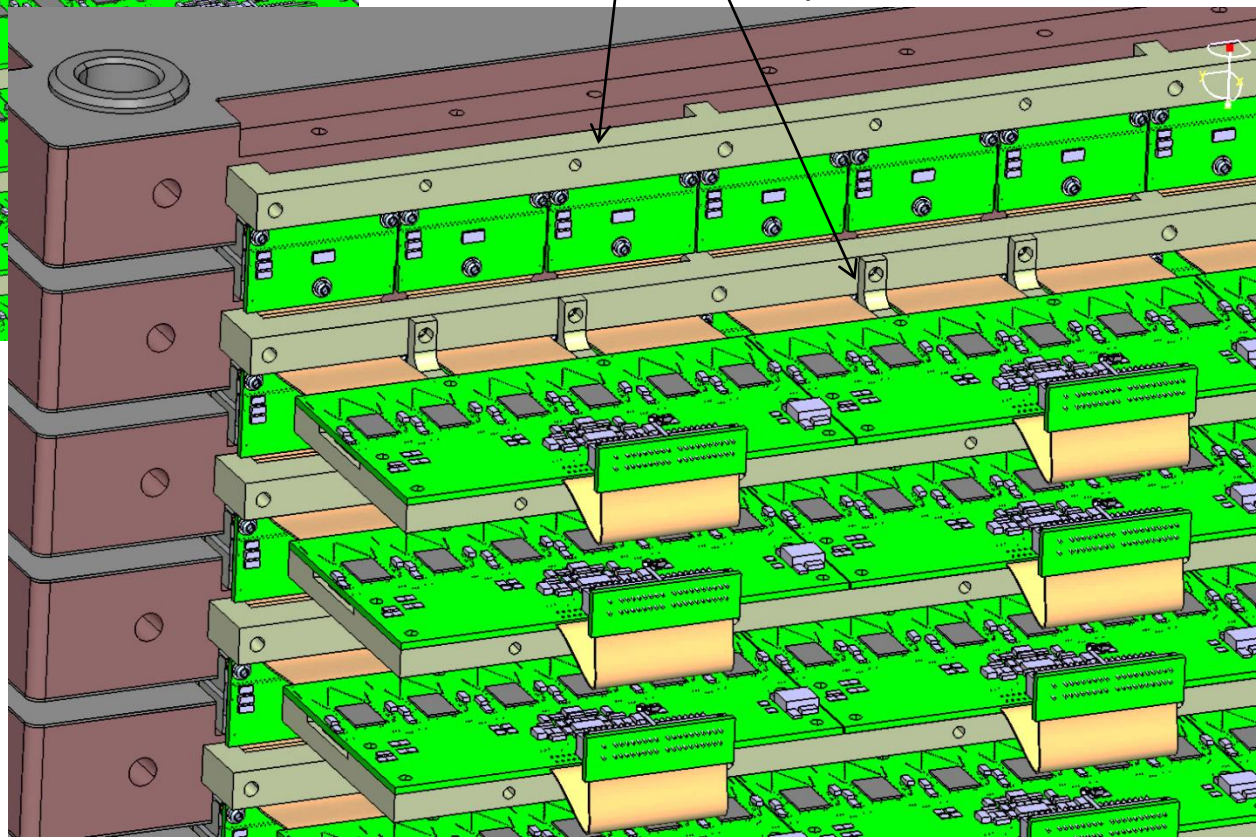
## FEB Latest design (Mechanical assembly onto TRAYS)



Step 1: SiPM fixation

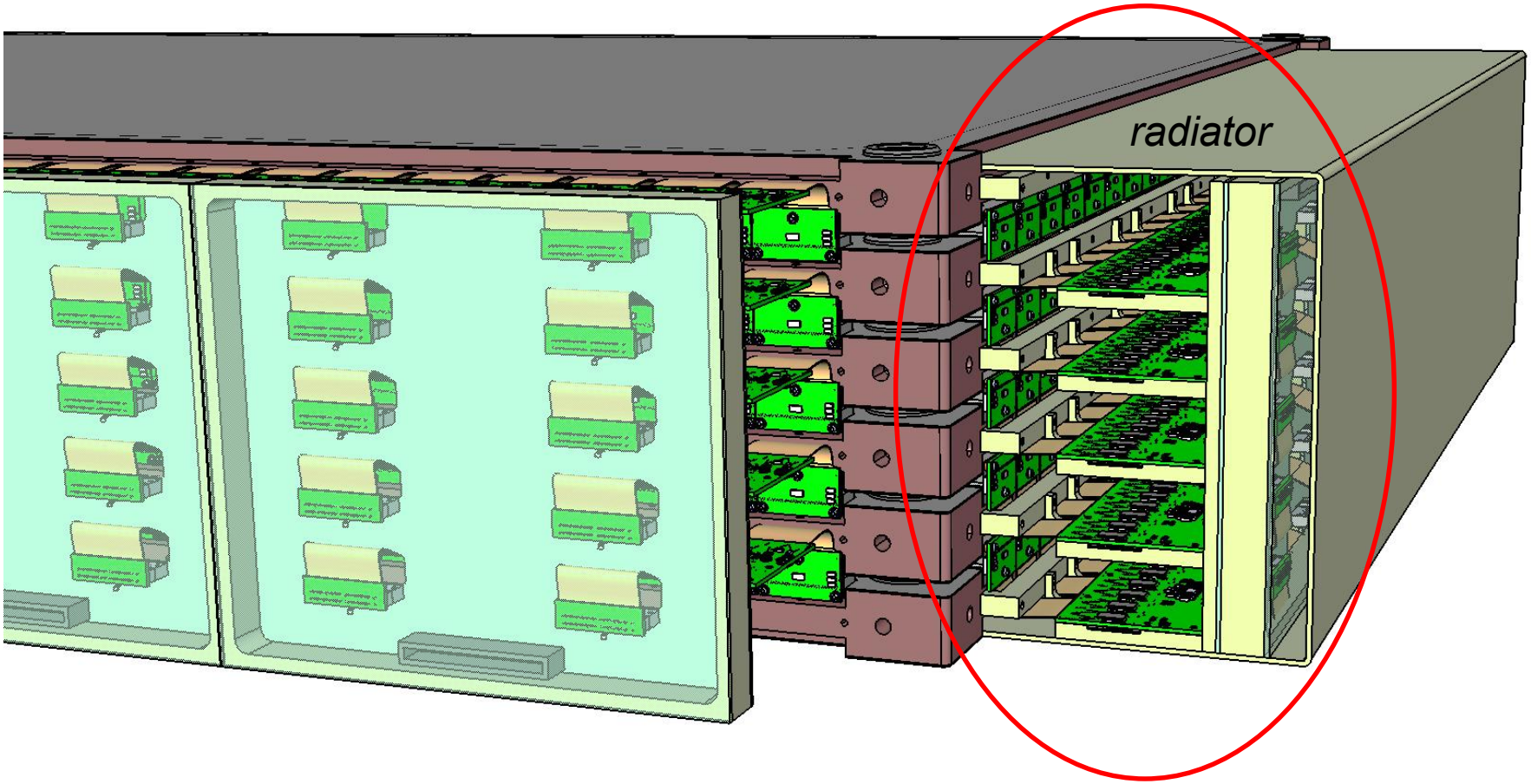
FEB frame design (preliminary)

Step 2: Frame fixation to TRAY



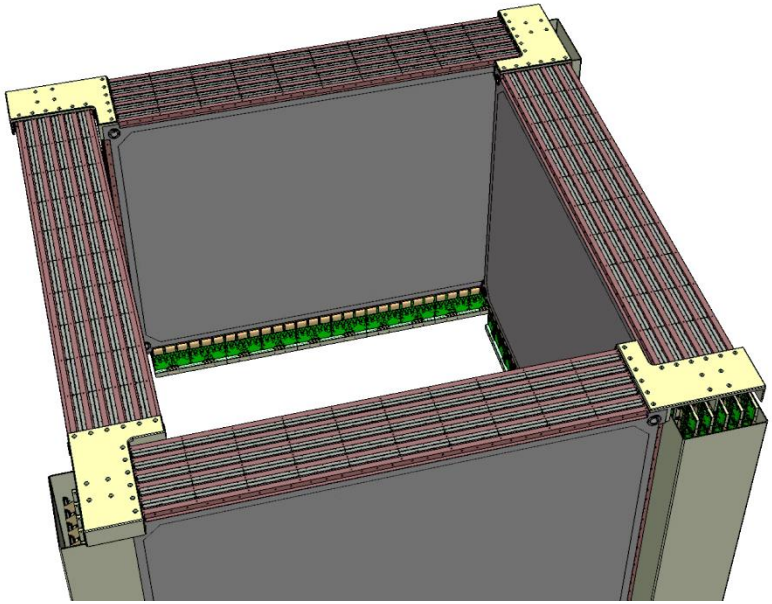
# FIT Design overview

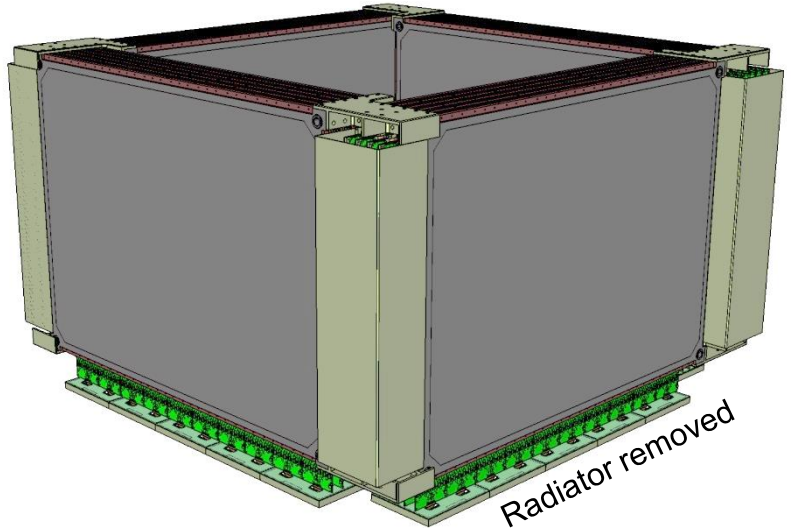
**FRB very first design …**

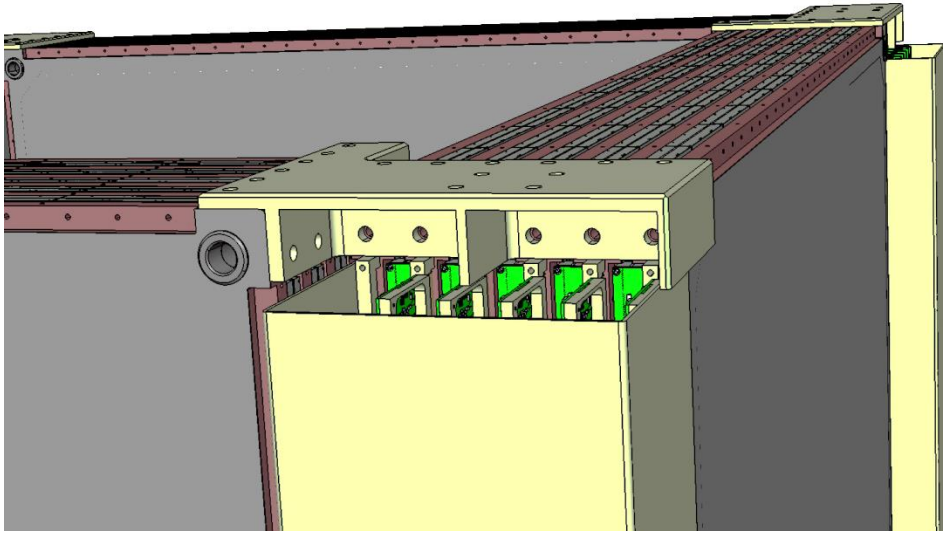


# FIT Design overview

## FIT overall assembly into HERD



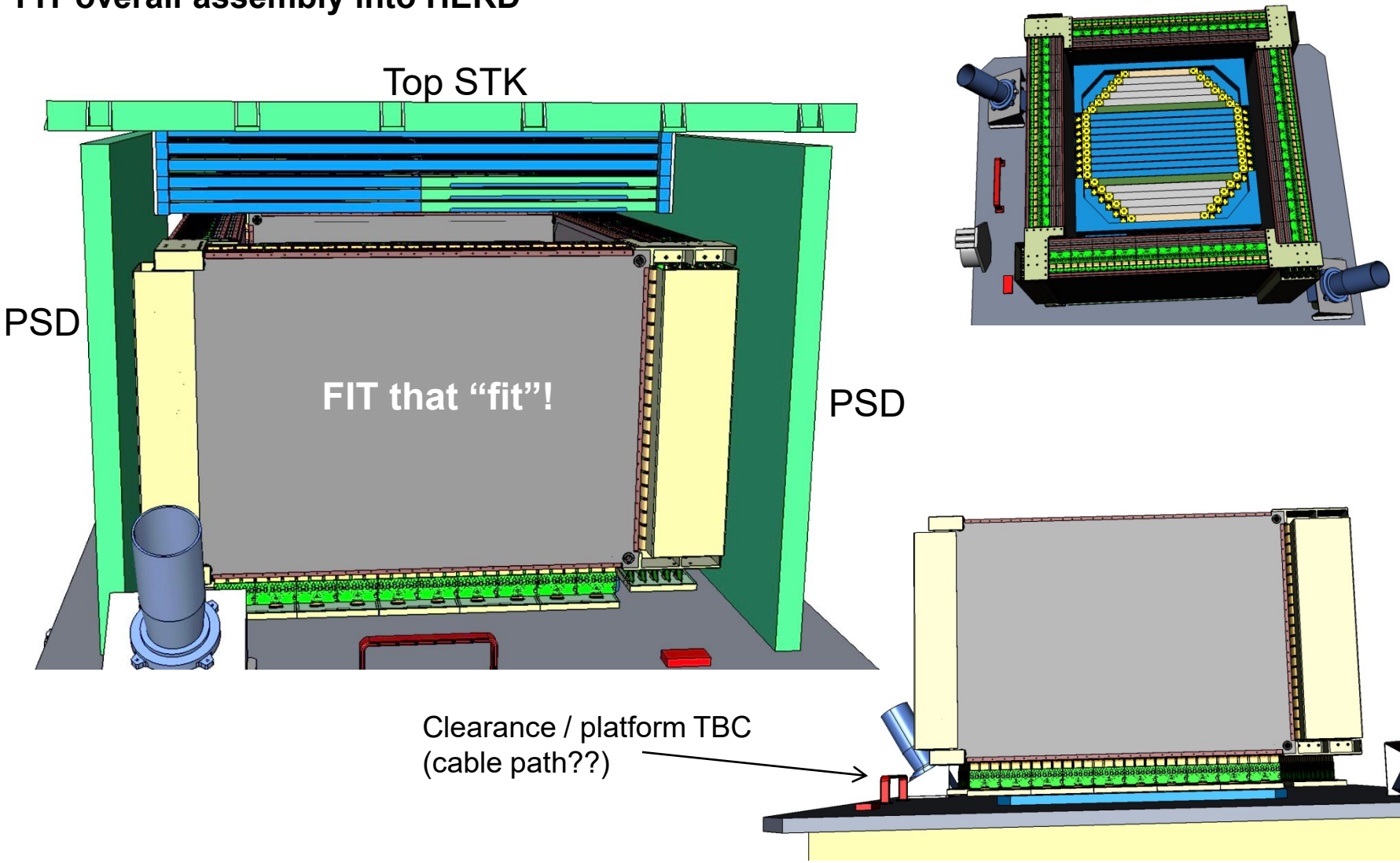


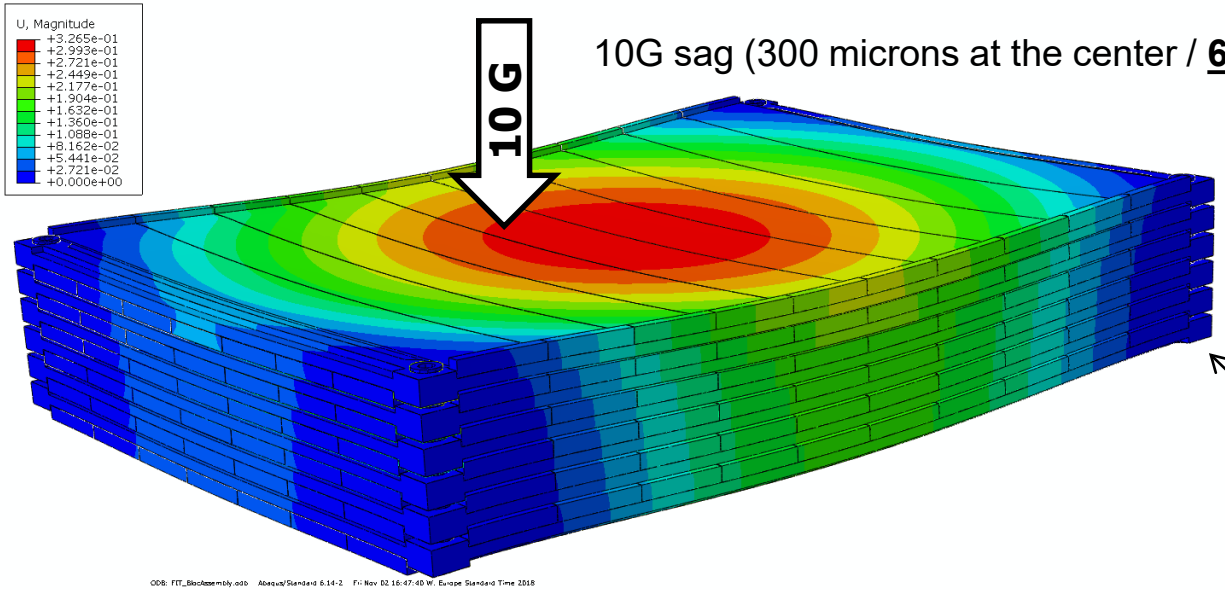
- Smaller corner feet (less material)
- Direct Interconnection between blocks
- Interfaces to HERD / Top STK
- May not need additional interface frame to STK (FEA to be done for validation)

# FIT Design overview

**FIT overall assembly into HERD**



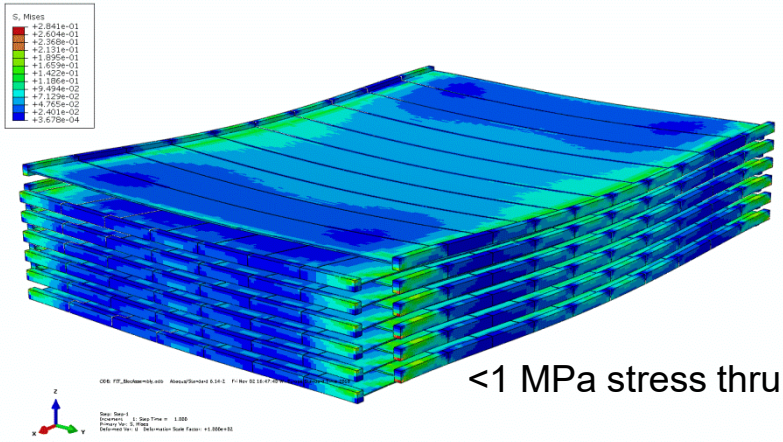
# FEA on TRAY assembly




10G sag (300 microns at the center / **6 plies CFRP**)

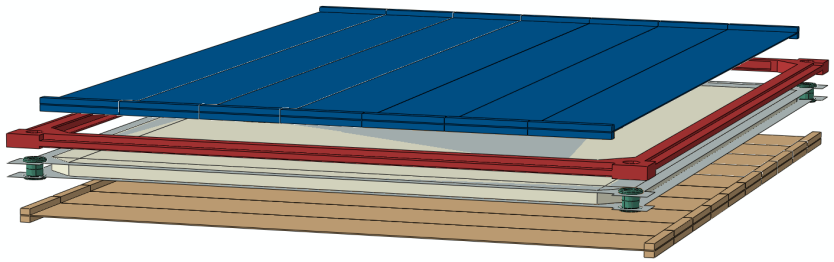
Resting on 4 corners

No FEB side frame (…conservative)




<1 MPa stress thru the MAT

Model of single TRAY



# FIT TRAY Weight status

| Qty | ITEM | Material (density) | Weight (Kg) |
|---|---|---|---|
| 1 TRAY | **Double Skins (6 plies)** | CFRP M55J (d=1.6) | **1.48** |
| | **Double Skins (4 plies)** | CFRP M55J (d=1.6) | **0.99** |
| | **Core 1 (20mm)** | AIREX foam (d=0.06) | **0.85** |
| | **Core 3 (25mm)** | AIREX foam (d=0.06) | **1.06** |
| | **Core 2 (16mm)** | AIREX foam (d=0.06) | **0.68** |
| | **Frame (core 1)** | CFRP T300 (d=1.6) | **1.83** |
| | **Frame (core 3)** | CFRP T300 (d=1.6) | **2.41*** |
| | **Frame (core 2)** | CFRP T300 (d=1.6) | **1.20** |
| | **Inserts** | Aluminum 7075 (d=2.8) | **0.06** |
| 7 | **Fiber MAT X (long)** | Plastic and epoxy (d=1.2) | **1.47** |
| 10 | **Fiber MAT Y (short)** | Plastic and epoxy (d=1.2) | **1.70** |
| | | | **7.7 Kg / TRAY** |
| | | | |
| | | **Total weight estimate for 6 TRAYS only** | **46.2 Kg max + FRB/FEB** |

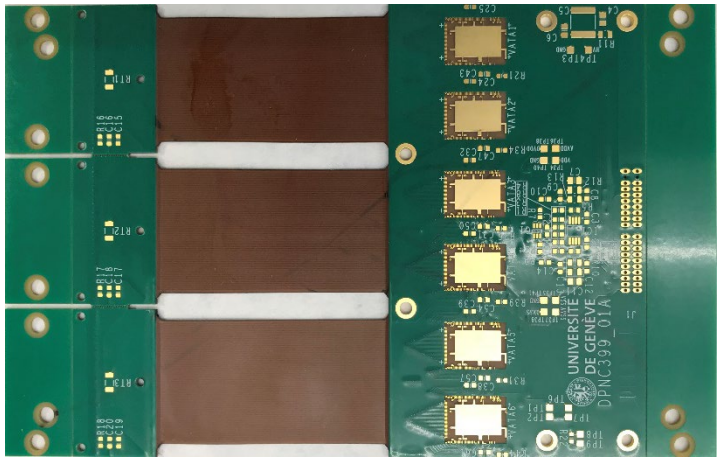
# Electronics designs

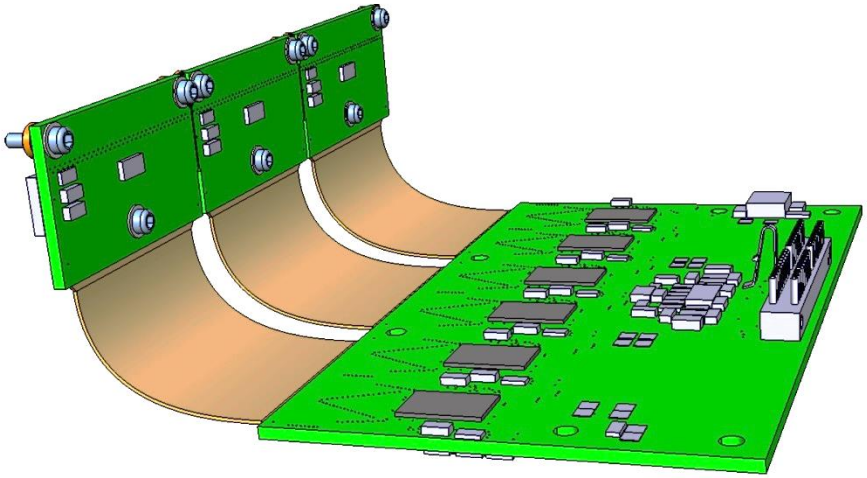
- Front-end electronics board
- Front-end DAQ board
- Fit Readout Board (FRB)

Yannick Favre, Daniel La Marra

# Front-end Electronics board

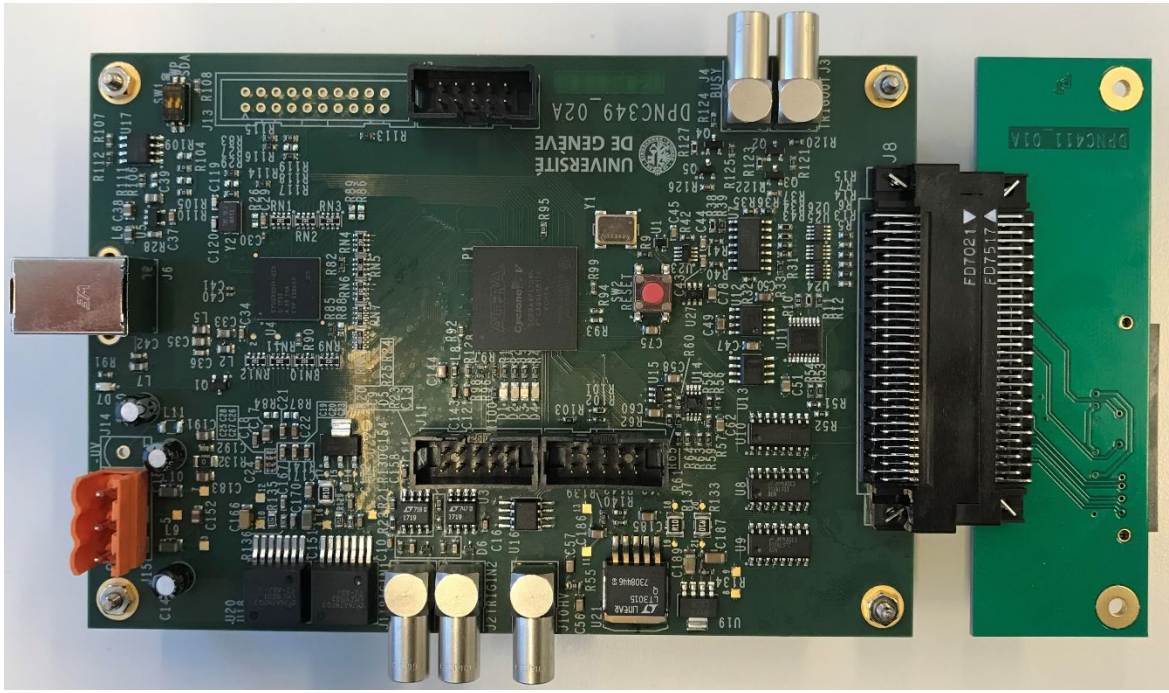
- Designed to read out three SiPM arrays.
- The present design uses six VATA ASICS.
- Another ASIC will be chosen for the flight model (next talk).
- The boards have been delivered, mounting of the first board will start in two weeks.
  - A preliminary study will be done to define the precision of the SiPM positioning and alignment.
  - Then, all the components will be mounted on the board.





# FEB DAQ board

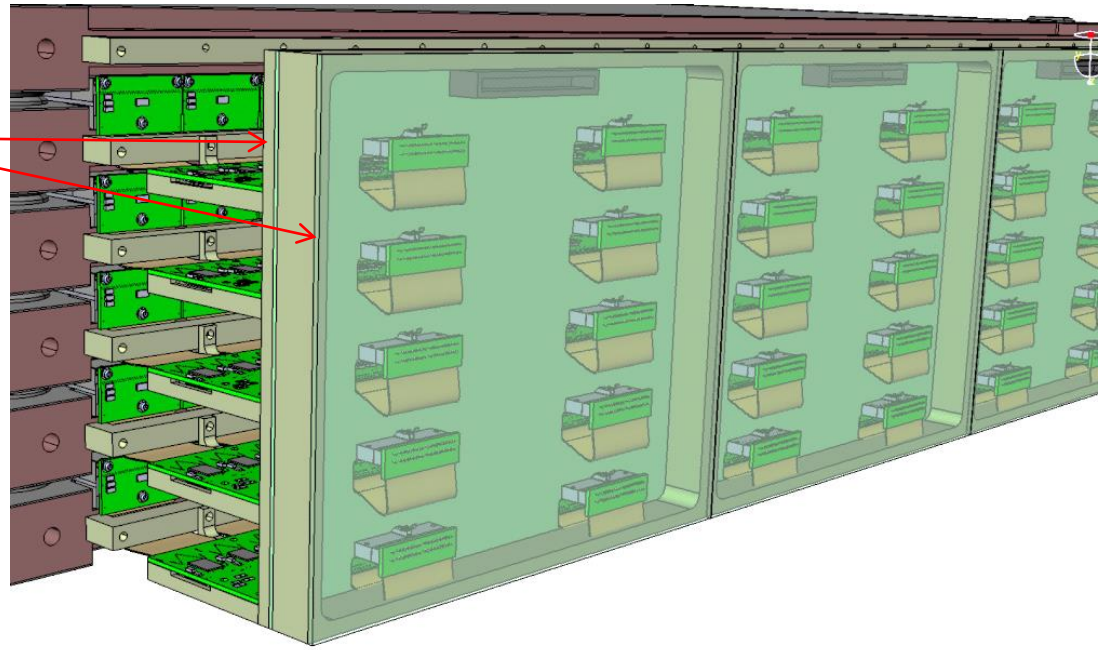
- The DAQ board is compatible with the old FEB design (2-VATA board).
- Firmware to readout the 2-VATA board is ready.
  - The new DAQ boards will be used for the first time at the DAMPE beam test next week.
- The firmware will then be adapted for the FEB with 6 VATAs.
- Four DAQ boards have been assembled.



# The FIT Readout Board (FRB)

- Dimension of a single board: 198 x 200 mm
- In the present design the FRB shall read out 10 FEBs.
- The FRB circuit will actually be composed of a stack of boards:
  - One hosting the FPGAs for DAQ control and communication.
  - One hosting the power supply.
  - This is a similar approach to the one chosen for the STK of DAMPE.

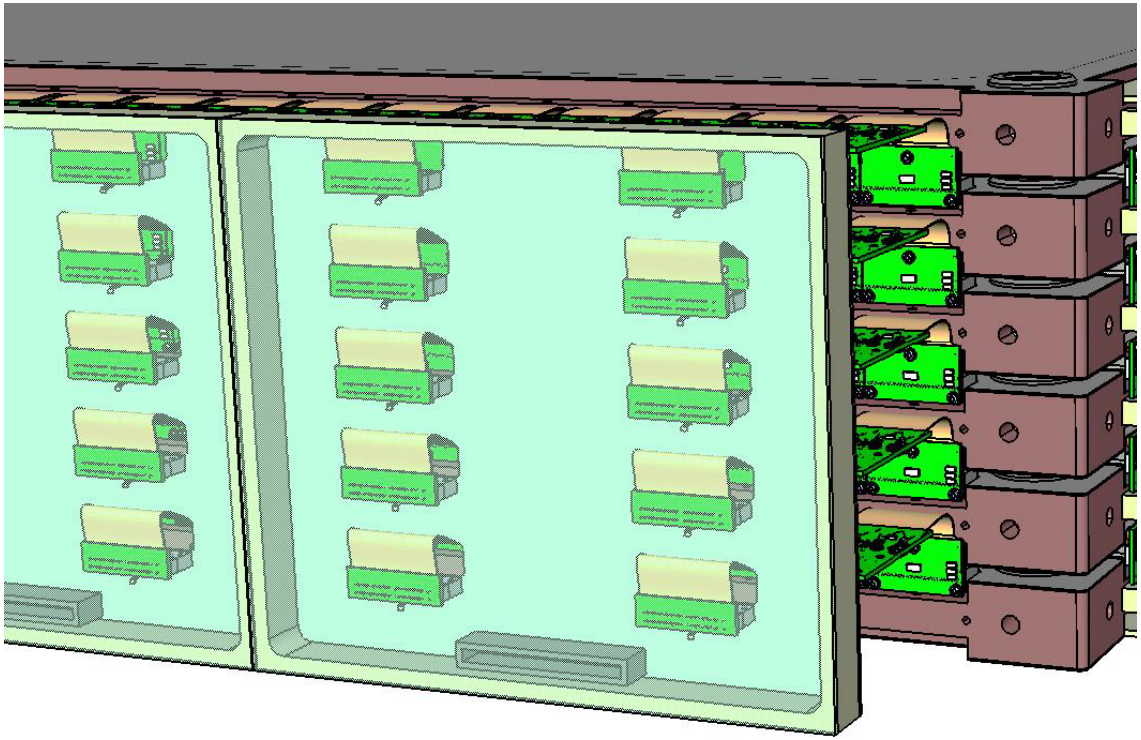
2 boards stacked up
(Dampe STK like)



# The FIT Readout Board (FRB)

The TRB specifications are being written. Two versions are documented:

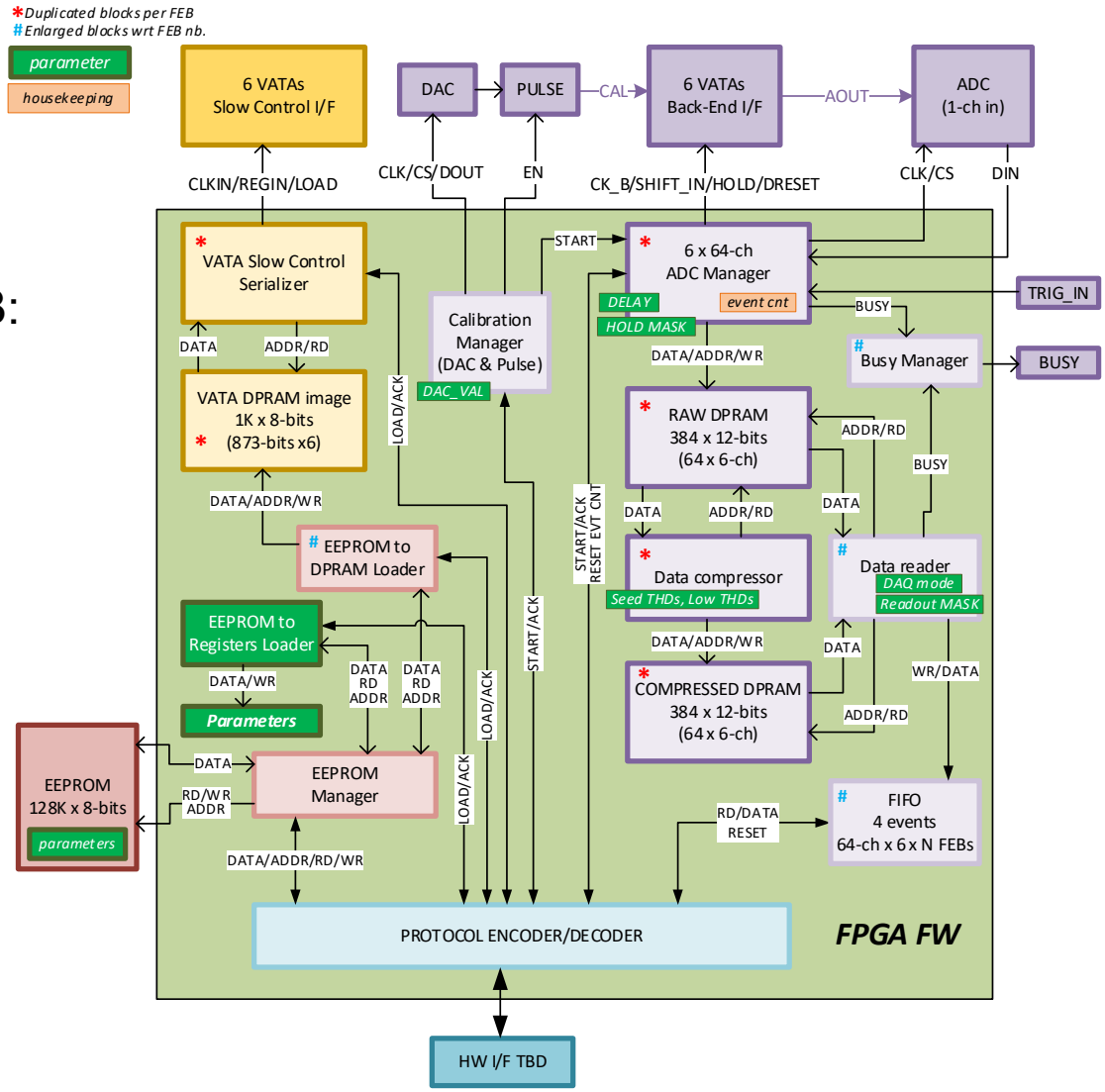
- The Engineering Model (EM) will read out max. 4 FEBs (with VATA ASIC).
- The Flight Model (FM), will read out 10 FEBs, with the final ASIC.
- One FIT side tracker will have 9 FRBs, reading out 85 FEBs.
- The total FIT tracker will have 36 FRBs, reading out 340 FEBs.



# FPGA firmware architecture (1)

Partial architecture for 1 FEB:

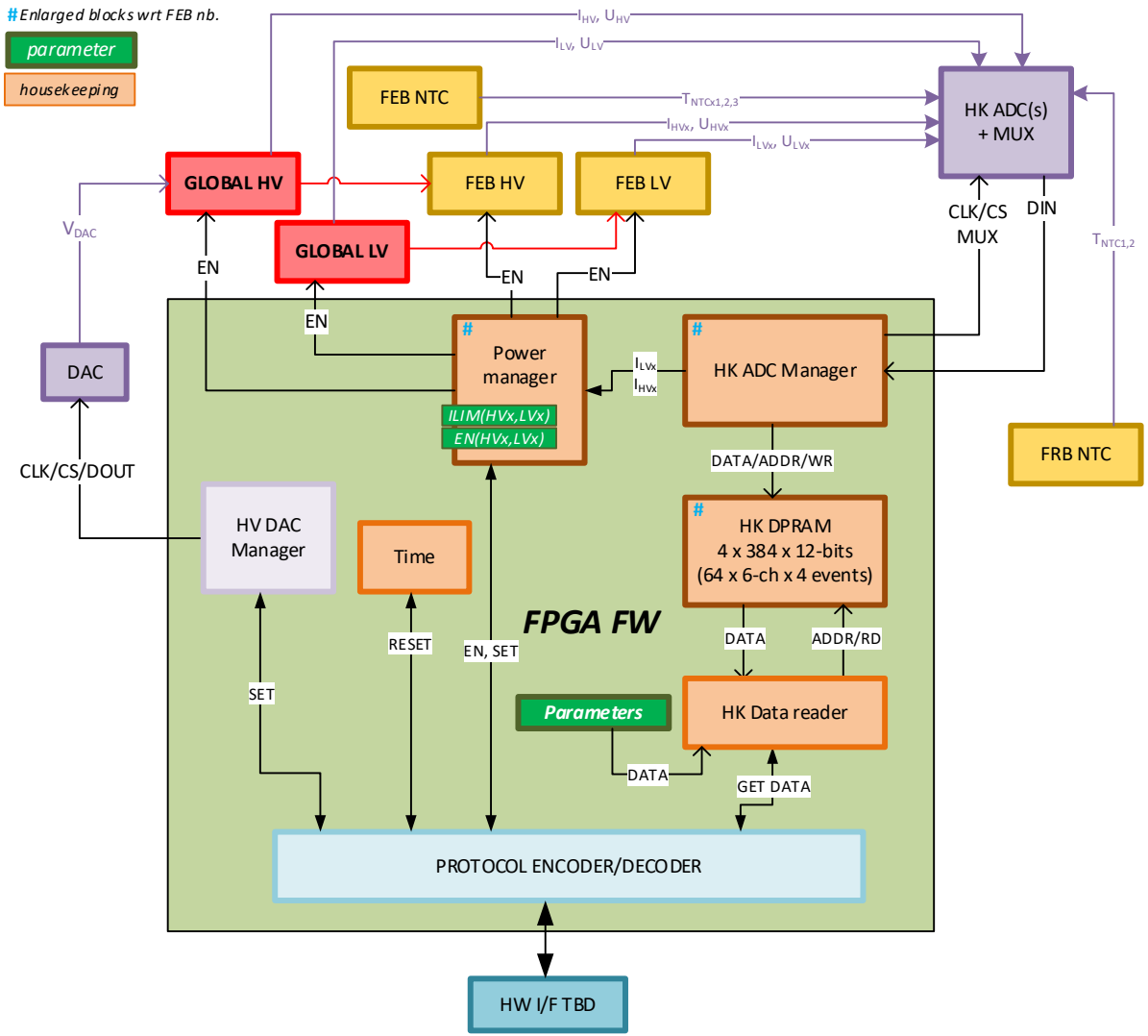
- Slow control blocks
- Calibration blocks
- Readout blocks



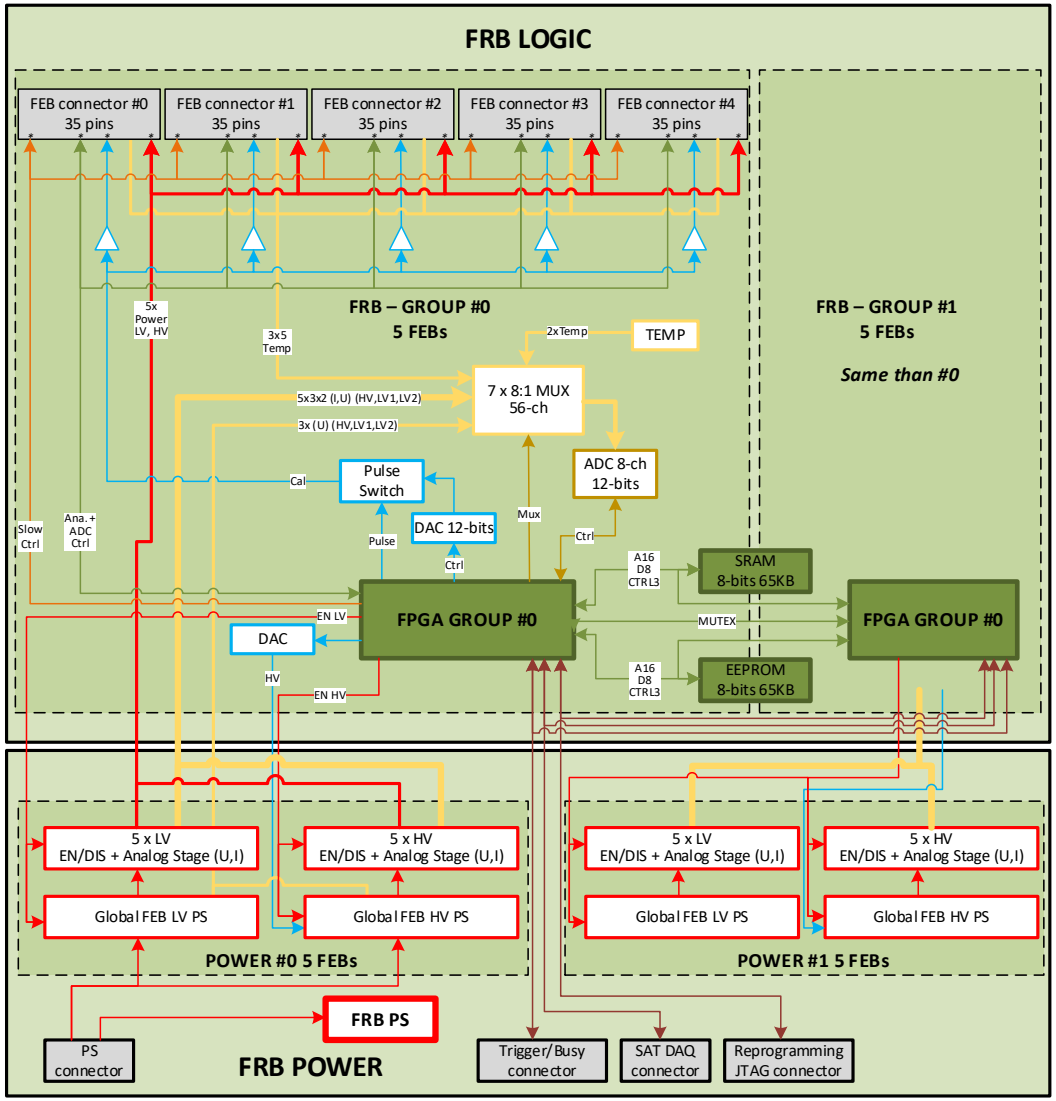
# FPGA firmware architecture (2)

Partial architecture for 1 FEB:

- power blocks
- safety blocks
- housekeeping blocks



# FRB architecture overview



# FPGA choice

- Microsemi FPGAs are a natural choice for space application.
- The RT ProASIC3 FPGAs are reprogrammable, nonvolatile and rad-hard flash-based FPGA. Triple-chip redundancy is not required.
- For prototyping, the RT3PE3000L (600L) uses the same silicon than A3PE1000L (600L) so migration is very easy. The space packages available are CQFP, CGA or LGA.

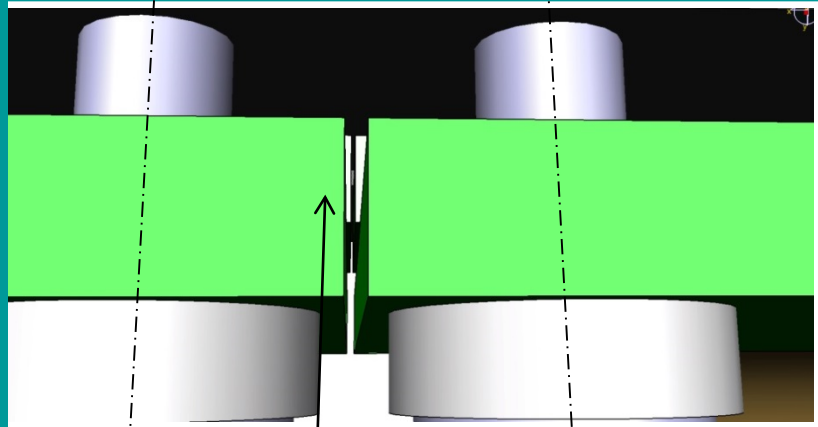
- As the FPGA is reprogrammable, it would be good to keep the possibility to reprogram the FPGA during the mission.
  - This means having JTAG lines connected to main DAQ computer.

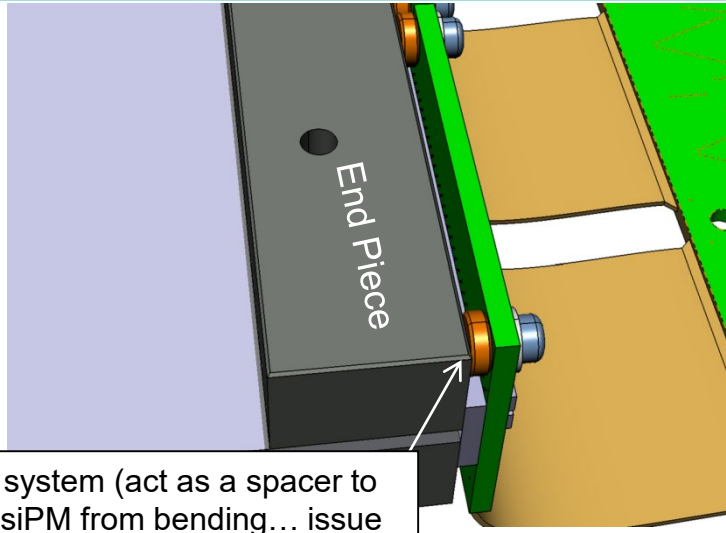
# Open questions

To go further with the development of the FIT, there are some open questions, listed here:

- Is there a documentation about the qualification levels / qualification test specifications for the subdetectors of HERD (vibration, shock, thermal, thermal vacuum, EMC/EMI) ?
- What are Radiation hardness and SEU specifications for the electronics of HERD ?
- What are the thermal constraints ? (e.g. radiator temperature)
- What is the foreseen communication protocol between the subdetector DAQ systems and the HERD DAQ ?
- We are considering working with a re-programmable FPGA, in a way that possibly the code can evolve during the mission. For this, we would need the main DAQ computer to have the ability to do the reprogramming, having the JTAG lines connected to the main computer. Is this approach feasible ?

# FIT Design overview

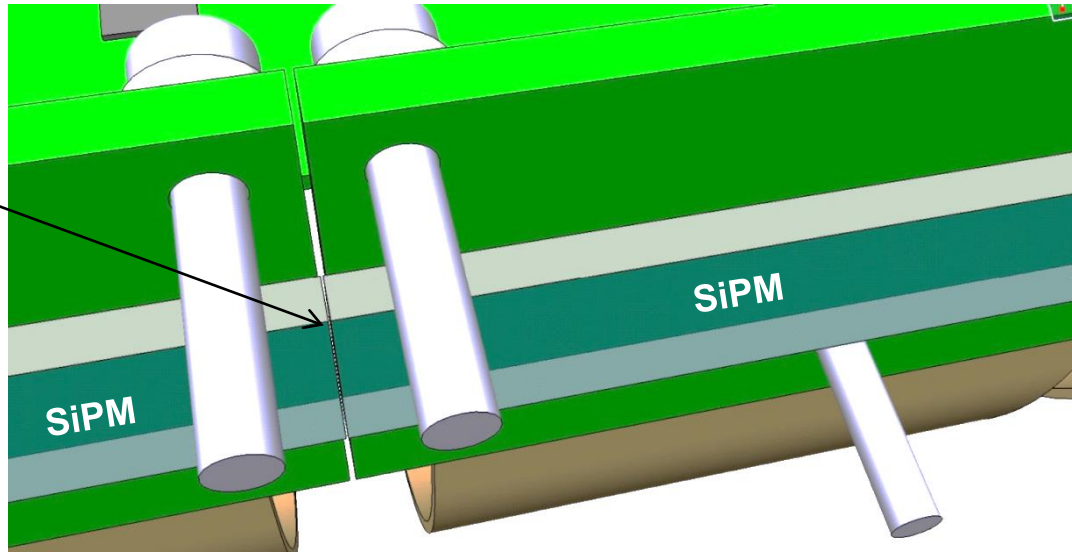





Self locking system (act as a spacer to prevent the siPM from bending… issue seen at last Test beam!)

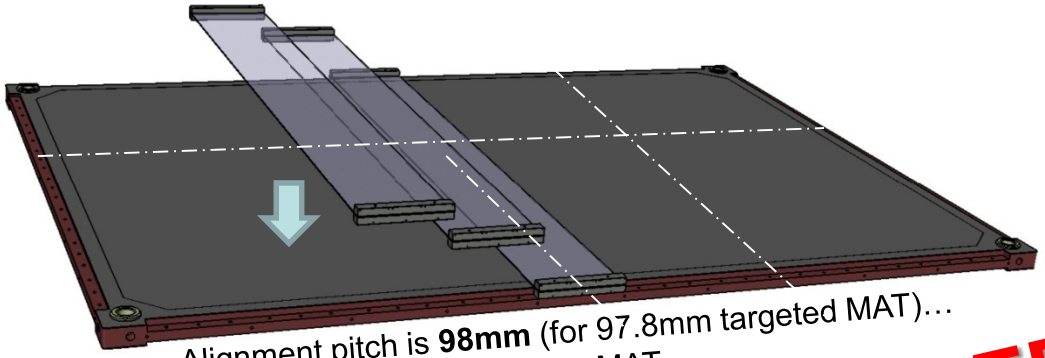
Clearance between SiPM ( < 50 microns)

**Highly precise SiPM assembly on PCB**

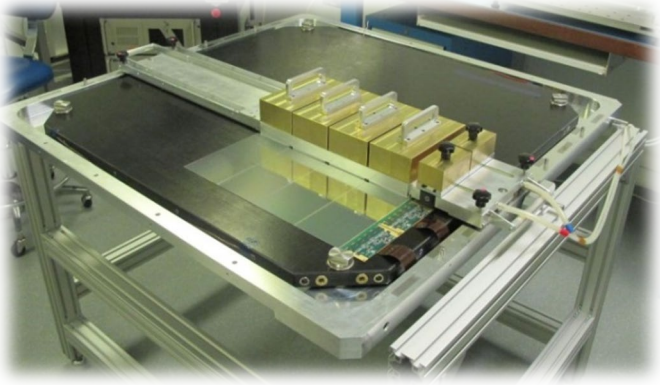


# FIT Design overview

**Fiber MAT "loading" process** (as compared to DAMPE STK's)



Alignment pitch is **98mm** (for 97.8mm targeted MAT)…
= **200 microns** gap between MAT



Assembly jig for DAMPE STK @ Geneva

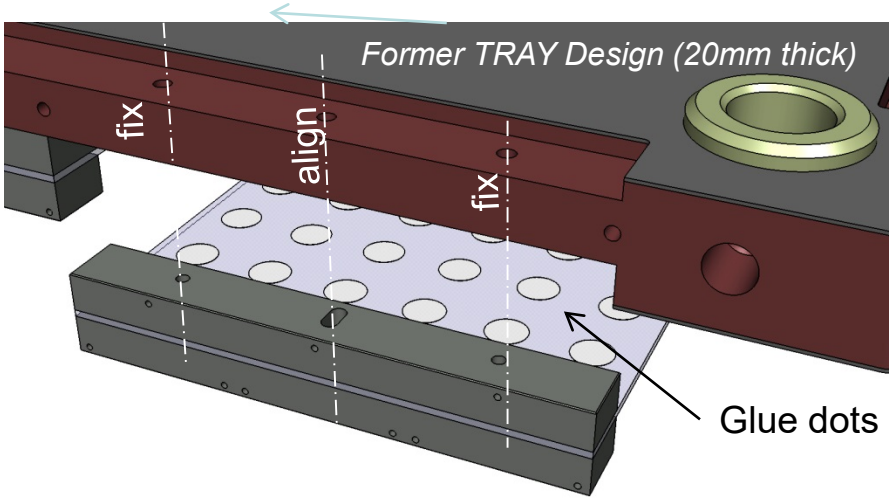
**REMINDER**

**Advantages** (comparing to STK loading)

- No need of dedicated long jigs (ref. on TRAY)
- Fiber MAT not fragile… easy handling
- 2 levels of fiber MAT fixation (screw + glue)
- No corrosion issues (easy storage)
- SiPM can be fixed later on TRAYS

⇩

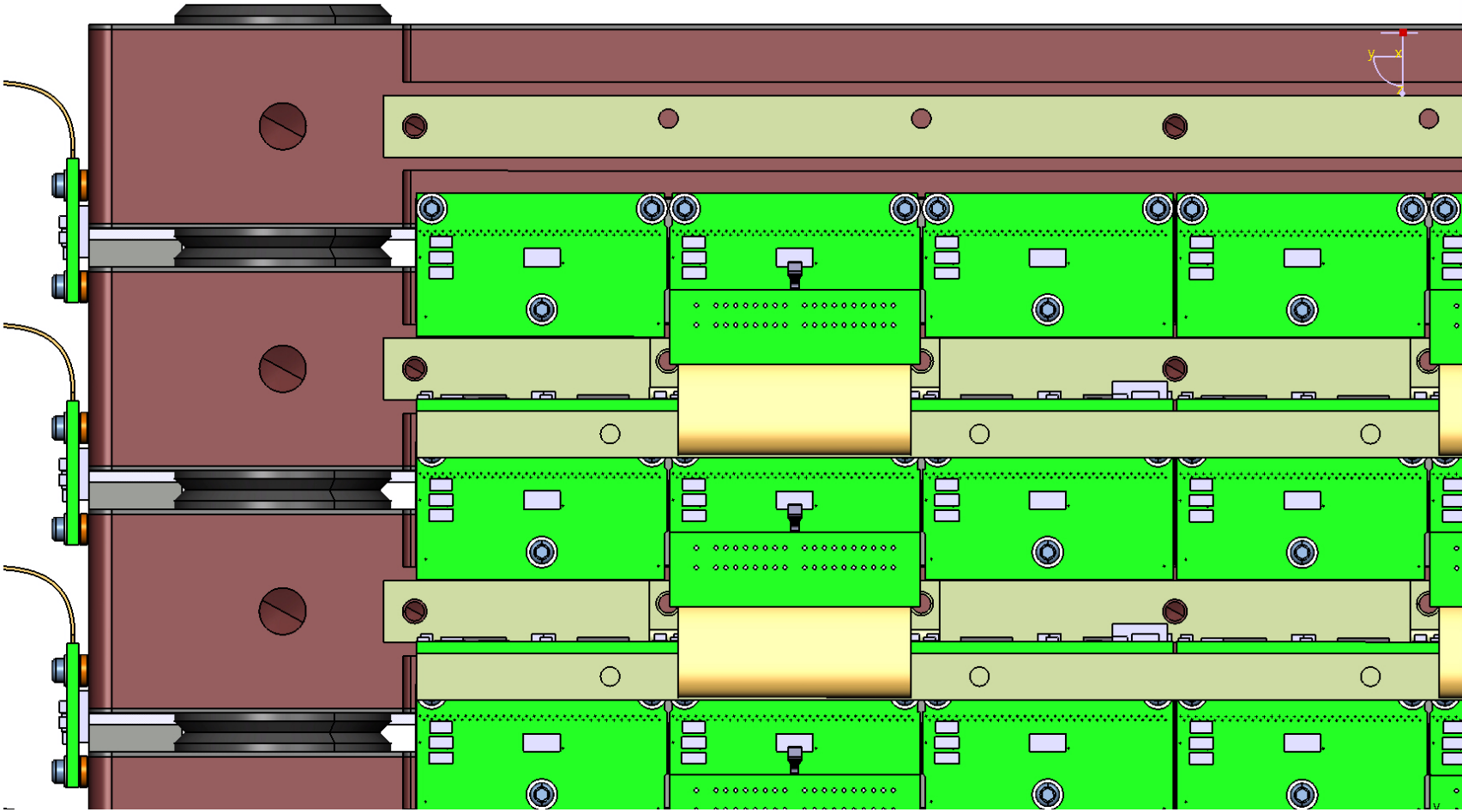
Leading to **time saving** for TRAY loading



# FIT Design overview

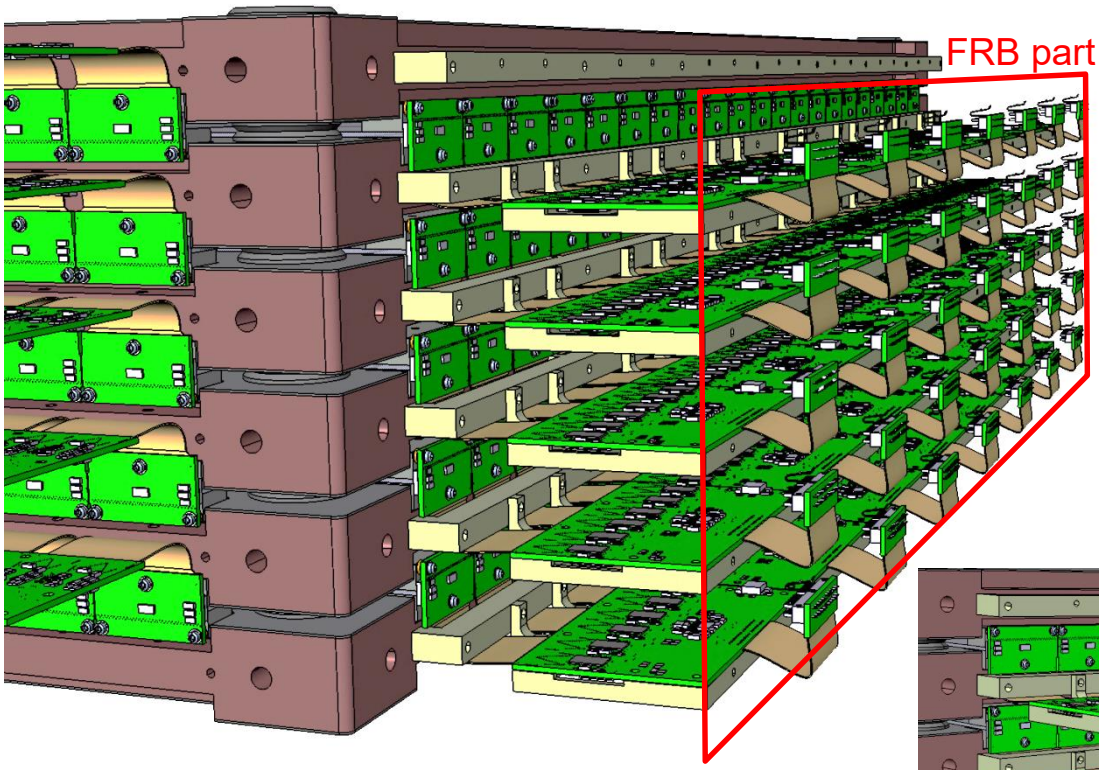
## FEB Latest design (Mechanical assembly onto TRAYS)

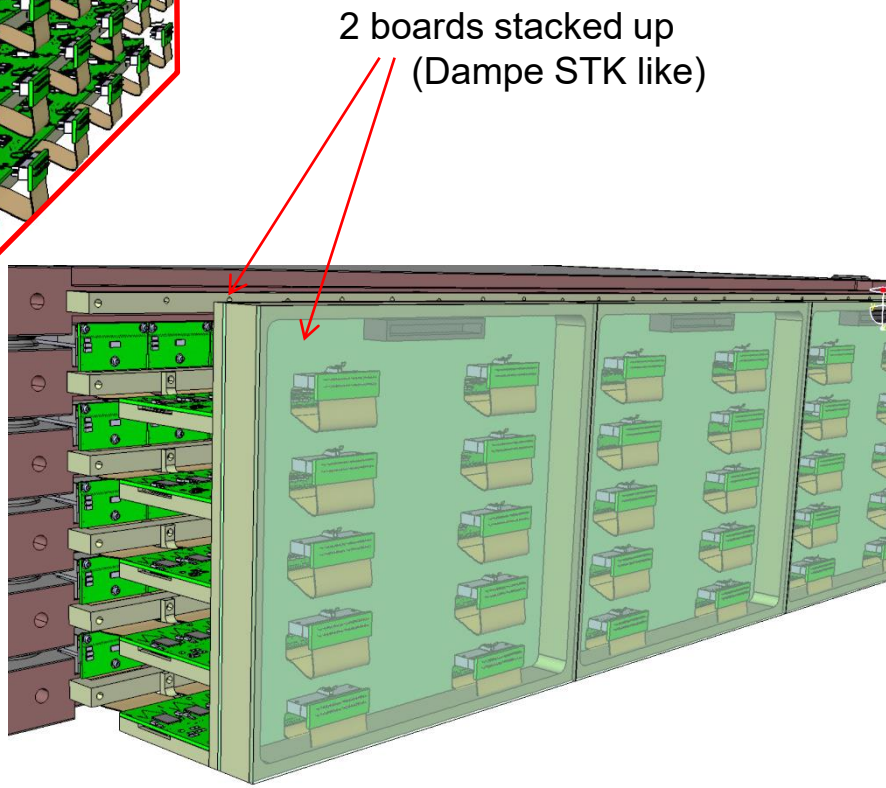
Every screw accessible from “outside”… by playing with flexes!



# FIT Design overview

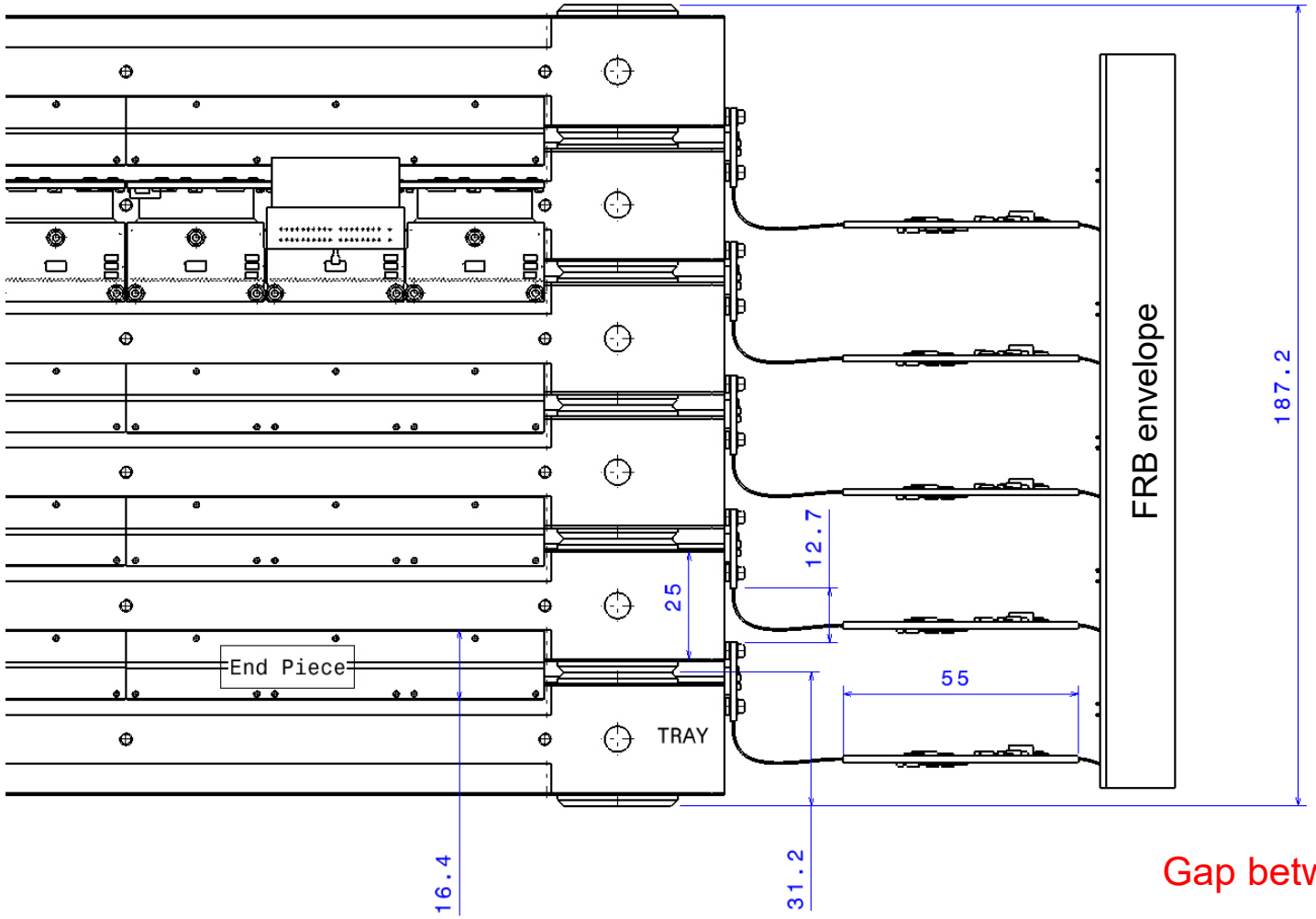
**FRB very first design …**



# FIT Design overview

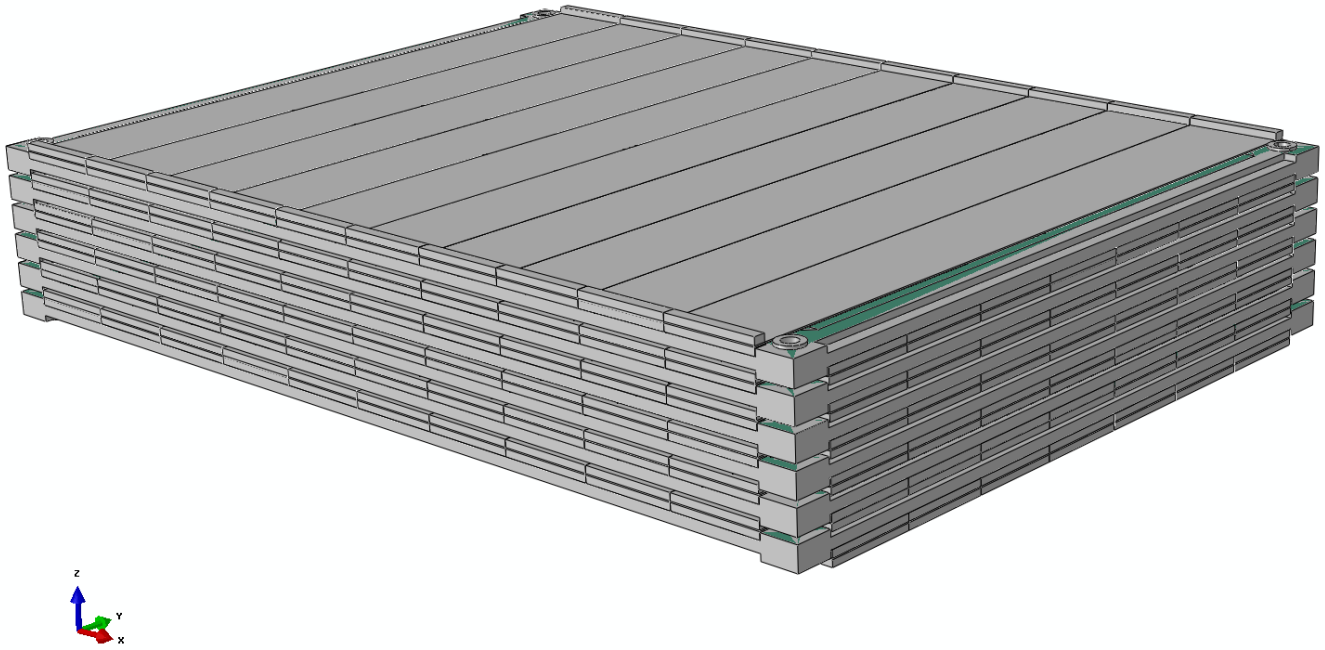
## New Design: 6 TRAYS (overall size)




Gap between MAT: 2.2mm

# Preliminary FEA (simulations)

## *From single TRAY to full assembly*



# FRB architecture overview

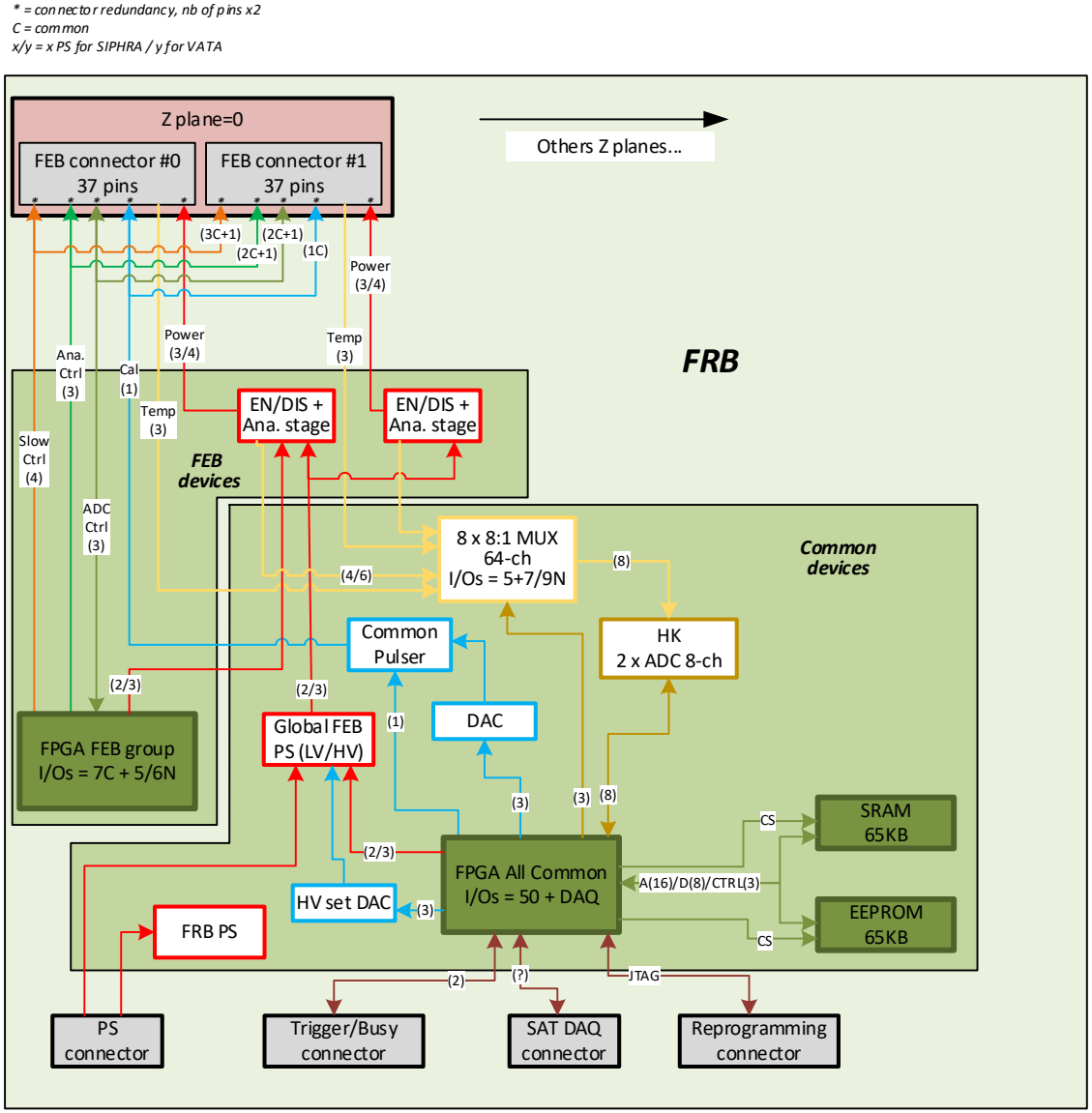
Two FPGAs will be required. There are two possible approaches on the FPGA task division:

- **Per FEB:** i.e. having 5 FEB per FPGA and the same firmware for both of them:
  - Drawback: The SRAM & EEPROM memories should be duplicated, 1 for each of the FPGA (assuming we need external SRAM memory).
  - Advantage : safer approach, we should be able to handle all the SiPM channels with 2 FPGAs (1920 channels per FPGA, memory and registers resources divided by 2)
- **Per functional block:**
  1st FPGA: SiPM ADC channels handling
  2nd FPGA: HK, PS enable, counting, synchronization, calibration
  - Drawback: To be sure to handle all 3840 SiPM channels in 1 single FPGA. 2 different firmware required.
  - Advantage: To be able to handle more advance control for HK & eventual HV compensation

The “per FEB” task division has been chosen.

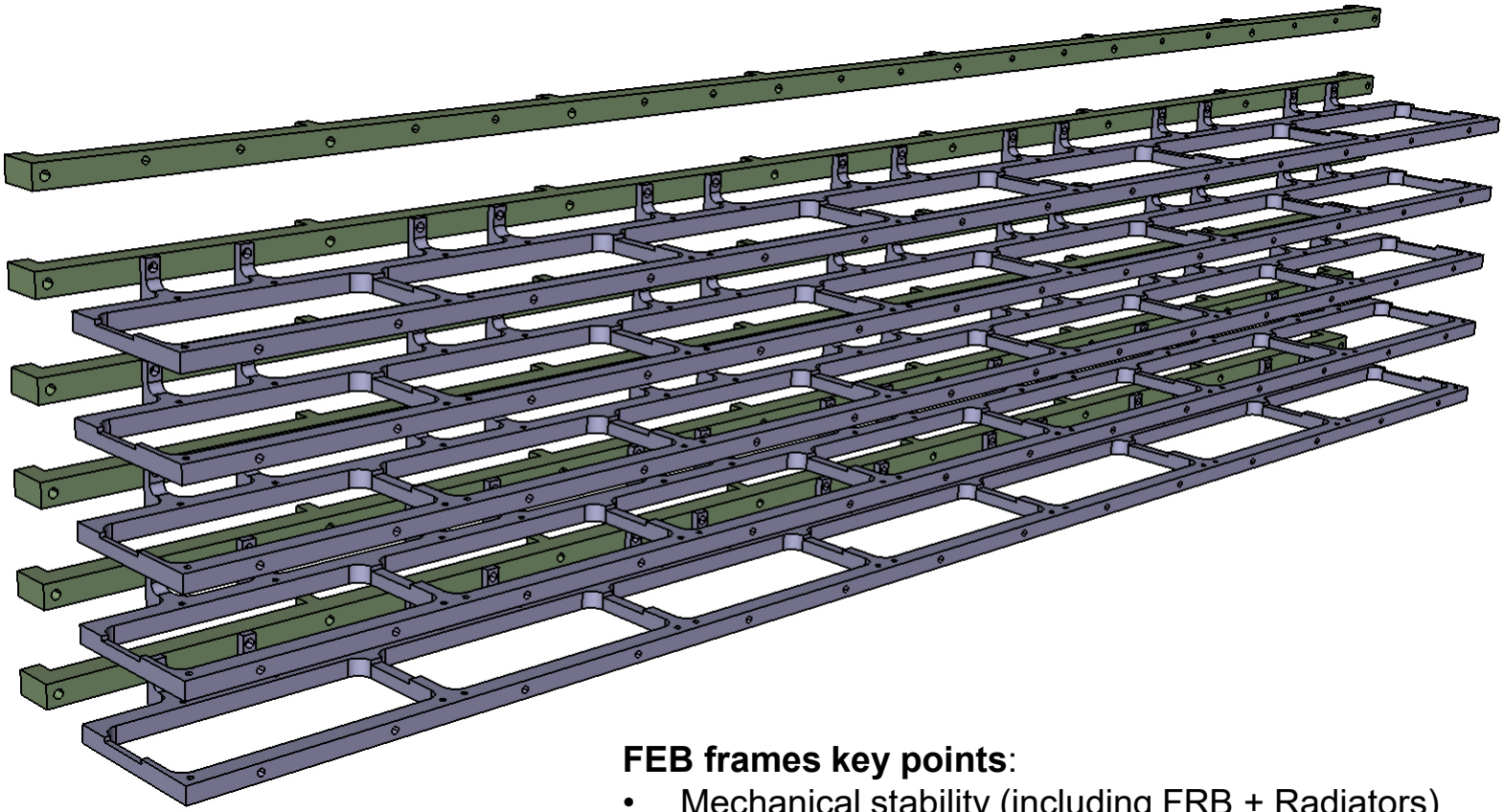
# FPGA partial functional architecture

- Preliminary functional view of the FPAG I/Os
- Only one group of 2 FEBs is shown, for the 4 others FEBs groups, the 'FEB devices' block should be duplicated.
- The 'Common devices' block is required only once.



# FIT Design overview

## FEB Latest design (Mechanical assembly onto TRAYS)



**FEB frames key points**:

- Mechanical stability (including FRB + Radiators)
- Thermal management (thru the aluminum pieces)
- Standard CNC machining
- Ease the mounting / dismounting (maintenance on SiPM)
- Interface to the FRB (see next slide)

# Preliminary FEA on TRAY

## Wrap up & Discussions

| Simu Type | 6 plies M55J / 20mm core | 4 plies M55J/ 20mm core | 6 plies M55J/ 16mm core | 4 plies / 16mm core | 6 plies M55J / 25mm core |
|---|---|---|---|---|---|
| SINGLE TRAY | | | | | |
| Acc. 10G (Def) | 0.47mm | 0.51mm | 0.68mm | 0.73mm | |
| Frequencies (First modes) | 91Hz / 157Hz / 170Hz | 88Hz / 149Hz / 170Hz | 75Hz / 132Hz / 142Hz | 72Hz / 126Hz / 142Hz | |
| TRAY ASSEMBLY | | | | | |
| Acc. 10 G (Def) | | | | | **0.32mm** |

**In theory**
following the single TRAY FEA, “4 plies + 25mm core” will lead to a deflection < 0.4mm