Evaluating the NanoXplore 65nm RadHard FPGA for CERN applications

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Outline

- FPGA under study
- Irradiation Test Setup
- Experimental Results
- Future steps
- Conclusions

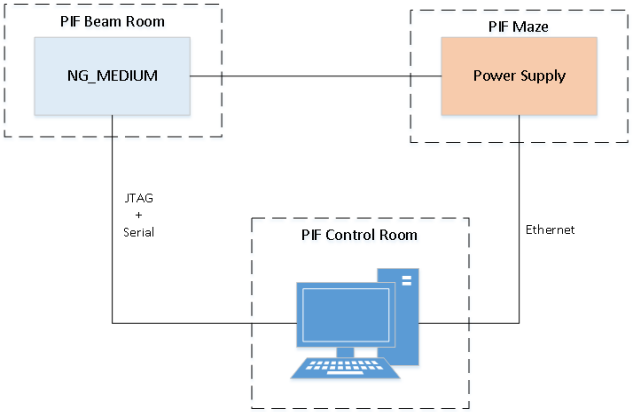
FPGA under study

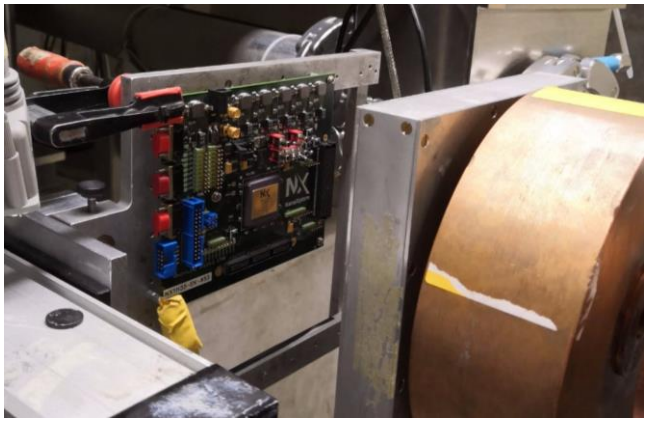
- New effort from EU to fabricate an RadHard ITAR-free FPGA
- NanoXplore leading the effort with NG-MEDIUM (NX1H25S) as the first FPGA to come out.
- STM C65 (65nm RadHard ST process)
- Rad Hard Configuration memory (CRAM) cells and Flip Flops
- CRAM Integrity Check (CMIC)
- NX1H25S specifications:
  - 56×48kbit RAM blocks (BRAM)(ECC available)
  - 34272 LUT – 4
  - 32256 Registers (Flip Flops)
  - 8064 Carry modules
  - 112 Digital Signal Processor (DSP)
  - 24 Clocks (4 PLLs)
  - 13 I/O Banks
- Python based software
- Synthesis, place and route in house developed

NanoXplore NG medium

Irradiation Test Setup

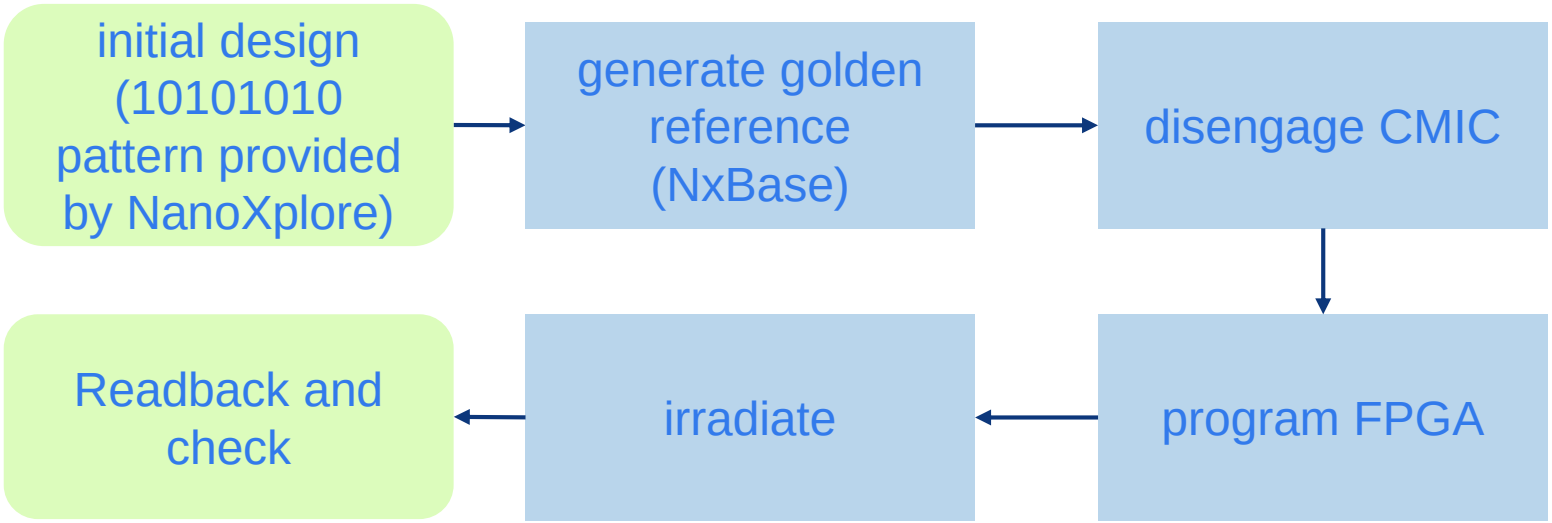
- Combination of three irradiation campaigns for the Qualification of the FPGA using 200MeV protons for SEE testing
- PIF instrument at PSI facility, Villigen, Switzerland
- 2 NG-MEDIUM Evaluation Kits as a test platforms
- Built-In-Self-Tests (BIST) for fast prototyping and high performance
- Most sensitive and most important parts of the FPGA were targeted:
  - CRAM
  - Block Memory (DPRAM)
  - Flip Flops
  - DSP
  - PLL
  - TID limits
- Transmission of data via UART to control computer
- 25 MHz oscillator
- Remote-Controlled power supply with power limiting and automatic power cycling utility





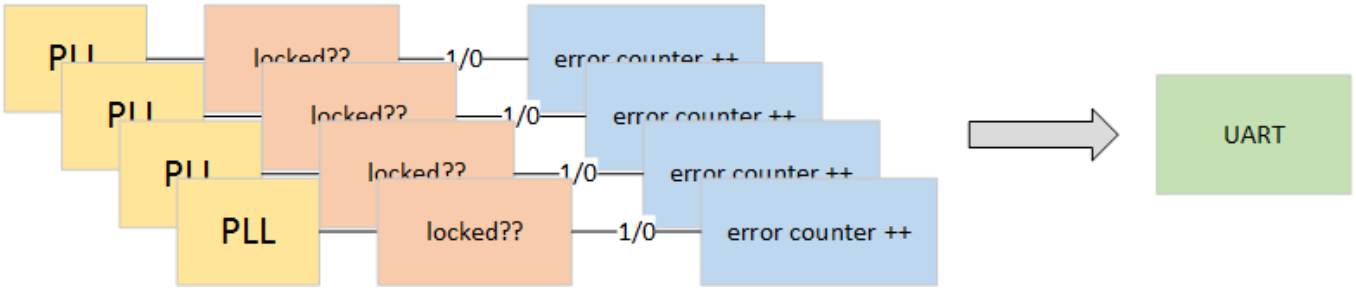
Irradiation Test Setup (CRAM)

- The CRAM is SRAM based using 65nm Rad Hard cells
  - ~6Mbits
- CMIC is able to correct the erroneous cells of the CRAM but is disengaged during the tests
- Static test of the CRAM
- Setup entirely configured using the NxBase2 software



Irradiation Test Setup (PLL)

- Utilization of all PLLs available in the FPGA
- Input clock is 25MHz (board Oscillator)
- Output clock is set to 6.25MHz
- # of clock cycles the lock is lost is transmitted via UART



Experimental Results (CRAM + PLL)

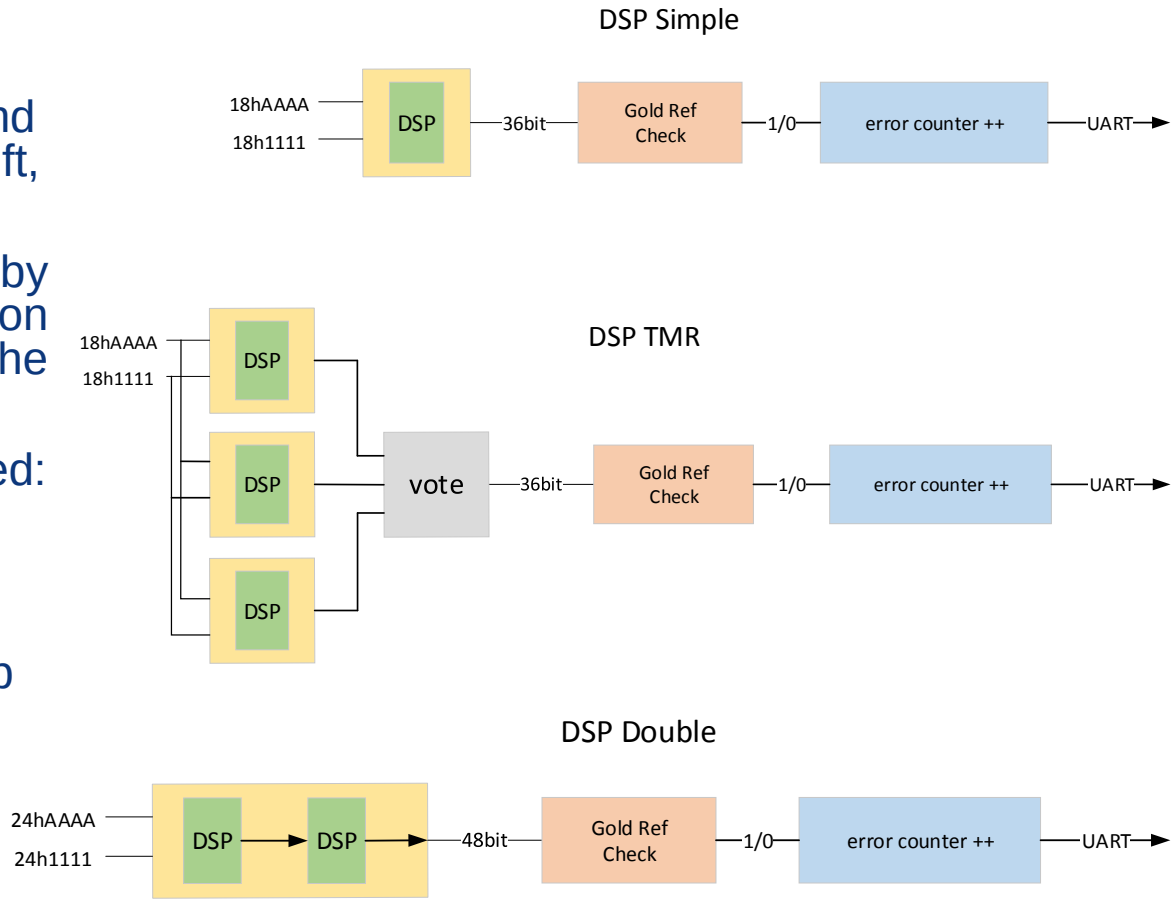
- CRAM
  - Three runs of $3 \cdot 10^{10}$ protons
  - SEUs observed in all three runs
  - CMIC was not engaged -> NO SCRUBBING

run#	fluence	SEUs	σ(cm^2/bit)
86	$3 \cdot 10^{10}$	225	$1.22 \cdot 10^{-15}$
87	$3 \cdot 10^{10}$	189	$1.03 \cdot 10^{-15}$
88	$3 \cdot 10^{10}$	282	$1.52 \cdot 10^{-15}$

- PLL
  - Three runs of $3 \cdot 10^{10}$ protons
  - No loss of lock observed

Irradiation Test Setup (DSP)

- The DSP is a very complex hard coded block able to perform various arithmetic and logic operations (multiply, shift, accumulate etc)
- Tests were conducted by considering the multiplication operation as being one of the most complex
- Three setups were considered:
- 96 DSPs on the DSP simple
- 32 DSPs on the DSP TMR
- 32 DSPs on the double setup (64)
- UART buffers are configured with Fast ECC scheme



Experimental Results (DSP)

- runs of $3 \cdot 10^{10}$ protons
- Two types of events observed:
  - Small clusters of events with errors up to a few tens (considered as SEUs, only during double DSP test)
  - Large clusters of thousands of events (SEFI) ⟹ self recovery
    - ~50k errors per SEFI -> 2ms
    - One SEFI per DSP -> not propagated to other DSPs
- Two design failures during the DSP TMR setup with a cross section of **$4.95 \cdot 10^{-12}$cm^2**

$$\sigma = \frac{\#errors}{N_{dsp} \times fluence}$$

setup	SEUs	SEFI	σ_{SEU}(cm^2/dsp)	σ_{SEFI}(cm^2/dsp)
DSP simple	-	9	-	**$1.04 \cdot 10^{-12}$**
DSP double	5	12	$8.6 \cdot 10^{-13}$	**$2.08 \cdot 10^{-12}$**
DSP TMR	-	5	-	**$3.87 \cdot 10^{-13}$**

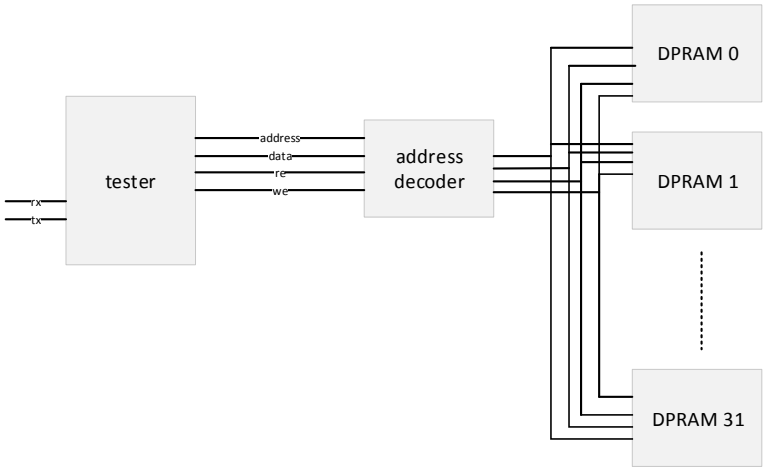
Irradiation Test Setup (DPRAM)

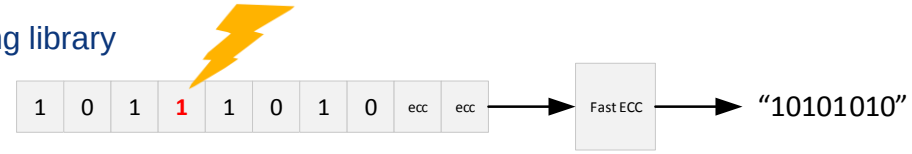
- The BRAM can be configured in three possible ways:
  - No ECC
  - Fast ECC: Error correction during the read operation, content remains erroneous
  - Slow ECC: Error correction during the read operation with write back to the array ⟹ PLL and wave form generator (WFG) is engaged to have this operation transparent
- ECC is Single Error Correction, Double Error Detection (SECDEC)
- All three setups were tested in static mode

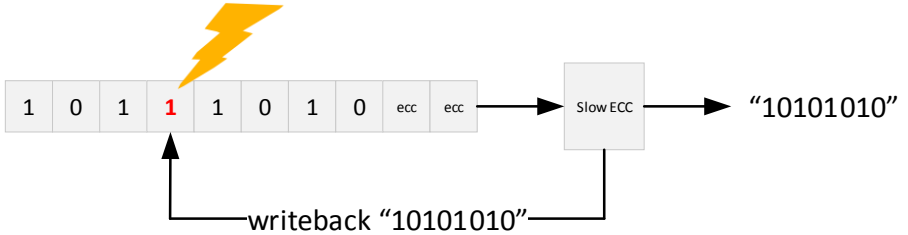
  (1) Write sequence prior irradiation to the entire array

  (2) Irradiate

  (3) Read Back/transmit wrong data along with address and block information
- Custom memory instantiation of 32 blocks (out of 56) using library component without automatic inference
  - Setup #1 -> Without EDAC uses 6144 x 8 bits per block
  - Setup #2 -> With EDAC Fast ECC 2048 x 18 bits per block
  - Setup #3 -> With EDAC Slow ECC 2048 x 18 bits per block







Experimental Results (DPRAM)

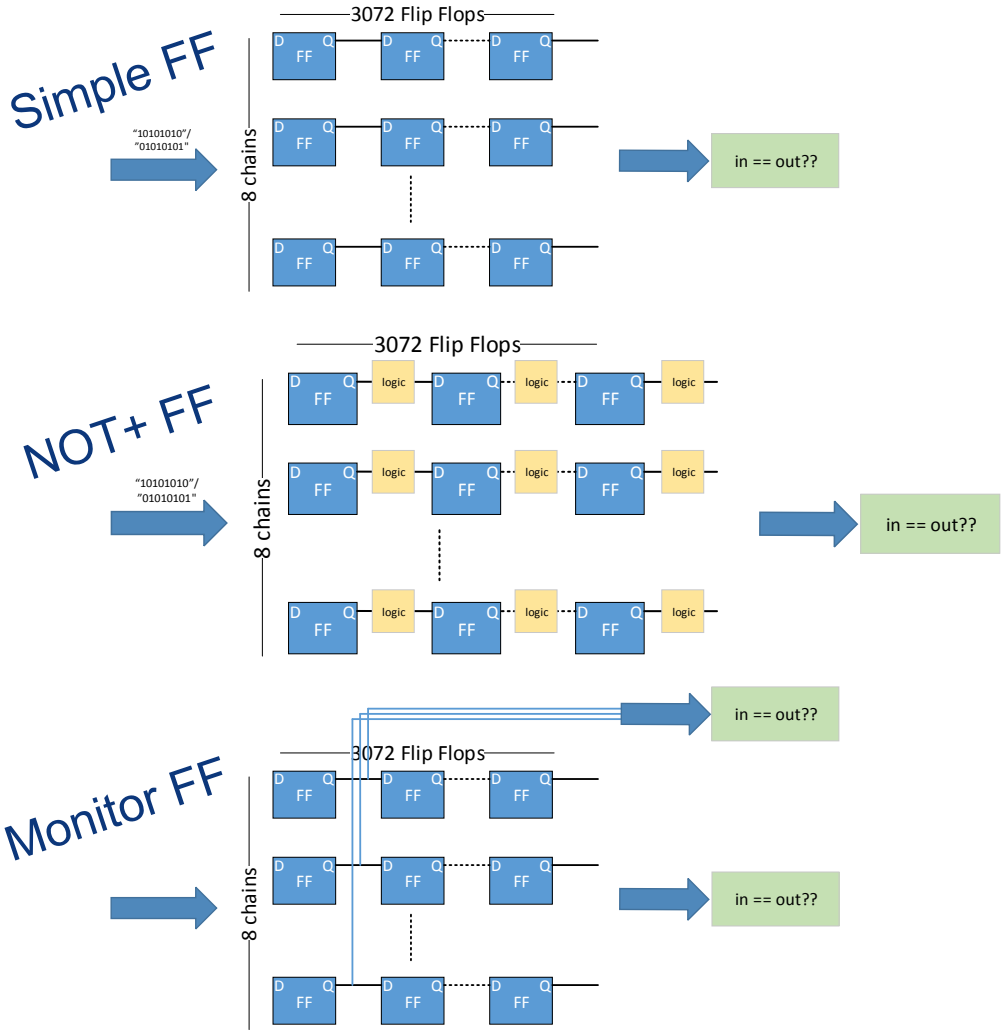
- 6 runs of $3 \cdot 10^{10}$ protons per run for the no ECC setup during June (device #1)
- 5 runs of $1 \cdot 10^{10}$ protons per run for the no ECC setup during October (device #2)
- 3 runs of $3 \cdot 10^{10}$ protons per run for the Fast ECC during July
- 5 runs of up to $1 \cdot 10^{11}$ protons per run for the Fast ECC during October
- 4 runs of $1 \cdot 10^{11}$ protons per run for the Slow ECC during October
- Homogeneous distribution of SEUs among the blocks
- Fast and Slow ECC demonstrated several SEUs and MBUs
- Slow ECC design experienced two failures during the tests

$$\sigma = \frac{\#errors}{N_{bits} \times fluence}$$

setup	SEUs	MBUs	σ_{SEU}(cm^2/bit)	σ_{MBU}(cm^2/bit)
no ECC June	17641	289	**$8.01 \cdot 10^{-14}$**	$1.31 \cdot 10^{-15}$
Fast ECC July	94	111	$8.85 \cdot 10^{-16}$	$1.04 \cdot 10^{-15}$
no ECC Oct	4872	9	**$6.13 \cdot 10^{-14}$**	$1.13 \cdot 10^{-16}$
Fast ECC Oct	773	1289	**$1.44 \cdot 10^{-15}$**	$2.41 \cdot 10^{-15}$
Slow ECC Oct	2907	1311	**$3.69 \cdot 10^{-15}$**	$1.66 \cdot 10^{-15}$

Irradiation Test Setup (FF)

- Flip Flop chains biased with a known pattern and monitored for any differences in their output
- 8 chains of 3072 flip flops each
- Three setups:
  - Setup #1 FF -> Only flip flops
  - Setup #2 FF -> 8 not gates interfered between every flip flop's input and the proceeding one's output ⟹ potential SET triggering
  - Setup #3 FF -> Only flip flops with a sampling point in the middle of the chains
- All chains are biased with an alternating pattern
- Results are compared at each clock cycle and transmitted to a control computer via UART in case of errors



Experimental Results (FF)

- 4 runs of $3 \cdot 10^{10}$ protons for the simple Flip Flop Setup in July
- 3 runs of $3 \cdot 10^{10}$ protons for the simple Flip Flop Setup in October
- 1 run of $1.72 \cdot 10^{11}$ protons for NOT gate interfered setup
- 3 runs of $3 \cdot 10^{10}$ protons for the double monitored Flip Flop Setup in October
- During the July runs, only in 1 out of four runs we experienced failures
- During the October runs, all setups had occurring errors, mainly SEFI events
- SEFIs were always occurring in one of the chains and are self recovered
- Double monitored setup showed that most failures occurred in the second half of the chain and it was as big as a few hundreds of events/clock-cycles, some times more than 1000 events/clock-cycles.
- NOT gate setup showed zero failures

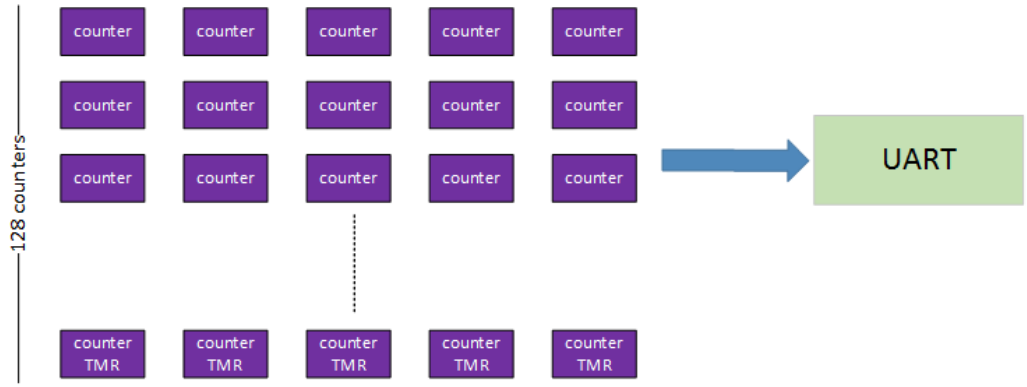
$$\sigma_{FF} = \frac{\#errors}{N_{bits} \times fluence}$$

$$\sigma = \frac{\#errors}{N_{chains} \times fluence}$$

setup	SEUs	SEFI	σ_{SEU}(cm^2/bit)	σ_{SEFI}(cm^2/chain)
Simple FF	1	3	$1.3 \cdot 10^{-15}$	$1.25 \cdot 10^{-11}$
NOT gate FF	0	0	$< 2.36 \cdot 10^{-16}$	$< 7.26 \cdot 10^{-13}$
Simple FF	3	20	$1.3 \cdot 10^{-15}$	$2.77 \cdot 10^{-11}$
Double Monitor FF	4	21	$1.7 \cdot 10^{-15}$	$2.9 \cdot 10^{-11}$

Irradiation Test Setup (Counter)

- 96 32-bit counters
- 32 TMRed 32-bit counters
- Each counter transmits its value every 5 seconds
- All counters are synchronized
- UART buffers are using Fast ECC scheme to avoid SEUs on the data
- CMIC engaged



Experimental Results (Counter)

- 3 runs of $3 \cdot 10^{10}$ protons
  - No errors found
- 3 runs of $1 \cdot 10^{11}$ protons
- In two runs we had one SEU per run, during the third run we lost the design
- 1 run of $3.09 \cdot 10^{12}$ protons (**1.8kGy**)
  - Several SEUs, 4 SEFIs two of which on the same counter, 2 of which to all counters.
  - 21 failures of the design -> they were recovered after re-sending the command via UART
  - 1 time needed to reprogram the FPGA for during 1.8kGy
  - TMRed counters also fail

$$\sigma = \frac{\#errors}{N_{counters} \times fluence}$$

setup	SEUs	SEFI	failures	σ_{SEU}(cm^2/bit)	σ_{SEFI}(cm^2)	σ_{fail}(cm^2)
Counter app	117	4	21	$2.62 \cdot 10^{-13}$	$1.15 \cdot 10^{-12}$	$6.79 \cdot 10^{-12}$

Conclusions and future Steps

- Up to 3kGy cumulative dose -> **no degradation**
- Results showed that this FPGA has a robust behavior
- Purchase of a significant lot of devices foreseen for the next year. The requests are collected by EN-SMM-RME (contact Salvatore.Danzeca@cern.ch)
- Training from NanoXplore to be scheduled between December and January!!!
- We need your feedback!

- Searching collaboration with the equipment groups to implement an application that will be tested at PSI

Thank you!

Questions???