512 channel Detector readout with VMM-SRS
&
VMM and the SRS - update

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Michael Lupberger (CERN)

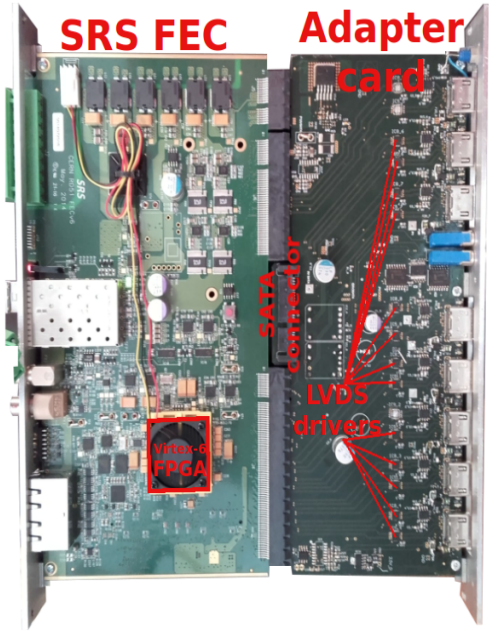
Outline

Michael:

- Available hardware
- Firmware
- VMM hybrid as trigger
- Measurements/Test

Dorothea:

Current status of hardware



Adapter Card

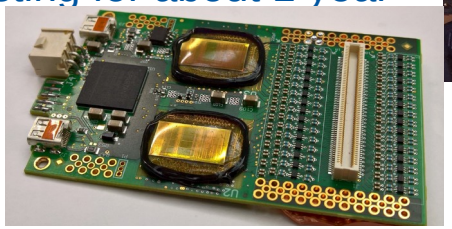
1+3 older versions working → increased number of cards & channels

PCB design of final version ongoing, schematics completed
→ PCB layout highest priority for Hans

Hybrids

Some VMM2 hybrids → not used any longer

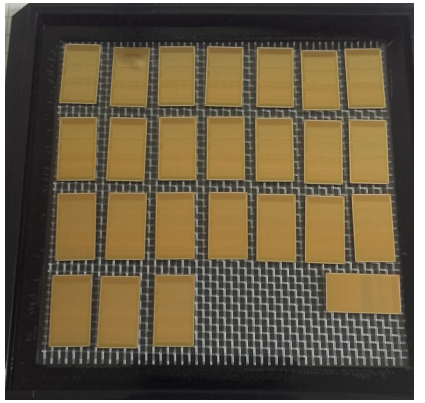
4 first VMM3 prototype hybrids died after intense testing for about 1 year



3 VMM3 prototype hybrids (not final version)

1 VMM3a prototype hybrid (not final version)

4 VMM3a final hybrids bonded/equipped at CERN



24 VMM3a final hybrids sent to company for mass production test

→ first 2 back, tested, working fine since October
→ Others arrived, with Hans for mounting cooling

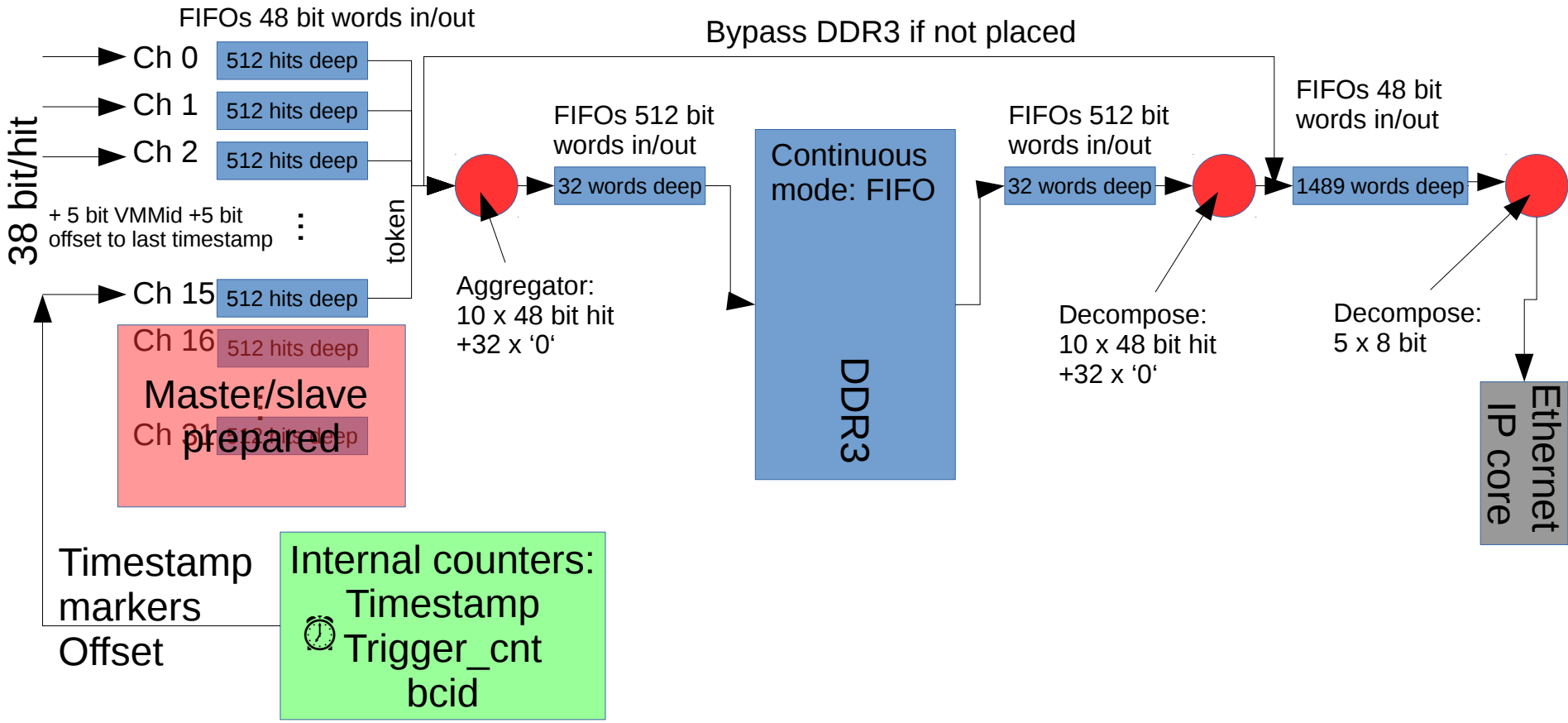
30 VMM3a ASICs left, possibly about 100 more from Vinnie soon

Wafers ordered with ATLAS production

FEC firmware (Yan's project)

External trigger mode

Idea/challenge: use same data path in FEC FPGA as in continuous mode



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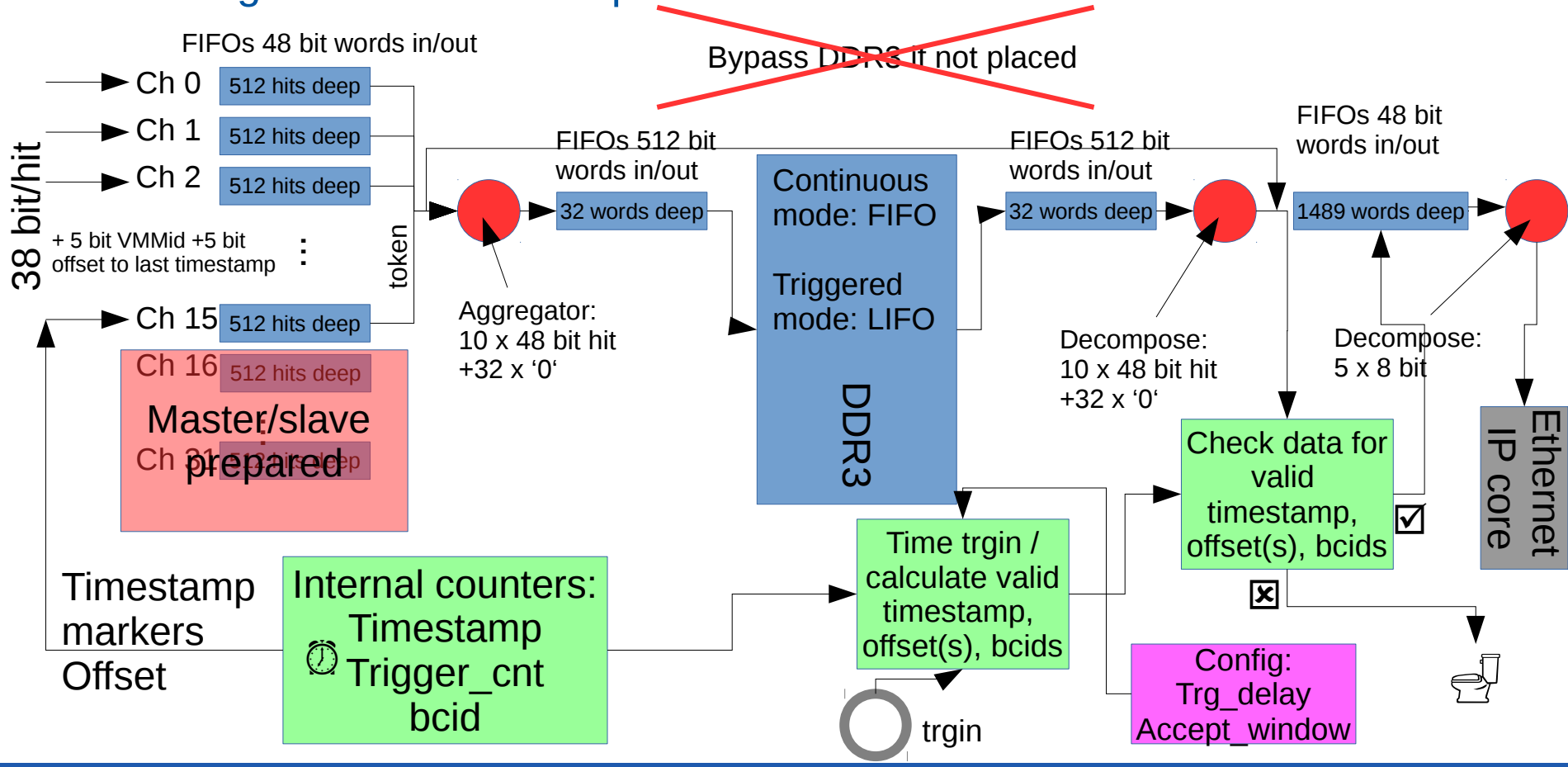


VMM Address in RealTime (ART)

VMM3a manual:

Each VMM provides, at a single dedicated digital output, art, the address of the first on-chip above-threshold event, called address in real time (ART). The system, thus, is equivalent to a trigger system with segmentation …

The ART latency is the sum of several delays

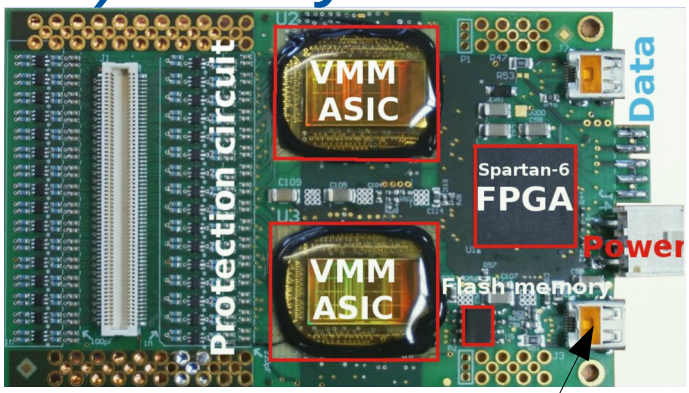
1. Time from instantaneous charge event to 1% of the peak is $\sim 10\,\text{ns}$
2. Time from pulse peak to peak found $\sim 5\,\text{ns}$
3. Digital latency from comparator firing to leading edge of ART is $\sim 5\,\text{ns}$
4. Digital latency from peak found to leading edge of ART is $\sim 5\,\text{ns}$

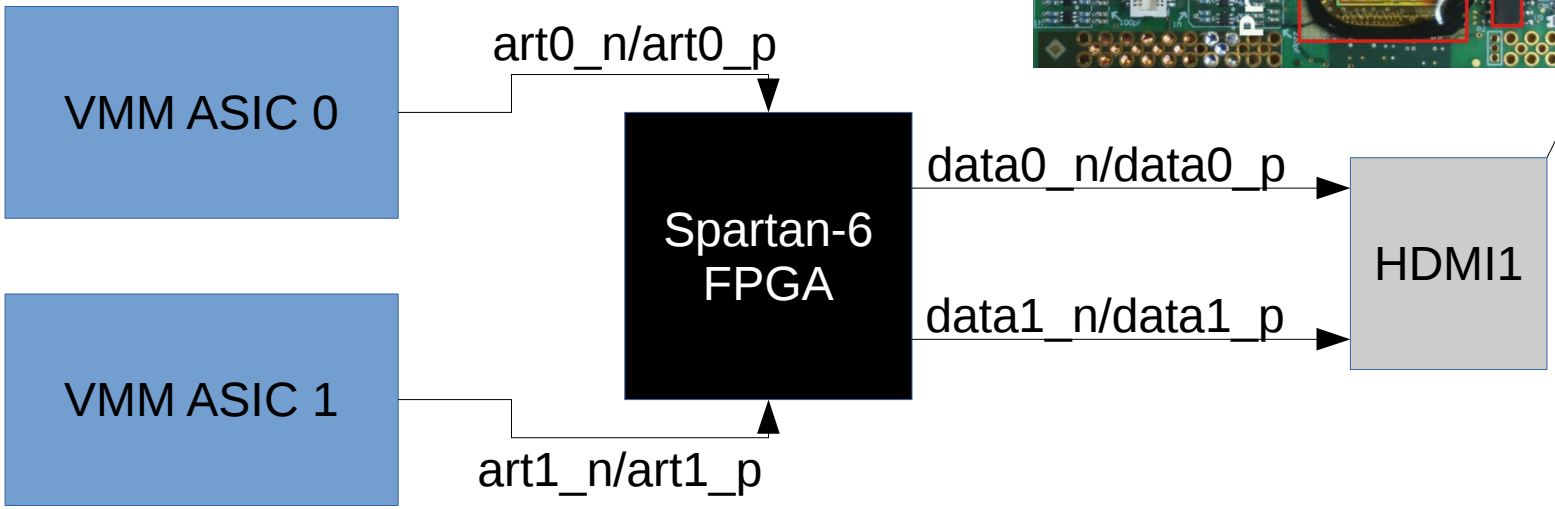
Or $\sim 15\,\text{ns}$ for the threshold crossing option or $\sim 20\,\text{ns}$ + peaking time if the peak detect is chosen. The above assumes a typical case of input capacitance of 200 pF and a load of 20 pF at the digital output.

→ fast logic signal 15 ns after first hit on one of the 64 channels, followed by the 6 bit channel address and synchronised to a 160 MHz clock.

VMM Address in RealTime (ART) on hybrid

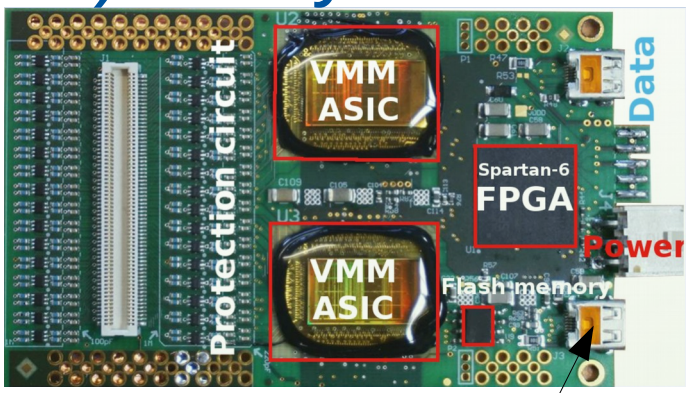
Treatment of differential art signals from VMMs - hardware

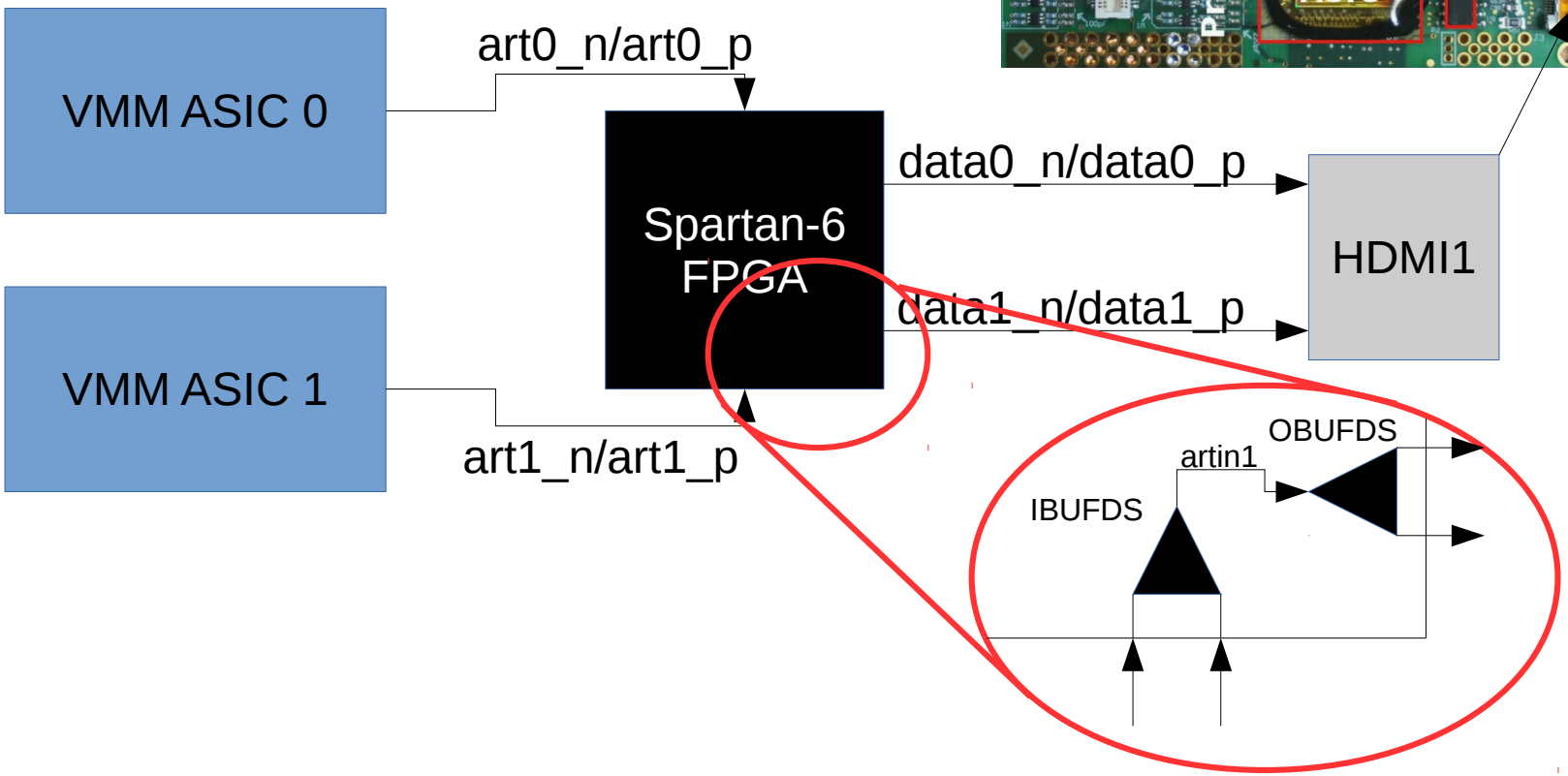




VMM Address in RealTime (ART) on hybrid

Treatment of differential art signals from VMMs - firmware

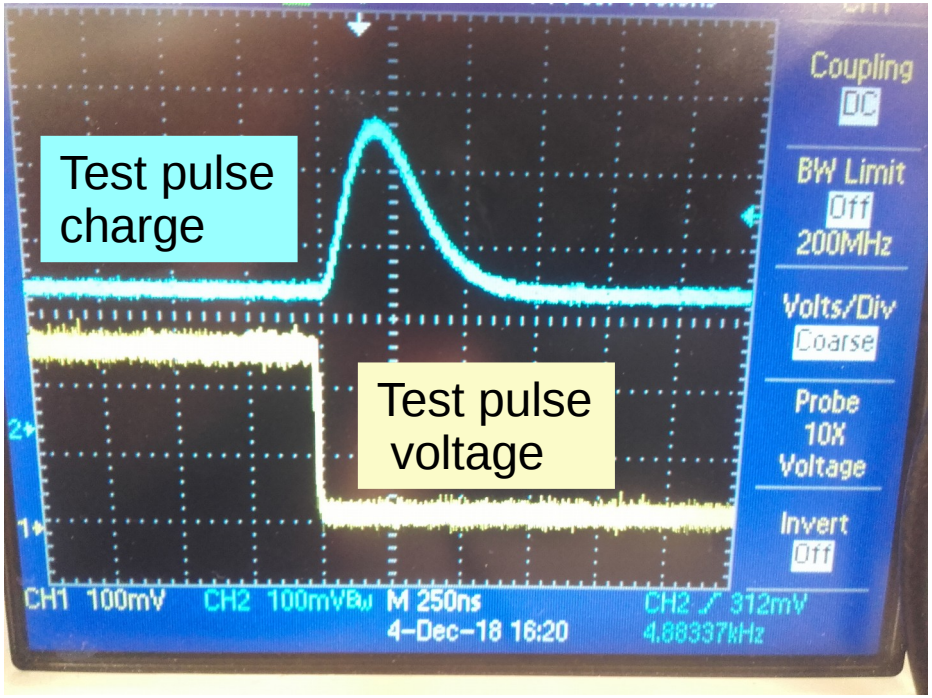


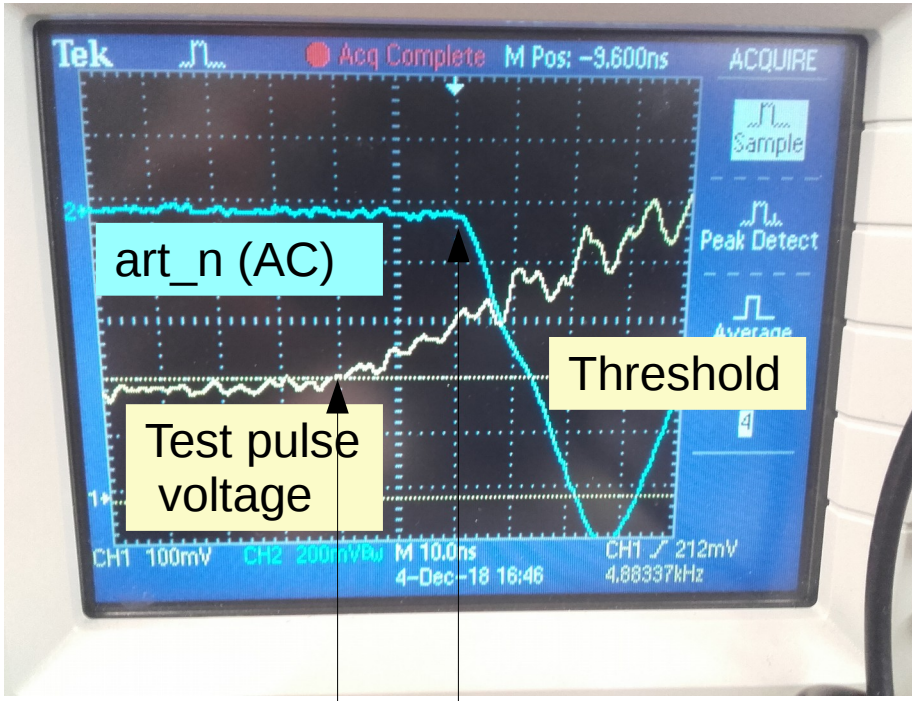


VMM Address in RealTime (ART) on hybrid

→ direct routing – no treatment ⇒ can be used for triggering

Quick test (200 MHz Oszi for 160 MHz ART clock not good enough)

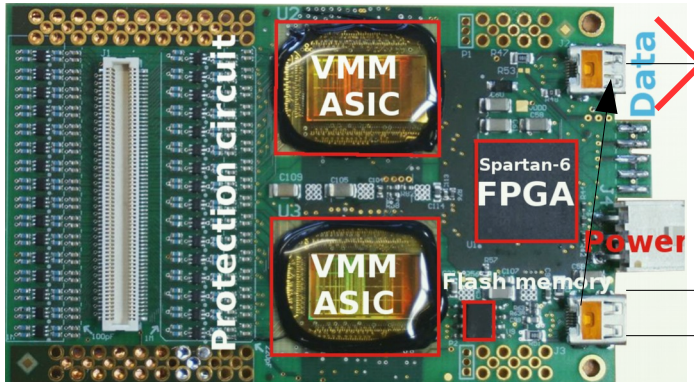




THL crossing 20 ns art logic start

VMM Address in RealTime (ART) on hybrid

→ direct routing – no treatment ⇒ can be used for triggering
What to do with it?



Not possible to route to FEC via data HDMI

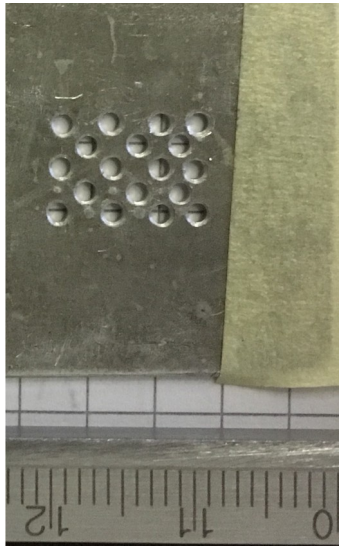
ART trigger 0
ART trigger 1
?

Possibilities:

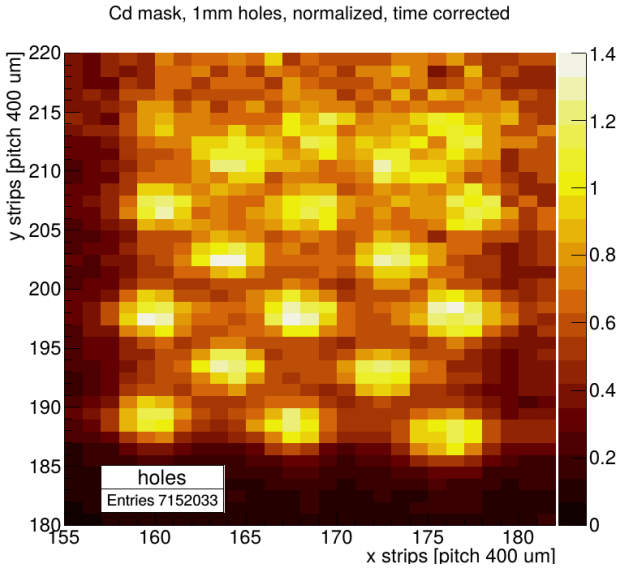
- Convert to LEMO and go to NIM Logic
- Design SRS trigger module (FPGA with simple interface e.g. Labview user configurable trigger as Wiener NIMBox)
- Route to FEC through Powerbox with second HDMI cable → user selection:
  - Master/Slave mode
  - Provide trigger

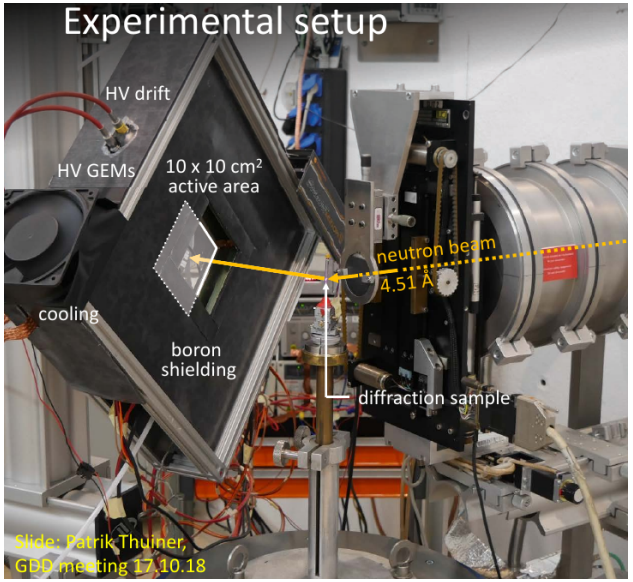
Test beams

Cadmium mask, 1 mm holes



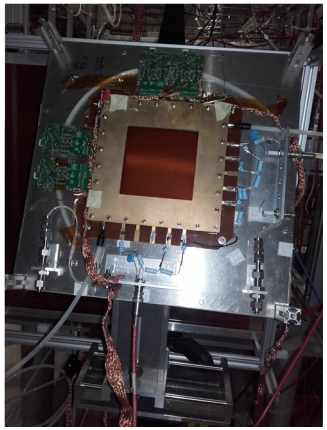
Reconstructed neutron hits

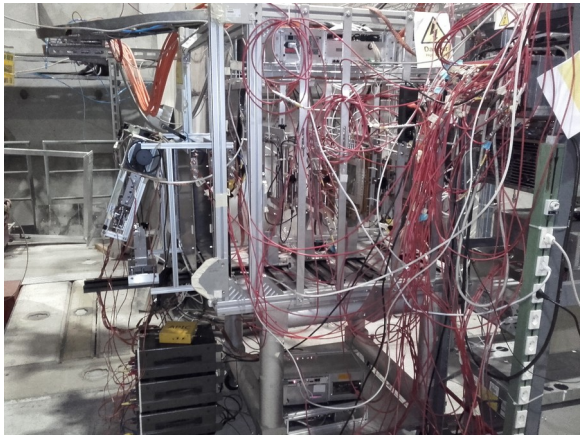




Oct 2018 (ILL): 4 VMM3a hybrids

July 2018 (Neutrons@Wigner): 3 VMM3 + 1 VMM3a hybrids





August 2018 (SPS): 3 VMM3 + 1 VMM3a hybrids, GBAR proto

Oct 2018 (SPS): 3 VMM3 + 7 VMM3a hybrids
2 FECs, 1 CTF, GEM telescope with 3 stations

Test beams

Nov 2018: Bonn with AC coupled segmented GEMs (2x VMM3)
Nov 2018: Mainz (2x VMM3a) 3-GEM detector in Lab and e beam
→ see Stefano's talk

Lab tests with Fe55

Online monitoring →
Gain 4.5 mV/fC
Peaking time 200 ns
Neighbouring logic on