SAMPA frontend for SRS

A Short Overview of SAMPA chip
Specification & Functionalities
Planning for a SAMPA frontend in the SRS ecosystem

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The SAMPA ASIC, where it came from

During Run3 ALICE needs to operate at higher rate, recording all MB events

Goal: 50kHz in Pb-Pb (~10nb^{-1} in Run3 and Run4)

Upgrade detectors and electronics during Long Shutdown 2 ("now"-2020)

➢ Time Projection Chamber (TPC)

- GEM readout plane, high rate capability, continuous readout.

TPC electronics used till ``past week" was not made to amplify negative charge input (as GEMs provides) and cannot cope with the higher rate and with the continuous readout operation planned

➢ Muon Chamber (Forward muon spectrometer)

- Higher rate capability, new acquisition electronics chain in ALICE

new electronics needed, too

TPC required a new readout, MCH too.

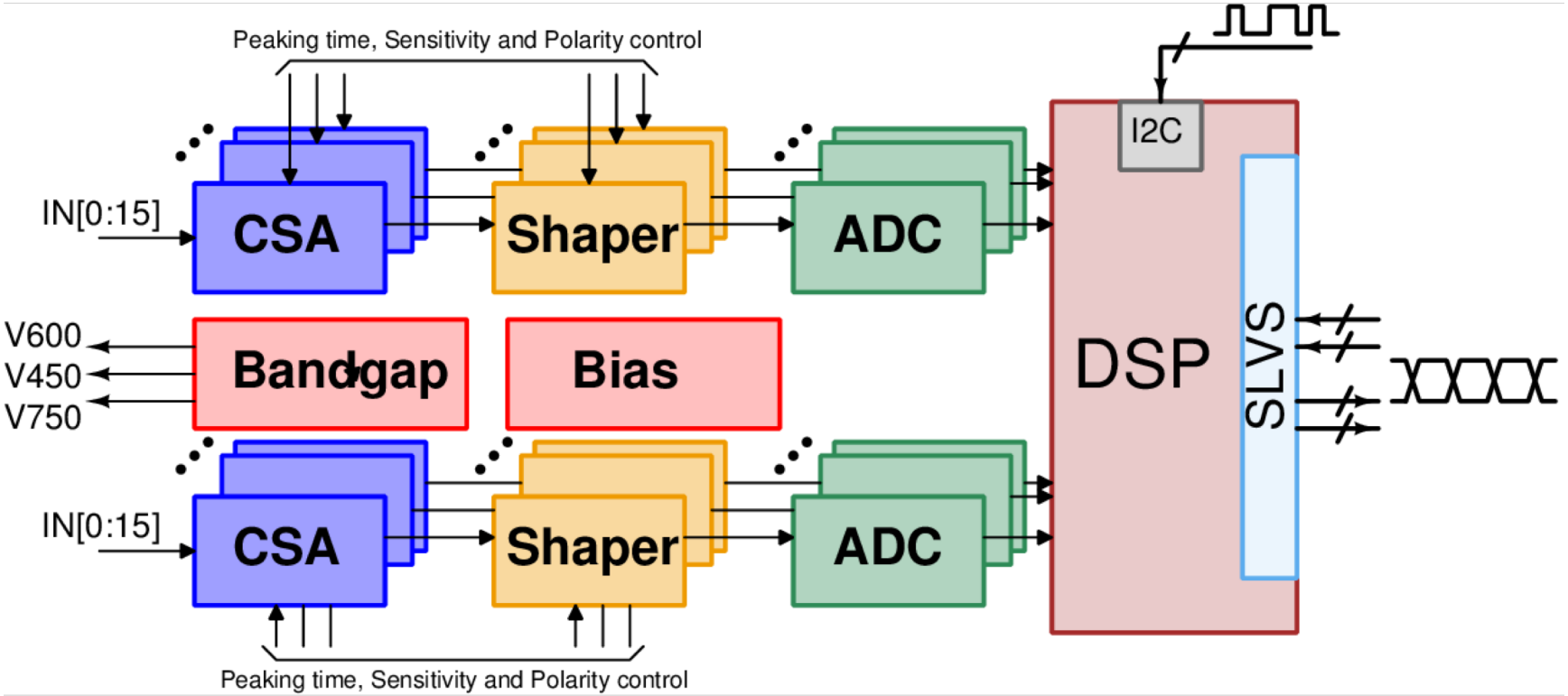
A common project to design a new ASIC: <u>SAMPA</u>

SAMPA Design Specifications Summary

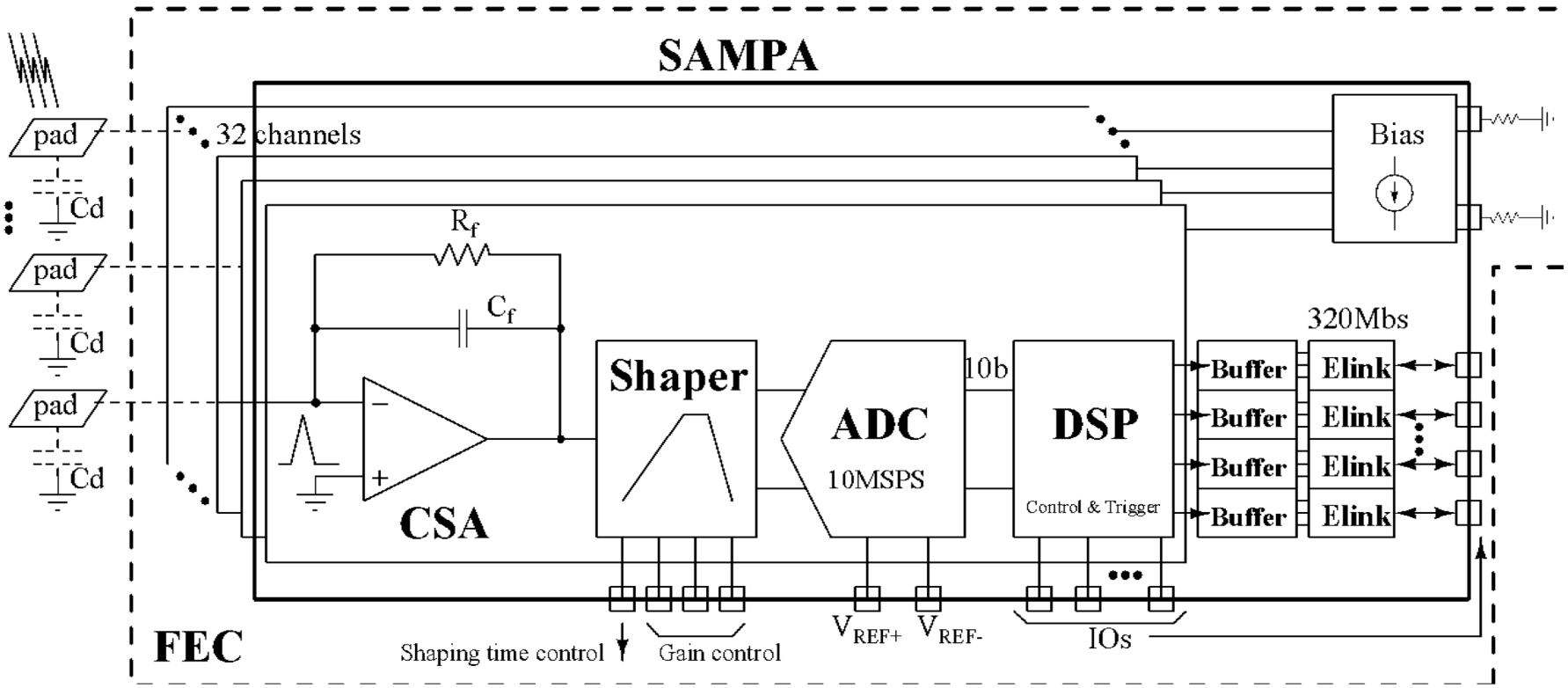
- TSMC CMOS 130 nm, 1.25V technology
- 32 channels, Front-end + ADC + DSP
- package size ≤15x15mm^2 (total footprint)
- ADC: 10-bit resolution, 10MS/s, ENOB>9.2
  (Alice TPC is eventually using: 5MS/s, to keep BW requirement in the readout chain lower)
- DSP functions: pedestal removal, baseline shift corrections, zero-suppression
- Data transmission: up to 11 e-link at 320 Mbps to GBTx, SLVS I/O
- Power < 32 mW/channel (Front End + ADC)

TPC Mode	MCH Mode
▪ Negative Input charge ▪ Sensor capacitance: 12 – 25 pF ▪ Sensitivity: 20mV/fC & 30mV/fC ▪ Noise: ENC ≤ 580 e^- @ 18.5pF ▪ Peaking time: ~160 ns ▪ Baseline return: <500 ns	▪ Positive input charge ▪ Sensor capacitance: 40–80 pF ▪ Sensitivity: 4mV/fC ▪ Noise: ENC ≤ 950 e- @ 40pF 1600 e- @80pF ▪ Peaking time: ~300 ns ▪ Baseline return: <550 ns

SAMPA Block Diagram



SAMPA Block Diagram



Functionalities overview

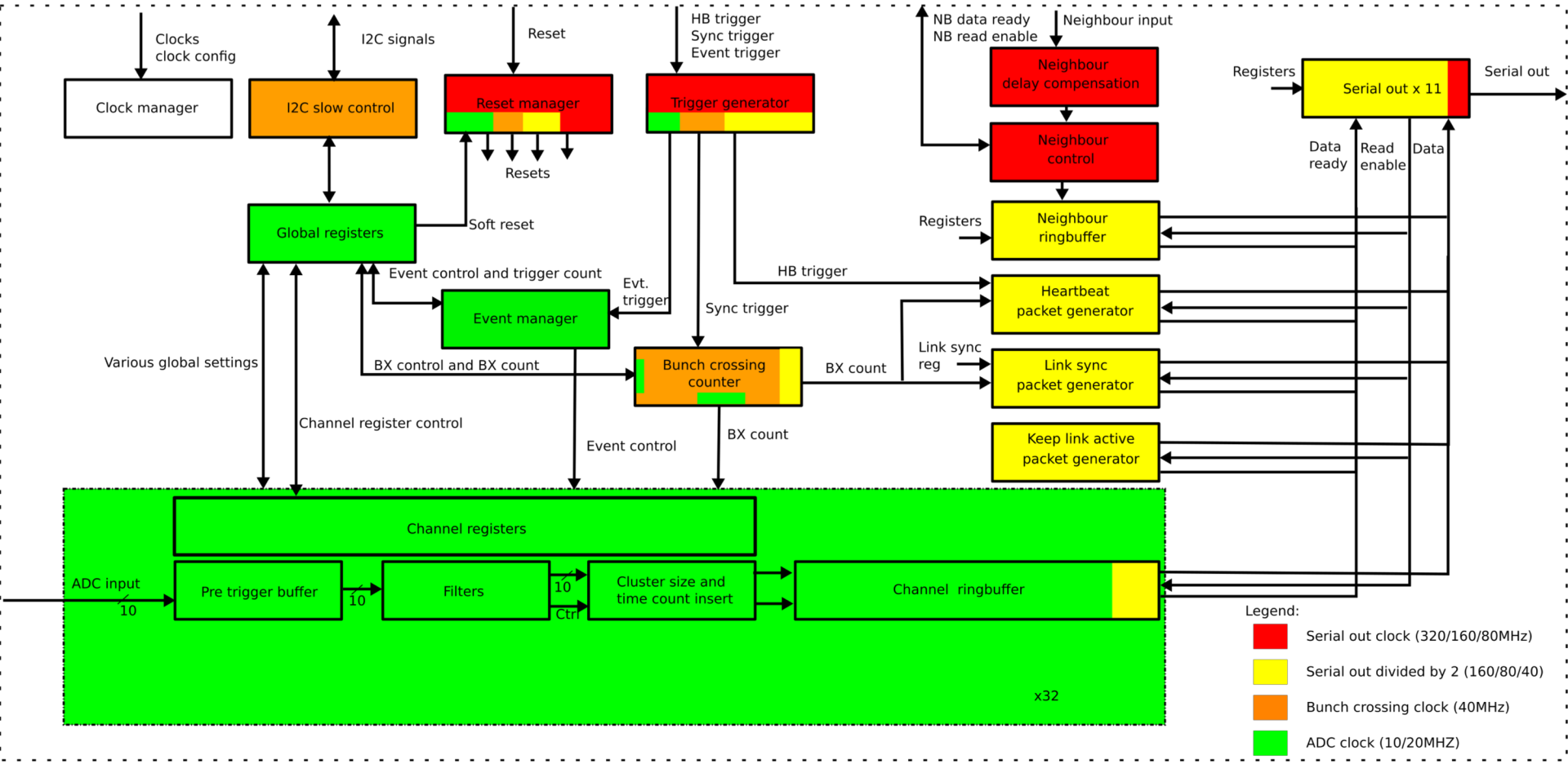
DSP

Top Level Functionality

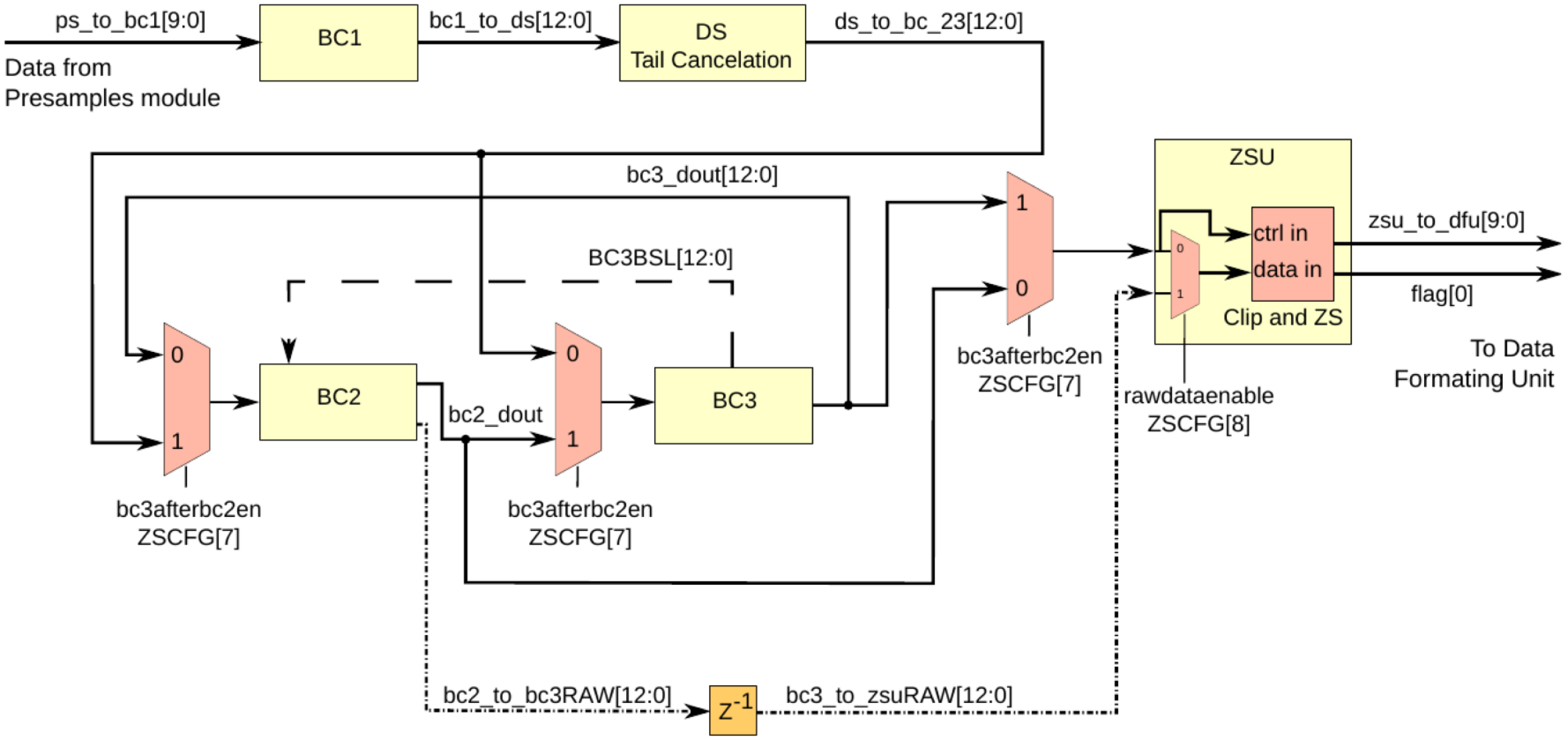
- 4 primary filter blocks
  - Individual correction per channel
  - Baseline correction
    - 1 FIR filter
    - 1 Slope based filter
    - 1 IIR filter
    - Lookup table correction(Pedestal Memory) f(t);f(din)
    - Conversion f(din)
    - Fixed correction
  - Tail cancellation
    - 1 IIR filter

SAMPA Digital Block Diagram

SAMPA block diagram



SAMPA Digital Filters Block Diagram



Top Level Functionality

- Compression
  - Zero suppression with run length encoding
    - Forward linked list for easier decoding
  - Cluster sum
    - Uses zero suppression with run length encoding , but sums cluster into 20bit word
  - Huffman
    - Differential encoded data
    - Programmable table of codes for +17 to -17
    - Values outside table have special Huffman code prepended to raw 10bit value

Top Level Functionality

- Configuration
  - Configurable through I2C
  - 1 global register unit, 32 sets of channel registers
- Design for test
  - JTAG boundary scan
  - Built in memory tester
  - Scan chain (on >98% of digital block flops)
- Radiation tolerant
  - TMR on almost all flip-flops
    - except on part of data path
  - Hamming protected headers

Readout

- Selectable number of serial links up to 11
  - 320/160/80Mbps
  - Channels divided among links, no load sharing
  - Which channel goes to which link and in which order can be selected
  - Data is packet based (header + payload)
    - One packet per channel per event
- Event modes
  - Triggered
  - Continuous
  - Selectable event length up to 1024 samples
  - 192 pre-trigger samples

Readout

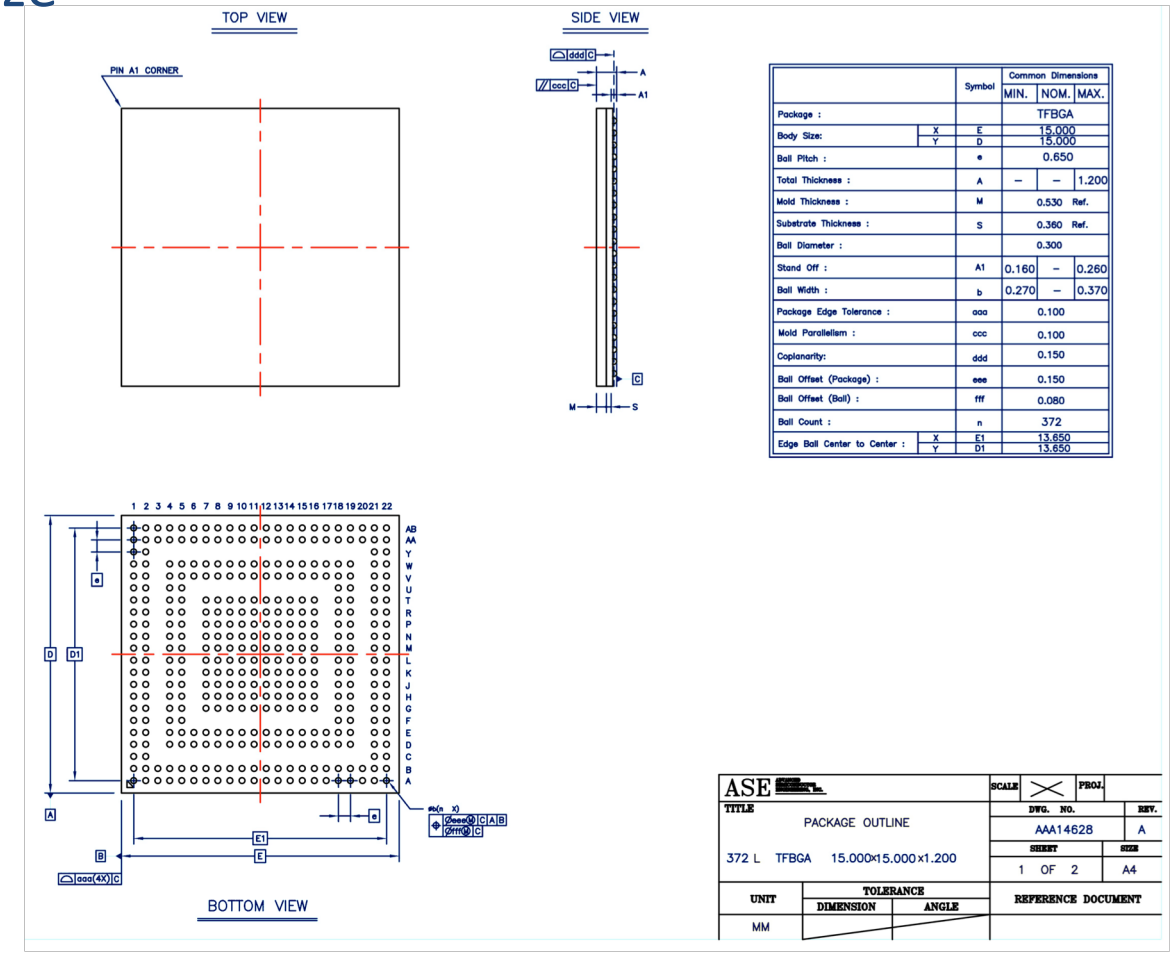
- Event buffer per channel
  - 6144(6K) words of compressed samples
  - 256 words of headers
  - Header still created if data memory goes full
- Daisy chain
  - Multiple devices can share a single serial link to readout unit
  - 2K word buffer in the receiving side

Readout

- Direct ADC serialization
  - –Data serialized directly from ADC at 32xADC speed over 10 links
  - –Raw data, no filtering, no headers
  - –Sync pattern on startup, receiver should maintain sync after that
  - –2 modes
    - •10 bits is sent consecutively for channel 0-31 each 32xADC cycle
    - •5 lower bits, then 5 higher bits consecutively for channel 0-15 is sent on link 0-4 and for channel 16-31 on link 5-9
  - –Clockgate the rest of the system to save power

SAMPA Package

- TFBGA package
- 15 mm x 15 mm body size
- 1.2 mm thickness
- 0.65 mm ball pitch.
- 372 balls
  - 4-substrate layers



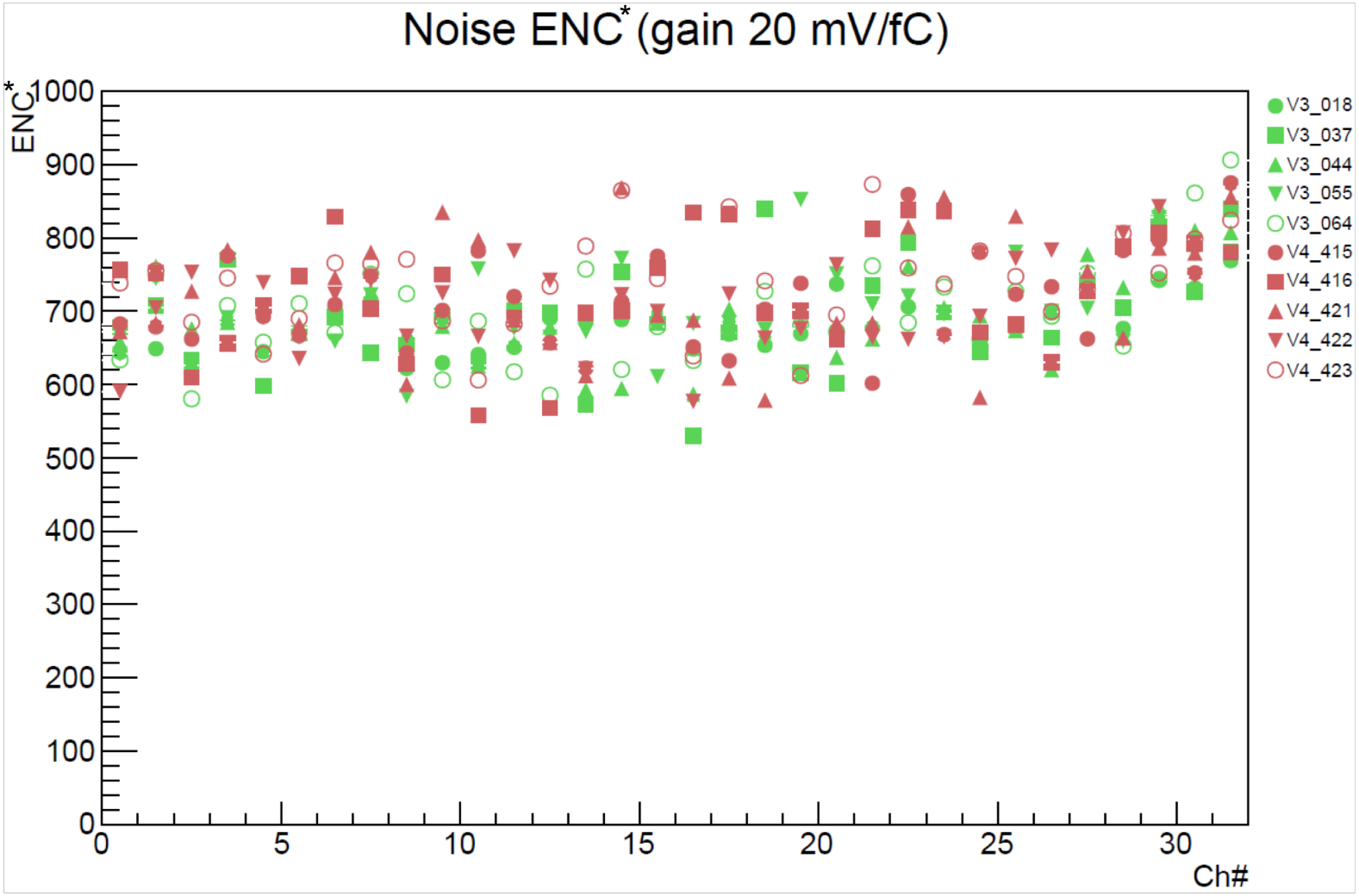
		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :				TFBGA	
Body Size:	X	E		15.000	
	Y	D		15.000	
Ball Pitch :		e		0.650	
Total Thickness :		A	–	–	1.200
Mold Thickness :		M		0.530 Ref.	
Substrate Thickness :		S		0.360 Ref.	
Ball Diameter :				0.300	
Stand Off :		A1	0.160	–	0.260
Ball Width :		b	0.270	–	0.370
Package Edge Tolerance :		aaa		0.100	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.150	
Ball Offset (Package) :		eee		0.150	
Ball Offset (Ball) :		fff		0.080	
Ball Count :		n		372	
Edge Ball Center to Center :	X	E1		13.650	
	Y	D1		13.650	

Performance

Some results from SAMPA qualification

Noise

Noise
(example of inside chip distribution)



*) ENC calculated using nominal FE gain (20mV/fC) and nominal ADC conversion factor (2.15 mV/ADU)

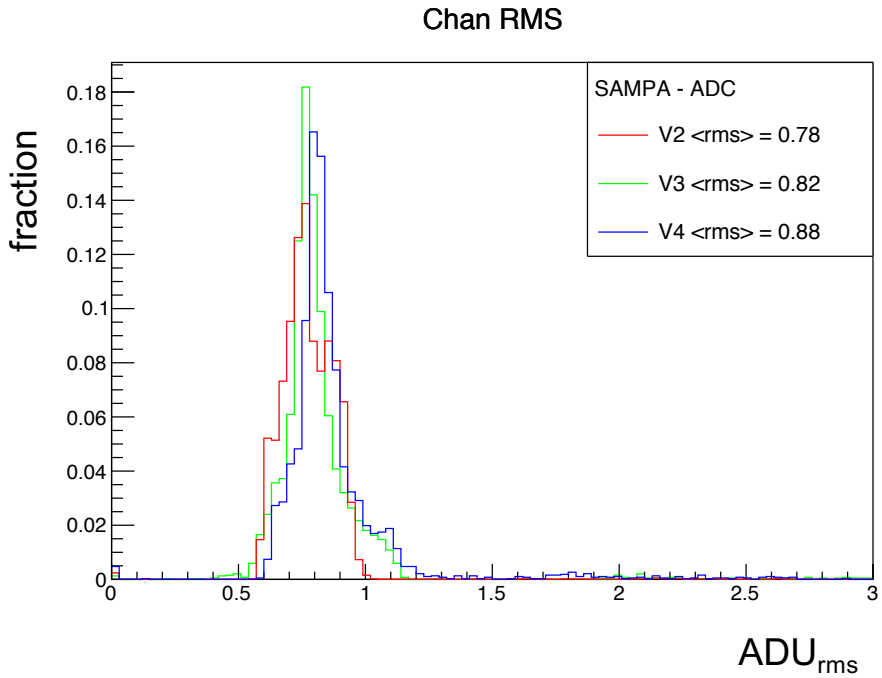
Noise (many chips)

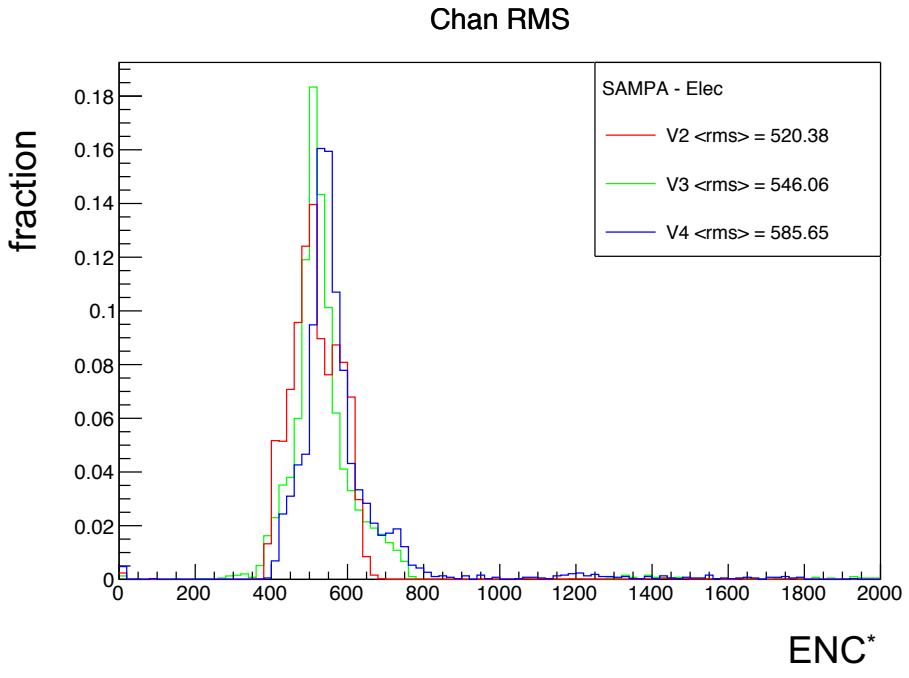
Experimental conditions:

C_{det}=0 (no added capacitance on the CSA input)

R_s=0 (external ESD-protection series resistor not present)

20N160





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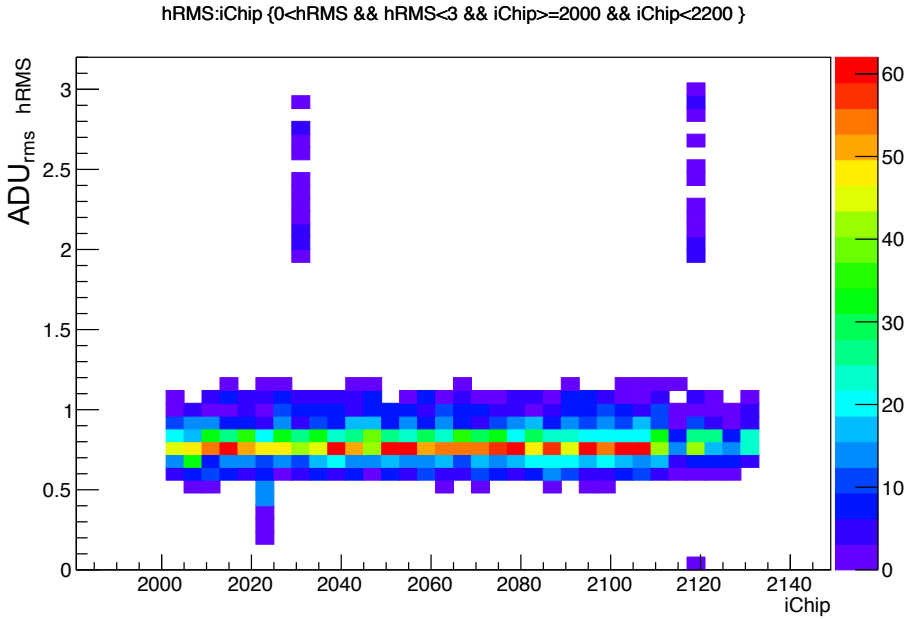
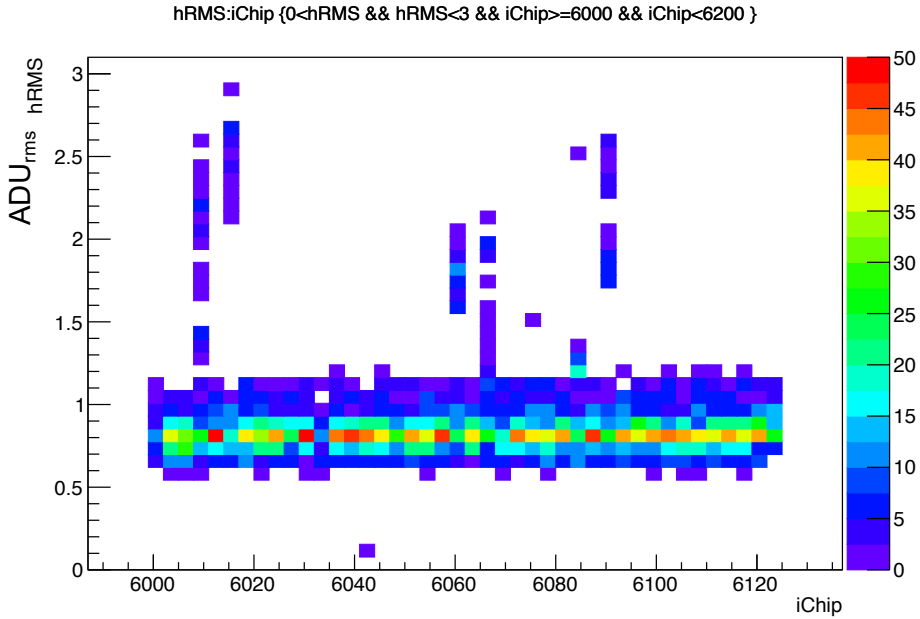
Noise (many chips)

20N160

V3



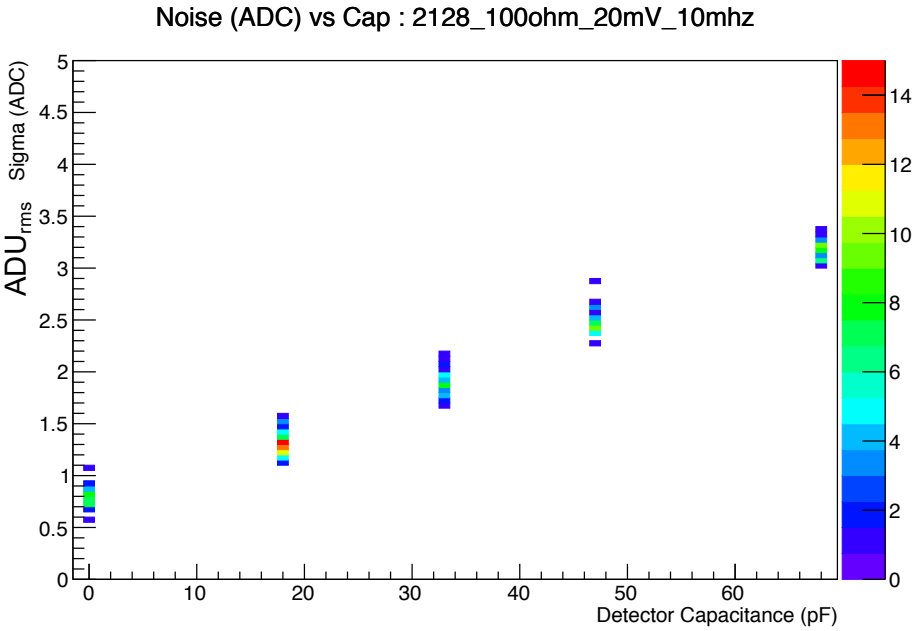
V4

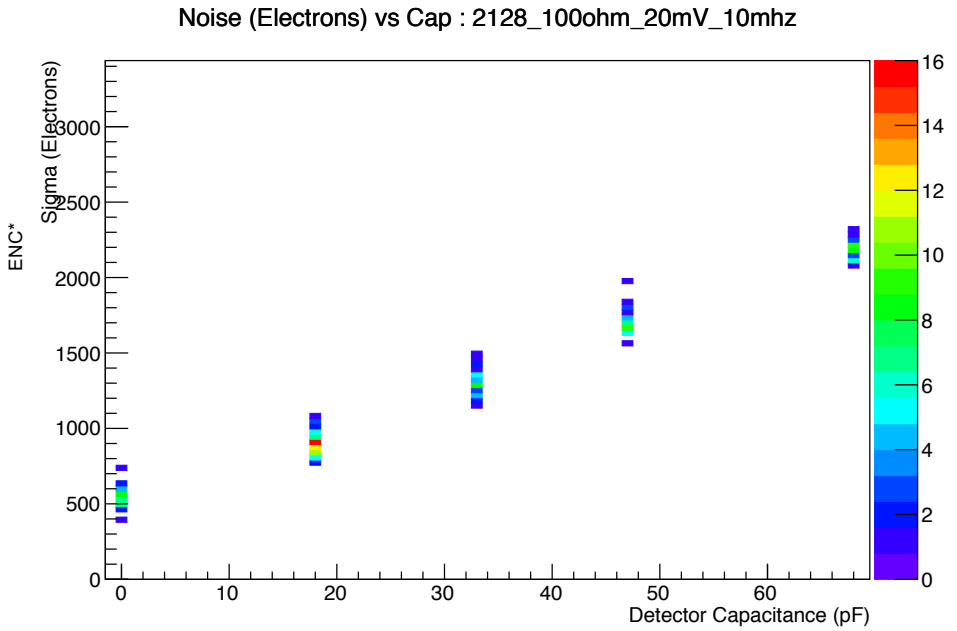


Noise vs C_{det} (V3, 20N160)

Experimental conditions:
C_{det} scan
R_s=100Ω

20N160, chip V3 #2128



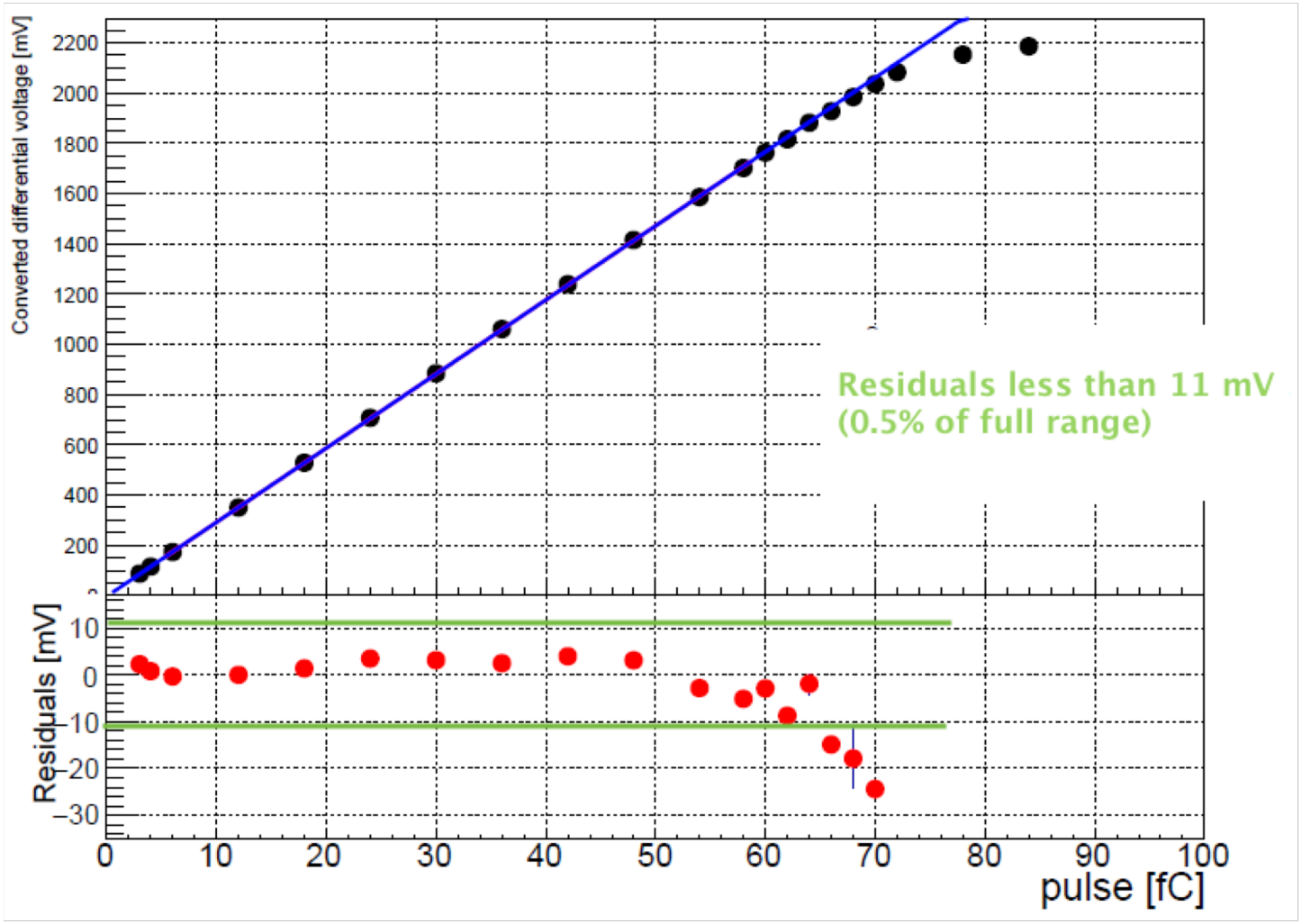


*) ENC calculated using nominal FE gain (20mV/fC) and nominal ADC conversion factor (2.15 mV/ADU)

Sensitivity (gain)

Linearity and Residual – an example

30N160



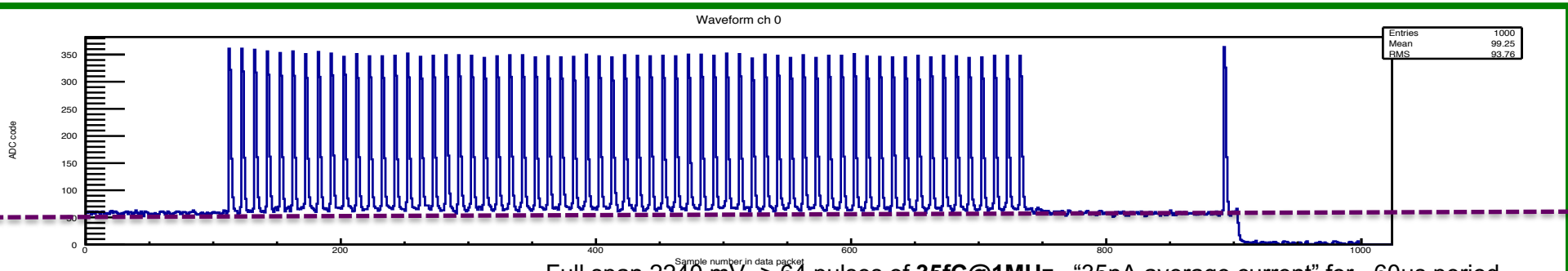
Linearity range, overview

- A calibration curve was performed for all channels of several chips
- The residuals* are very small (<10mV), for all channels, for a consistent part of the operational range:
  - 20N160: until ~95 fC ⇔ 1900 mV (>85% of the full range)
  - 30N160: until ~63 fC ⇔ 1900 mV (>85% of the full range)
  - 4P300: until ~480 fC ⇔ 1900mV (>85% of the full range)

* The curve used to calculate the residuals is the result of a linear fit in the central range (~15%-75%)

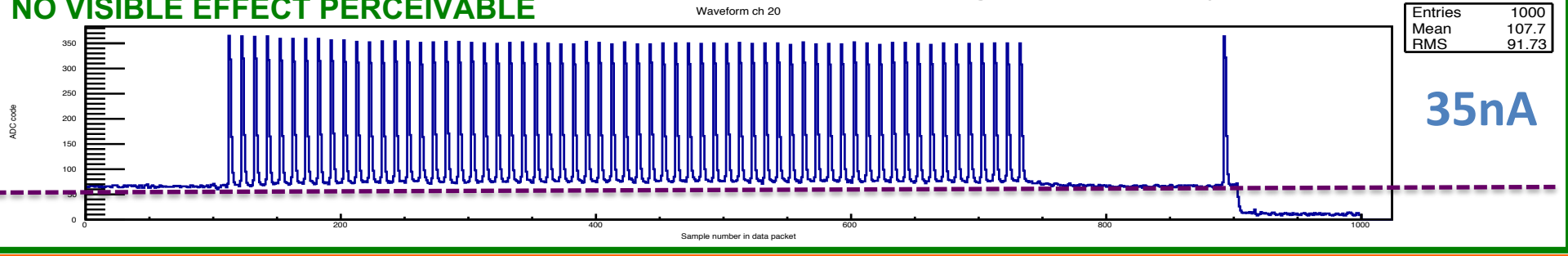
CSA robustness against Pile Up in SAMPA V4

Pile-up testing of a V4 chip

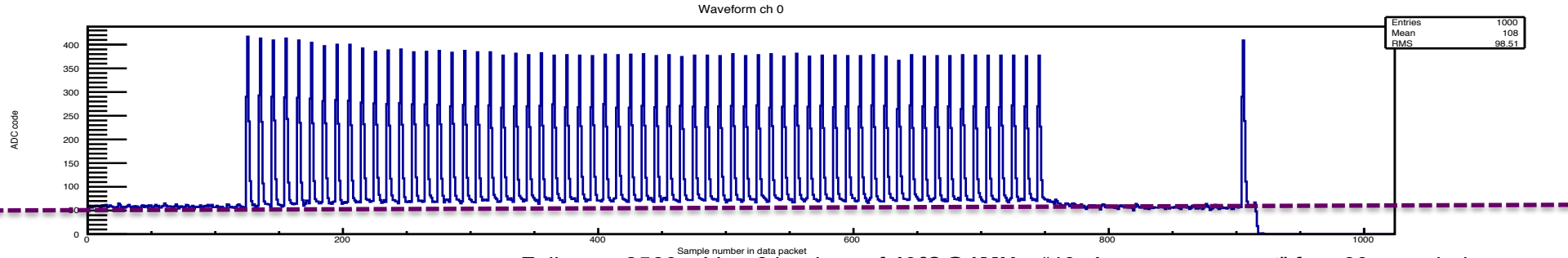


Full span 2240 mV -> 64 pulses of **35fC@1MHz**, “35nA average current” for ~60µs period

NO VISIBLE EFFECT PERCEIVABLE

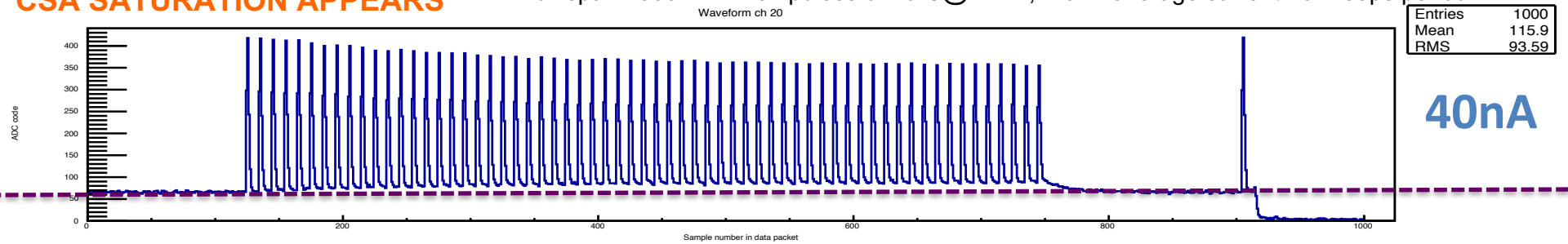


35nA



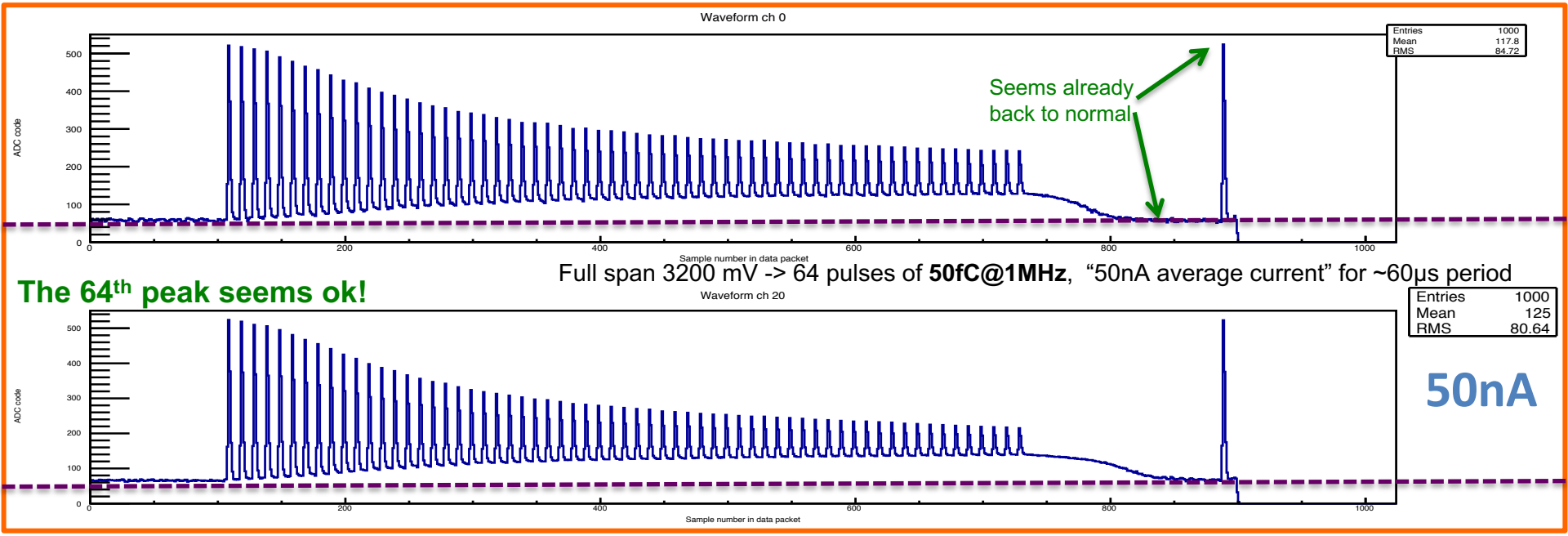
CSA SATURATION APPEARS

Full span 2560 mV -> 64 pulses of **40fC@1MHz**, “40nA average current” for ~60µs period



40nA

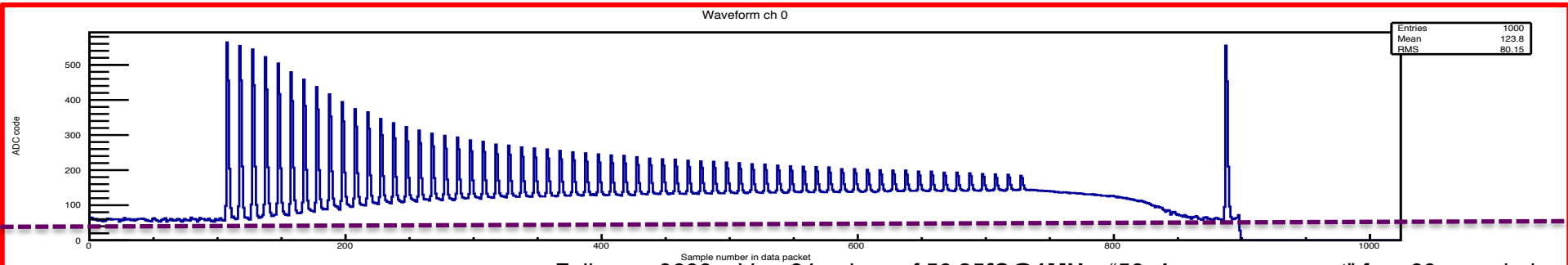
Going on: now really stressing a V4 chip



Full span 3200 mV -> 64 pulses of **50fC@1MHz**, "50nA average current" for ~60µs period

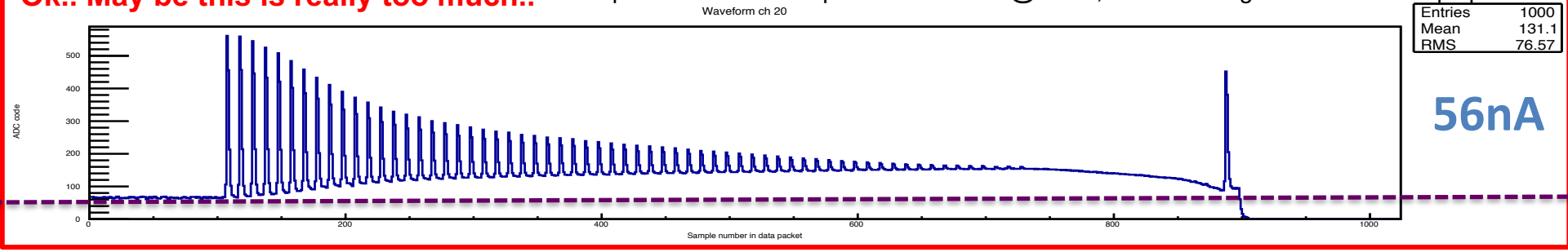
The 64th peak seems ok!

50nA



Ok.. May be this is really too much..

Full span 3600 mV -> 64 pulses of **56.25fC@1MHz**, "56nA average current" for ~60µs period



56nA

SAMPA chip overview summary

- SAMPA design was ALICE TPC/MCH driven, nevertheless design quite general:
  - ASIC for gas detector readout (either “GEM-like”, electron collection) or “MWPC-like” (induced charge collection)
  - 4/20/30 mV/fC gain (500/100/66 fC range) provided
  - Digitalization @10MS/s [improved version @20MS/s under study]
- Several readout options available by the embedded DSP:
  - “raw data” (DSP-bypassed, no trigger, continuous read-out)
  - Continuous or triggered readout, framed data (DSP)
    - Filters available for baseline correction
    - Either ZeroSuppression or Huffman coding for data reduction
    - Possibility of Cluster_sum output and DaisyChain
- I/O via I2C (settings) and up to eleven 320Mbps LVDS links

Why SAMPA frontend for SRS

- SAMPA design was ALICE TPC/MCH driven, nevertheless design quite general:
- Several readout options available by the embedded DSP:
- I/O via I2C (settings) and up to eleven 320Mbps LVDS links

SAMPA ASIC is working and available.

It was designed for gaseous (GEM / MWPC) detector readout

Likely of interest also outside ALICE/LHC community

We feel that it does make sense to integrate it on SRS

Our group directly interested in having such a system working to be used in local activities

Our Planning for a SRS frontend

- SAMPA designed locally, good knowledge, quick and full access to the original designers (important here, the digital ones)
- Two mains challenges
  1. Firmware for the FPGA linking SAMPA to SRS backend
  2. Design of high density, multilayer, low crosstalk (analog & analog-digital), etc., board to host 4 SAMPAs (to provide 128chs hybrid)
- First steps
  - Study both in simulations and with an assembly "SAMPA_testboard" <-> "FPGA developing board" the coupling and the comunication btw SAMPA and target FPGA (w/o hybrid)
  - Start already design of hybrid board

FPGA firmware engineer already contracted;

Board design specialist candidate being evaluated right now.

QUESTIONS?

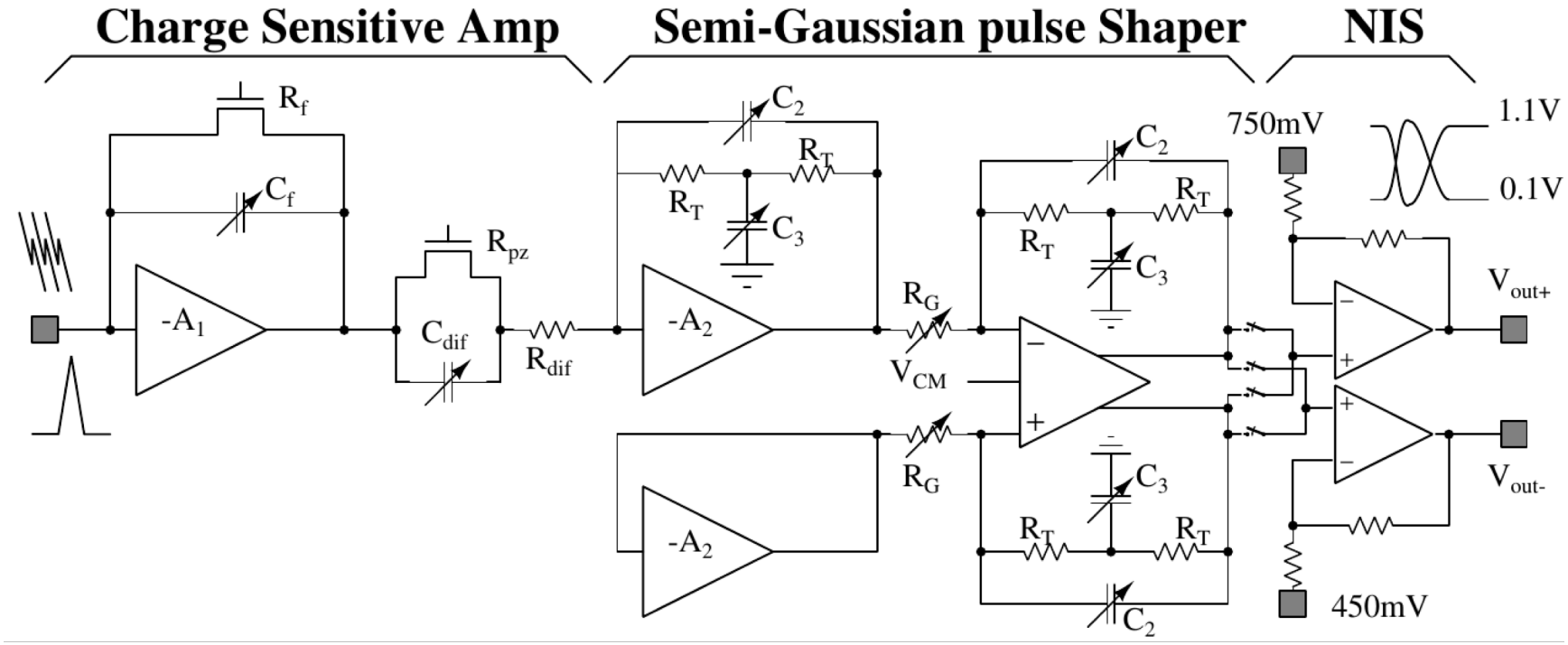
COMMENTS?

SUGGESTIONS?

More informations

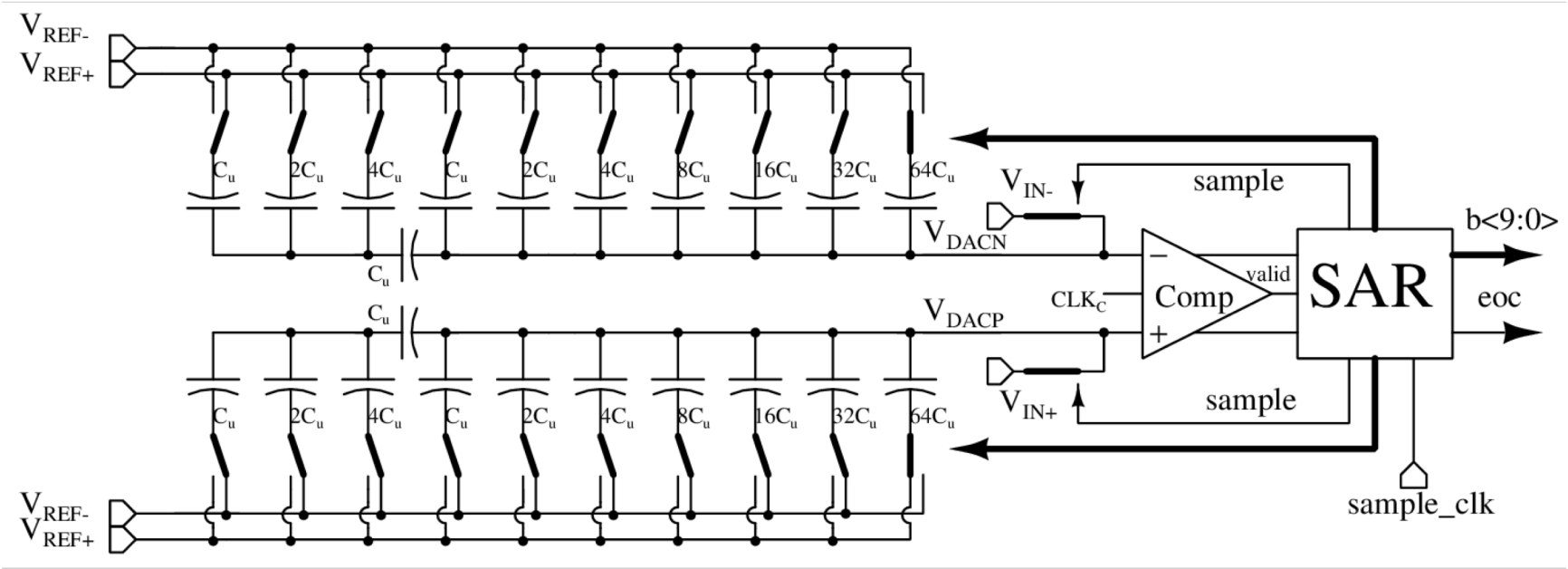
BackUp Slides

SAMPA V3: CSA + Shaper

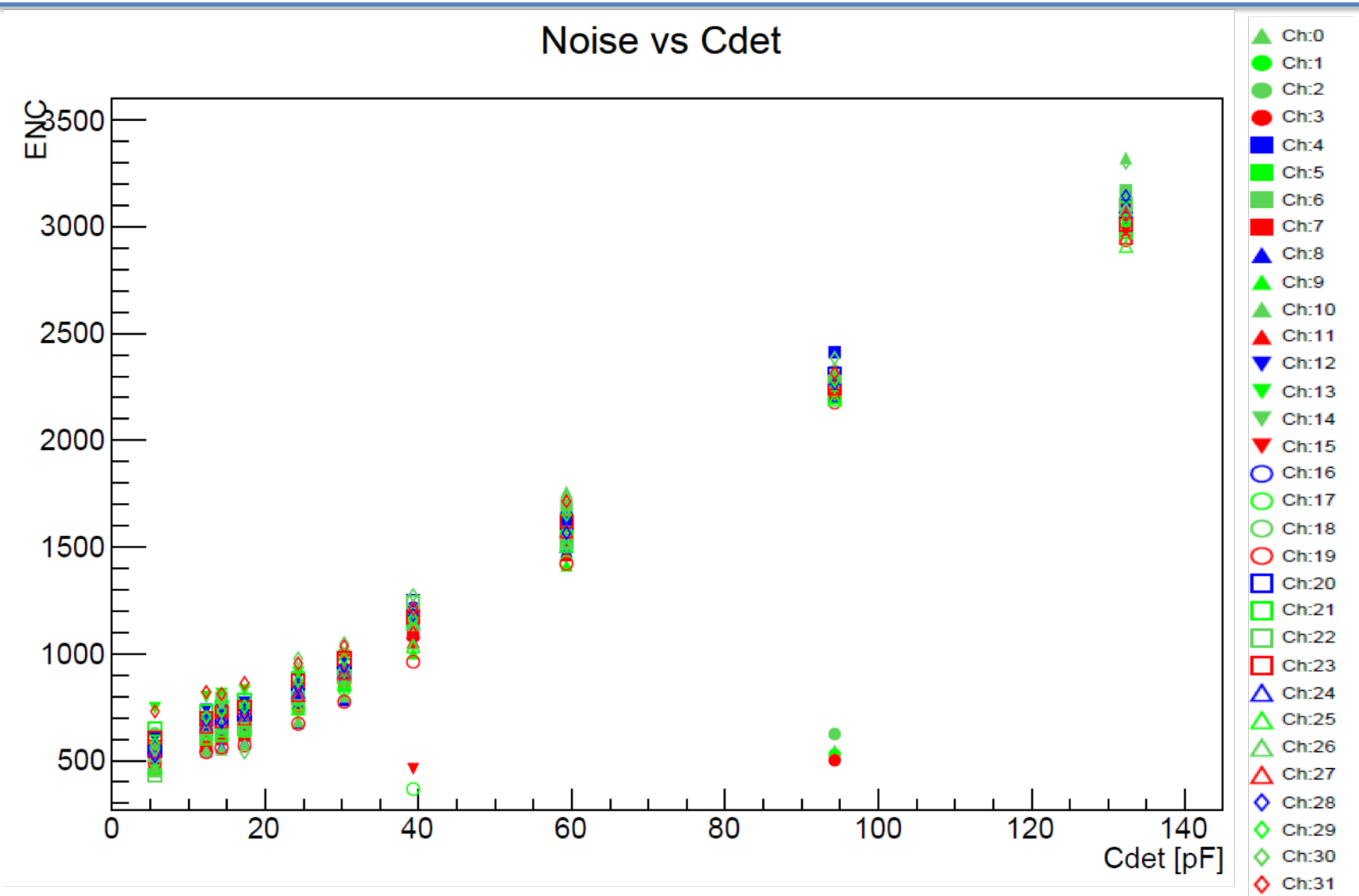


SAMPA : ADC

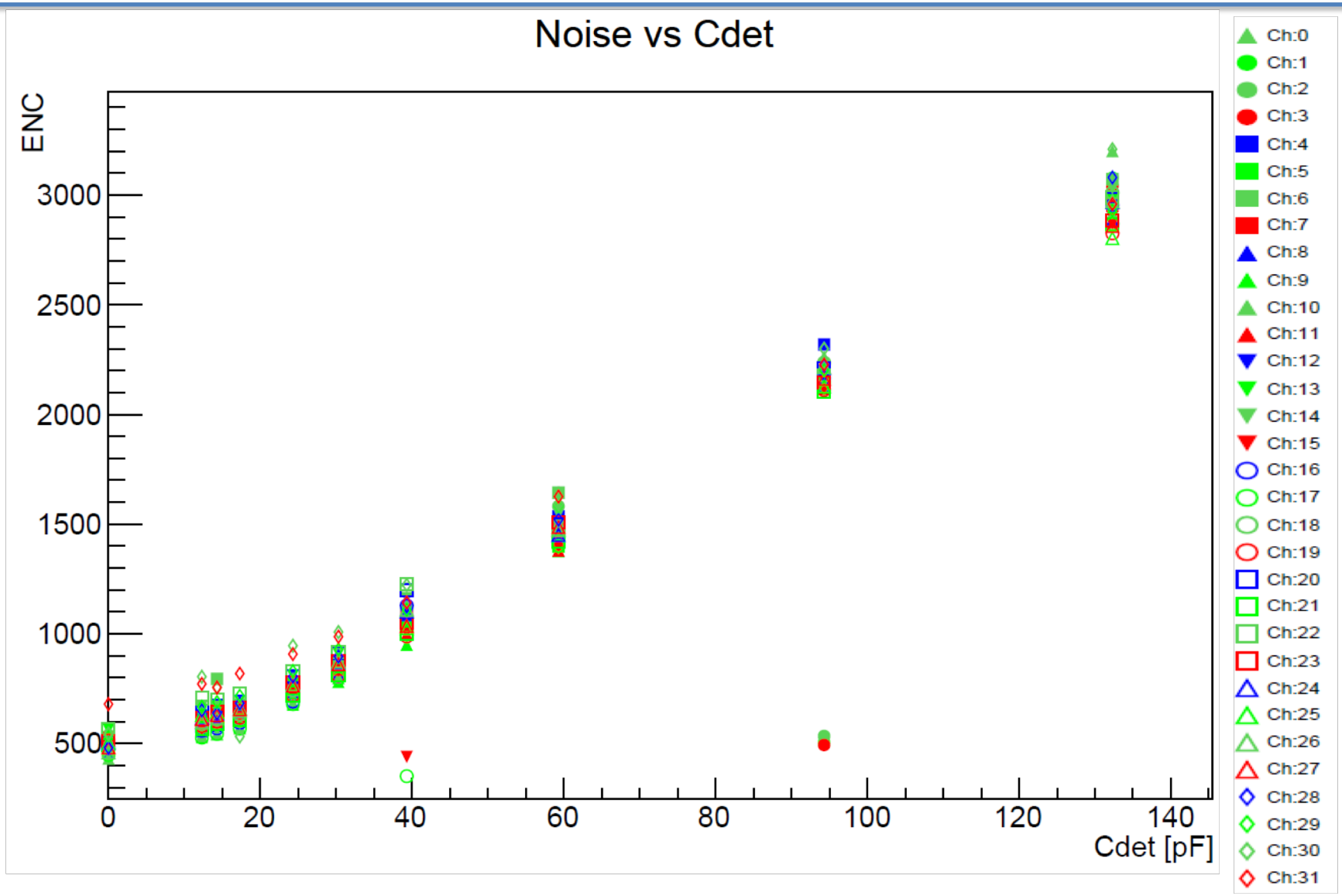
- SAR ADC: 80MHZ (Conversion clock) and 10MHz (Sampling Clock)



Noise, TPC 20N160 - SAMPLE 057



Noise, TPC 30N160 - SAMPLE 057



How to emulate a burst of charge pulses

”stairs-shaped waveform”, 63 steps, 1µs apart, + a last one after ~16µs, applied via series C_{inj}