Distributed I/O Tier project

Task of HL-LHC WP18

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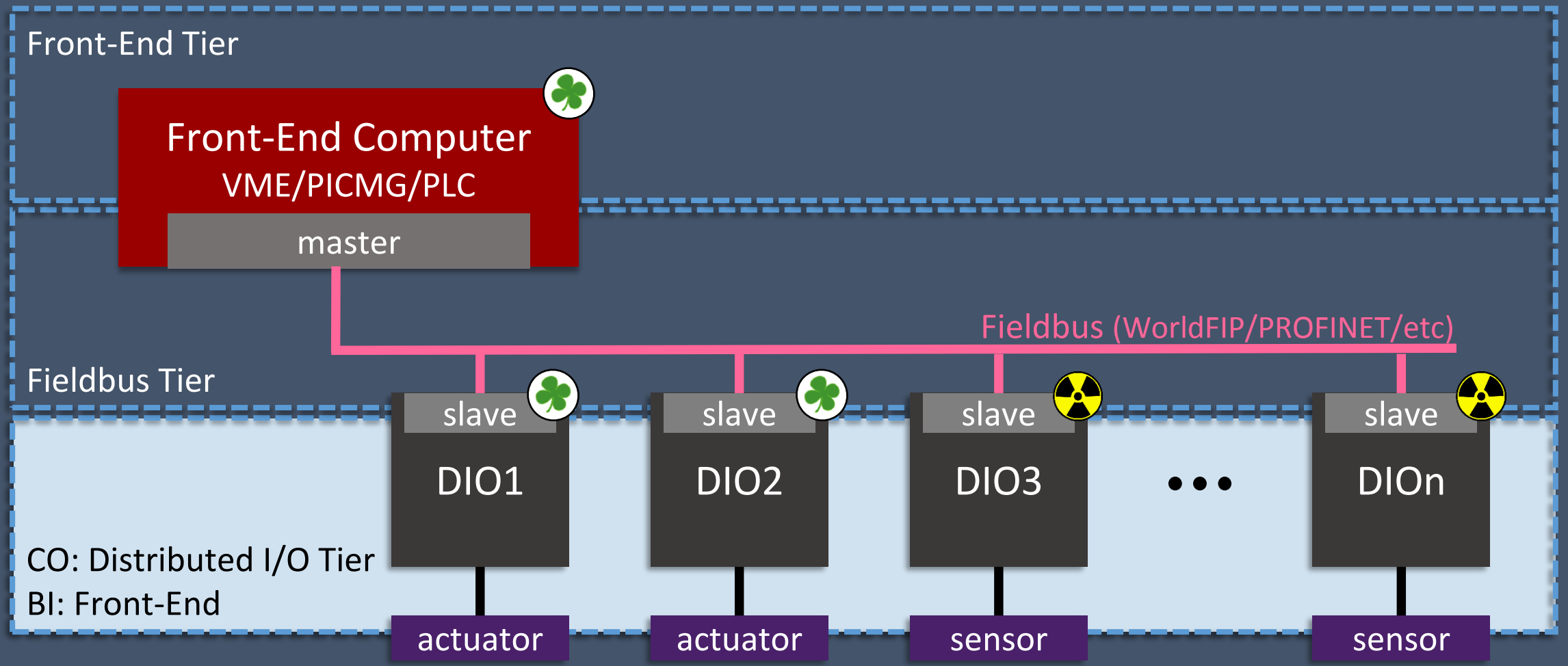
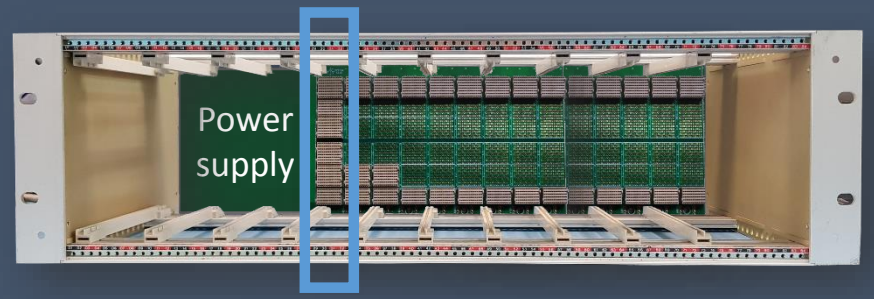
(BE-CO)

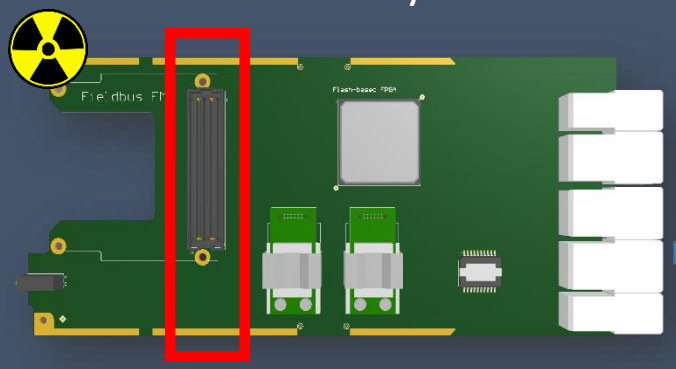
Custom electronics architecture



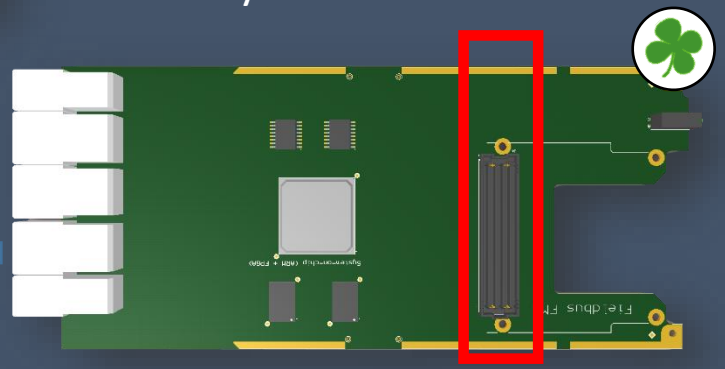
Common hardware kit for DIOT

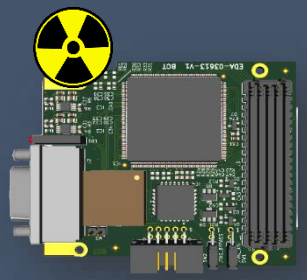


Radiation-tolerant System Board

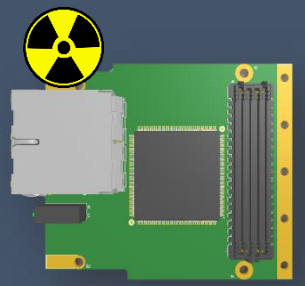


System Board

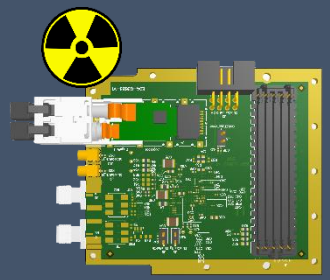




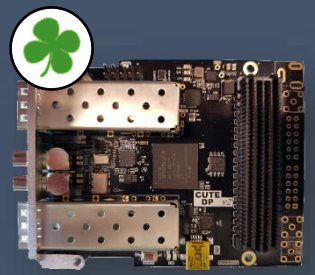
WorldFIP FMC



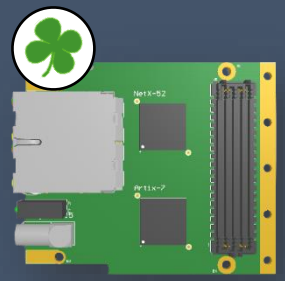
Powerlink FMC



LpGBTx FMC



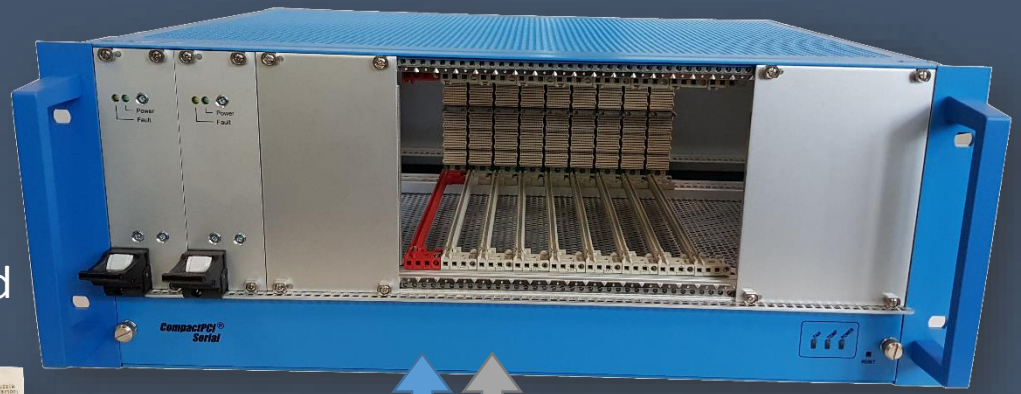
White Rabbit FMC



Industrial Ethernet FMC

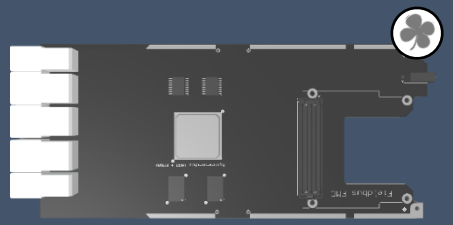
First DIOT demonstrator for lab tests

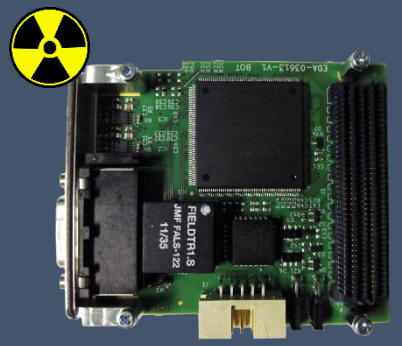
First DIOT demonstrator



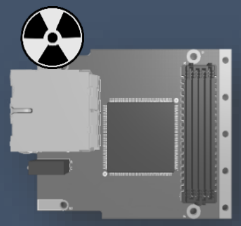
Radiation-tolerant System Board

System Board

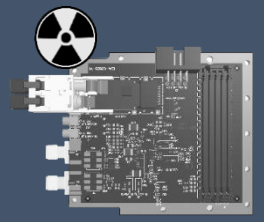




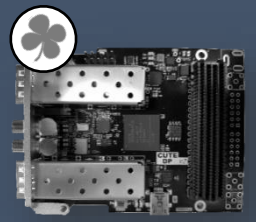
WorldFIP FMC



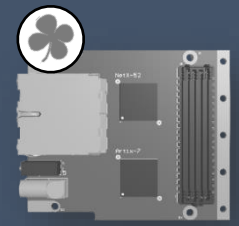
Powerlink FMC



LpGBTx FMC



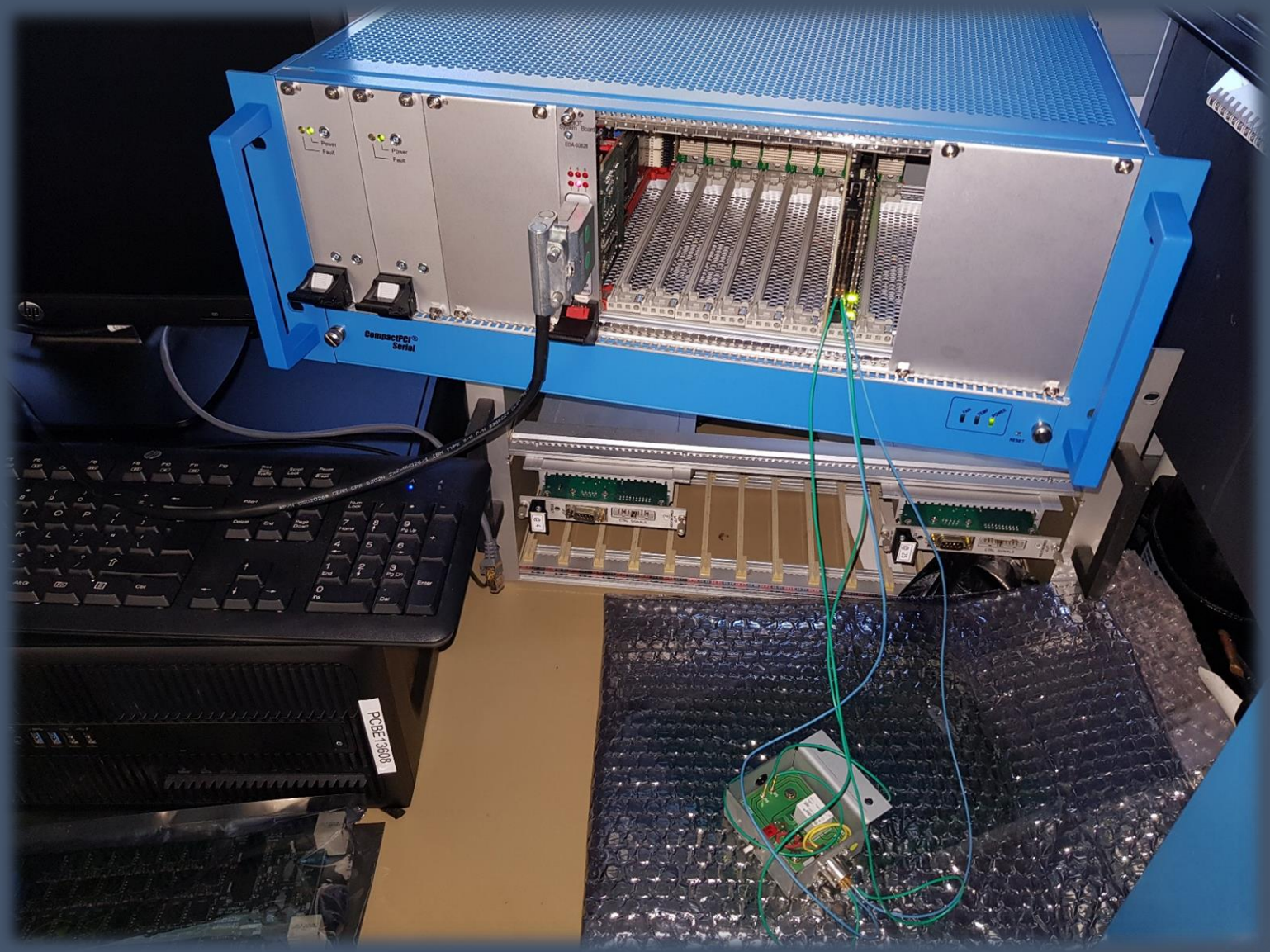
White Rabbit FMC



Industrial Ethernet FMC

DIOT demonstrator

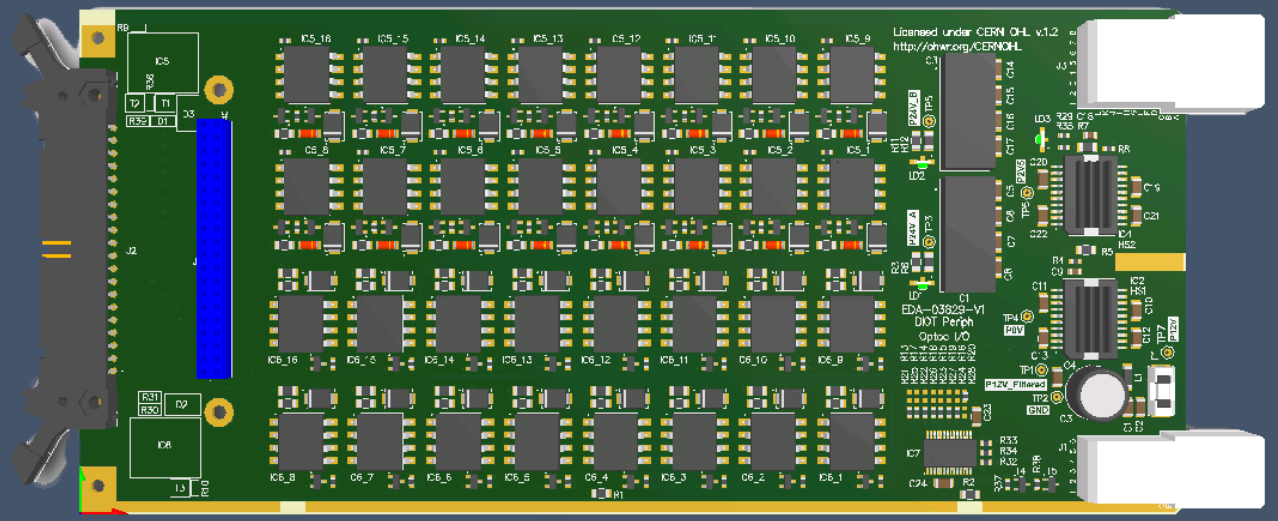
- Off-the-shelf chassis
- Redesigned C-GEFE
  as the main FPGA board
- NanoFIP FMC mezzanine
  for WorldFIP communication
- 16 I/O Peripheral Board
  for WIC (TE-MPE)



System Board prototype

- EDA-03828
- Redesigned C-GEFE
- Added backplane connector to communicate with peripheral boards
- Together with: BE-BI (Manoel), TE-MPE, EN-SMM
- WIC application logic in FPGA
- Simple crate monitoring

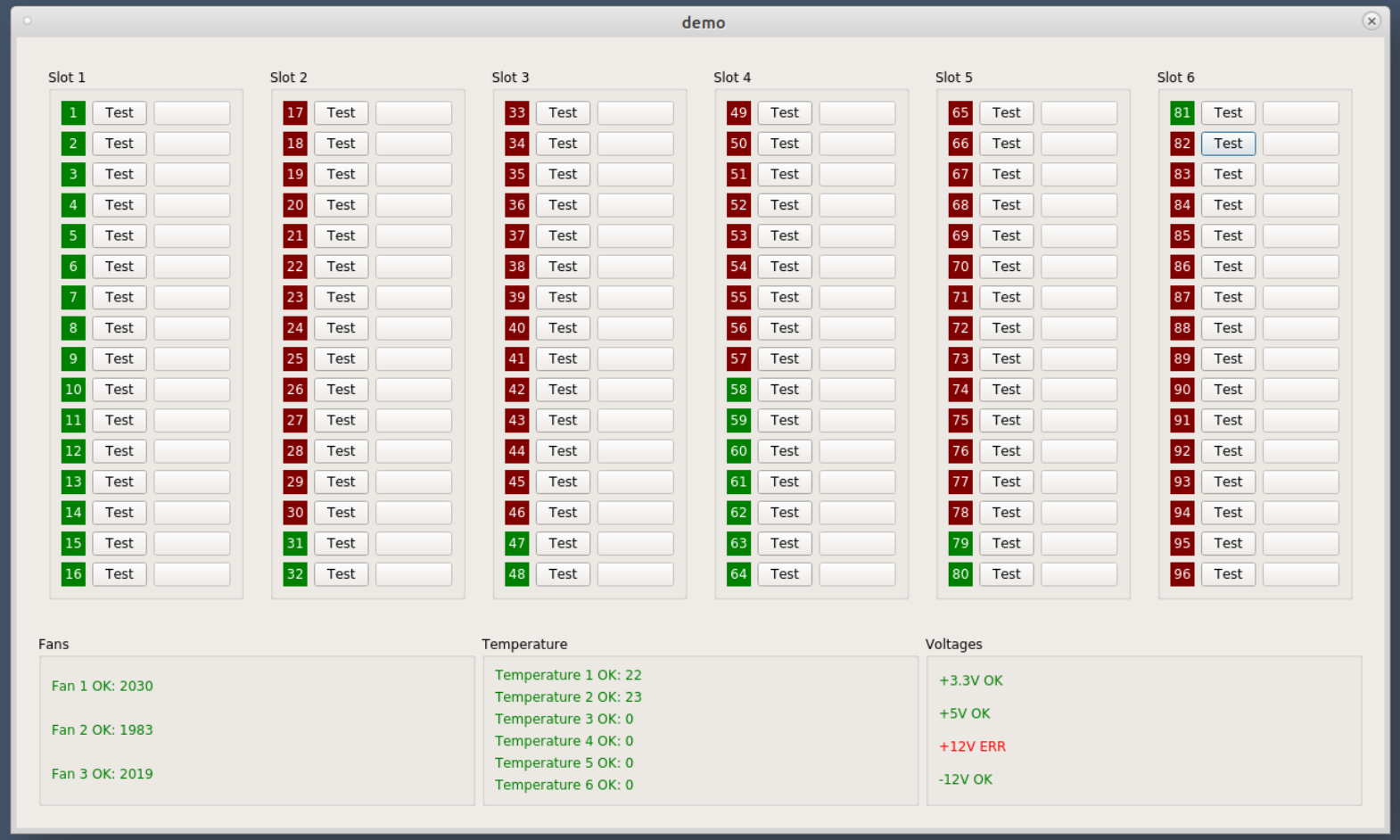
Template Peripheral Board



- EDA-0829
- I/O board based on requirements for Warm Interlocks application (TE-MPE)
- 24V production
- 16 opto-coupled current loop inputs
- 16 opto-coupled relay driving outputs
- Template for other DIOT developments

DIOT demonstrator GUI

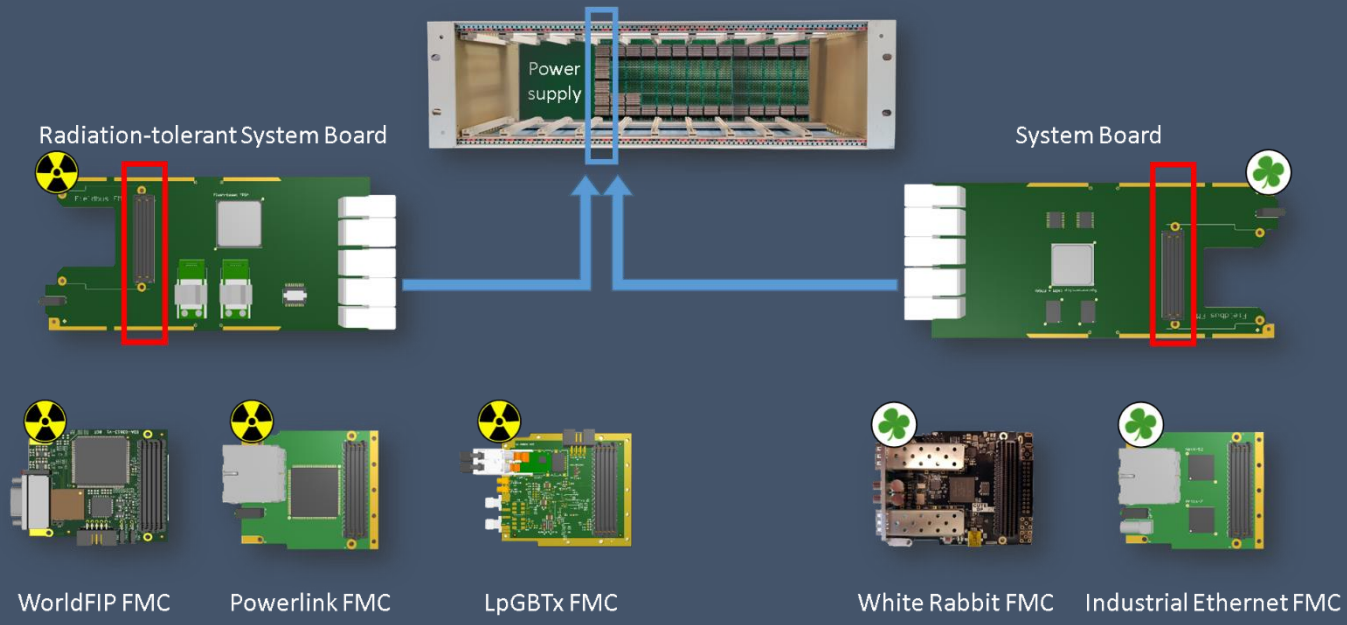
- Simple GUI running on MasterFIP PC
- Reads inputs (current loops state)
- Drives outputs (current loops test relays)
- Displays simple monitoring



Work towards final DIOT hardware kit

List of developments

- <u>Development together with equipment groups</u>
  - everyone has expertise about the final system
- 3U crate specification and design (with industrial partner)
- Rad-tol power supply
- Rad-tol System Board
- Rad-tol Powerlink FMC
- LpGBTx FMC
- Non-rad-tol System Board
- Common HDL for monitoring
- Reliability studies



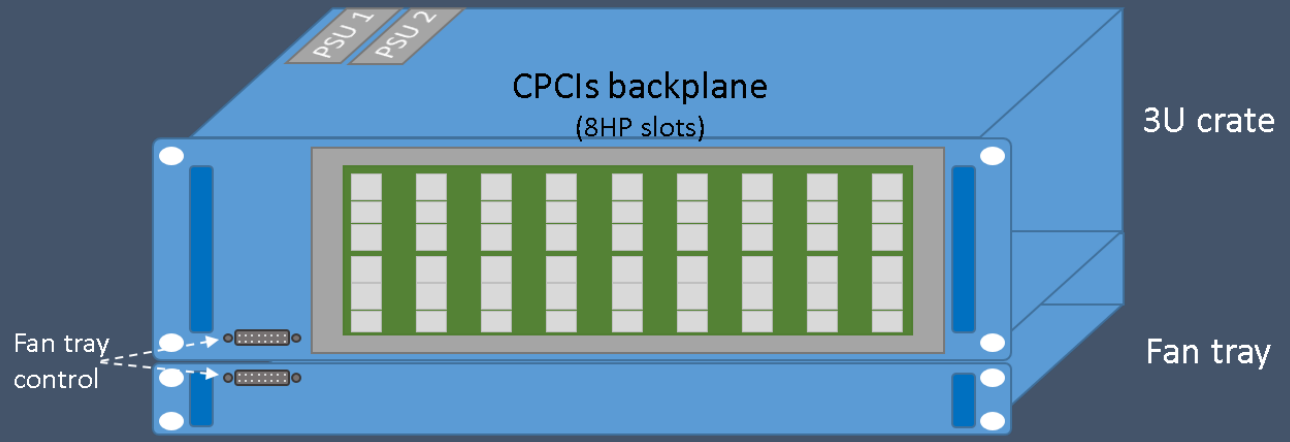
Preliminary crate specification (may still evolve)

https://wikis.cern.ch/display/DIOT/Distributed+IO+Tier+chassis

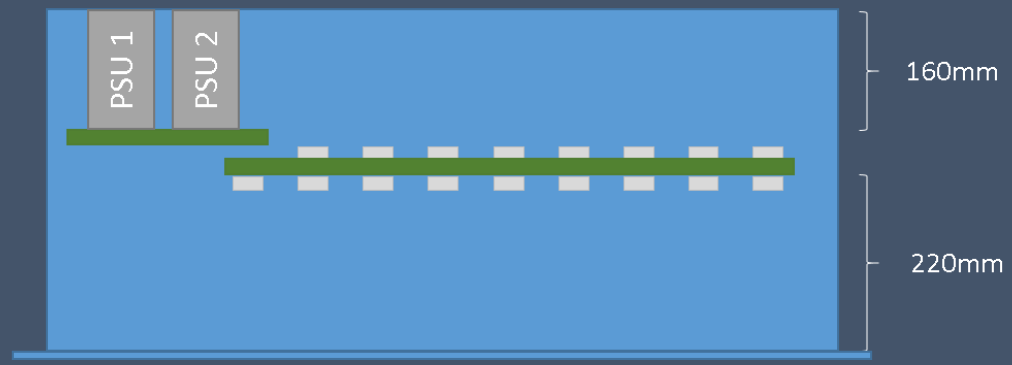
- 3U CompactPCI Serial crate
- 1U optional fan tray
- Grounding and EMC: to be discussed

- 9-slots backplane, each slot 8HP
- 220mm front boards
- ≥ 160mm RTM space
- Two PSU slots in the back
- Low cost
- Open-hardware

Front view

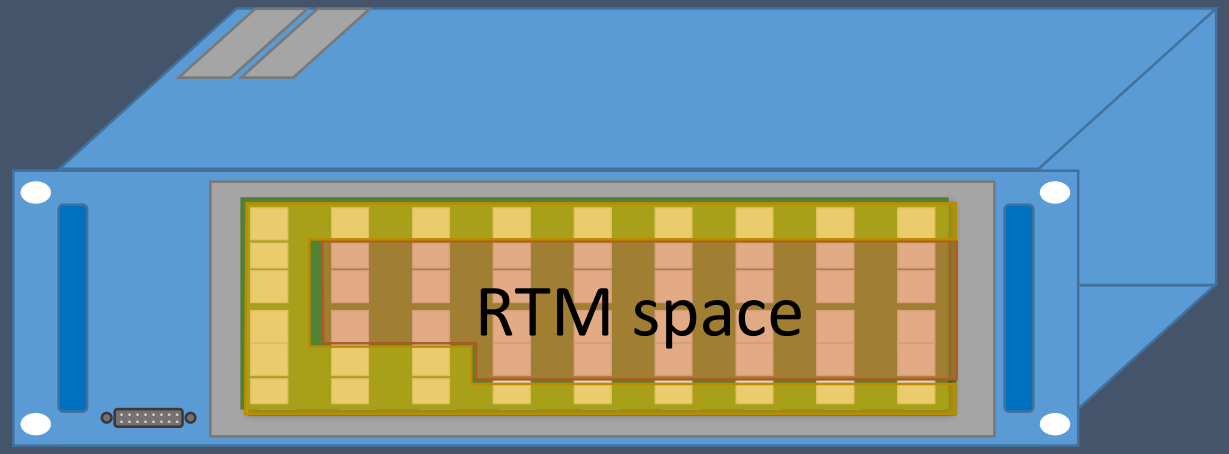


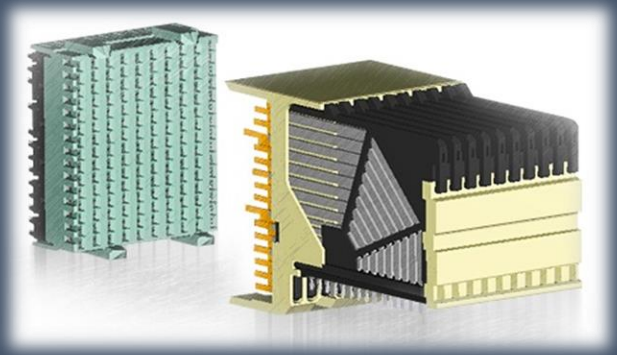
Top view



Preliminary crate specification (may still evolve)

- Backplane split in two regions
- Star-topology differential lanes from System Slot to Peripheral Slots
  - AirMax VS connector system to ensure enough GND, signal I/Os and support fast signaling
- RTM space
  - Rear modules
  - … or expansion backplane (e.g. for aux voltage distribution)
  - We can specify different connector type
- AirMax VS
  - Used in transportation applications
  - 72-pin and 96-pin variants used
  - Up to 0.95A per-pin





Rad-tol power supply

https://wikis.cern.ch/display/DIOT/Rad-tol+power+supply

- Fellow (Lalit) dedicated to this task
- Official collaboration set up with R2E and TE-EPC
- R2E support for common building blocks
- Design together with all equipment groups
- Currently gathering requirements and drafting specification
  - +12V, +5V, 100W
  - PMBus monitoring interface
  - Redundancy
  - Standard PSU connector FCI 51939-667
- … and working on first lab prototype using FEAST chips

System Boards

- 3U: 100mm x 220mm
- FMC connector for communication mezzanines
- AirMax Vs backplane connectors (grand total 338 signal lines available)

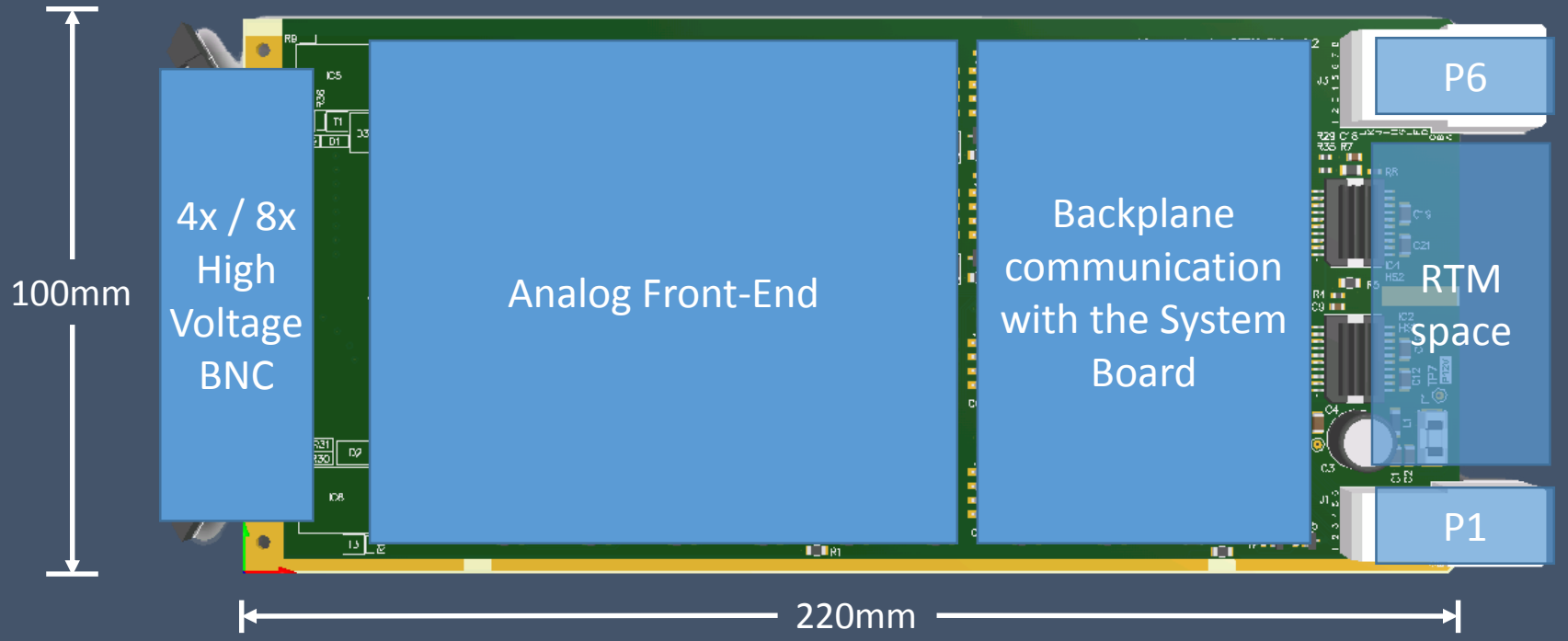
Radiation-tolerant

- NanoXplore or Microsemi FPGA
- Together with: EN-SMM, TE-MPE

Non-Radiation-tolerant

- SoC-based
- Now specification drafting with EN-SMM and TE-ABT

BLM Peripheral Board idea



- 4 or 8 (requires double width front panel) High Voltage BNC
- P1 mandatory for power and backplane communication
- P6 optional if more backplane lines are required
- RTM space for optional rear modules connectivity or custom backplane

Timeline

Sep 2018

- First hardware demonstrator ready

Work with equipment groups, HL-LHC fellows and R2E on specifications and designs

LS2 (2019-2020)

- Building blocks/prototype available

LS3

- HL-LHC deployments