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Optimal Designing and Performance Evaluation of Inductive Superconducting Fault Current Limiter Combined with Low-Voltage Mechanical Circuit Breaker in DC Microgrid System

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Background

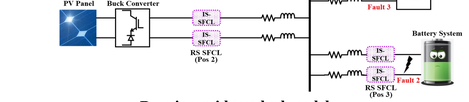
- Dc microgrids based on renewable energy sources are in the limelight as the next-generation distribution network. Thus, **to operate a dc microgrid reliably, it is essential to provide an effective protection scheme.**
- Due to **the importance of the stability and reliability** in renewable sources-based dc microgrid, low-voltage mechanical circuit breakers (**LV DCCB**) and superconducting fault current limiter (**SFCL**) **have many advantages to improve dc microgrid durability**.
- Because SFCL is bulky and expensive, it has been **mainly applied to power transmission system**. However, recently, as the optimal design of the SFCL has been developed, **many researches are being conducted to apply to the low-voltage distribution system**.
- Despite the high interrupting reliability and near-zero steady state loss, recent **DCCB researches are related to solid-state and hybrid type that have a fast interrupting performance using semiconductor switch.**
- Because DCCB's strengths are important to develop dc microgrids, by combining low voltage DCCB and SFCL, we designed a protection scheme that **can compensate for the drawbacks of LV DCCB.**

Objectives

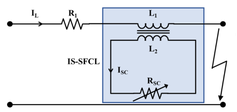
- In this paper, we proposed an **optimal design of inductive shielded core SFCL (IS-SFCL) combining LV DCCB to protect dc microgrid** reliably and improve the interrupting efficiency.
- IS-SFCL's optimal position was selected, and the LV DCCB was optimized through comparison by dividing the case with and without SFCL.

Methodology & Simulation Model

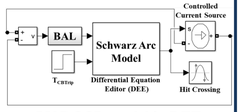
- **Fault Location : the rectifier side fault (RSF)** and **the battery side fault (BSF)** were considered. Because PV side discharging current is low, PV side faults (PSF) is excluded from analysis. And **load side fault (LSF)** is simulated.
- **Location of SFCL :** the location of the SFCL is located on the **ac utility**, **PV system**, and **battery system.**
- **Optimal Design of LV DCCB :** SFCL and the DCCB were installed at the position **derived from the optimal positioning simulation**. the simulation was performed by considering the cases with and without application of SFCL.
- Dc microgrid model : The dc microgrid is a bipolar system (±400 V) consisting of three multiple distributed sources, an **ac utility grid**, a **PV array**, **a battery system**, and **dc loads**, as shown in Figure.
- IS-SFCL model : IS-SFCL consists of a **superconducting module** of R component, **a primary and secondary transformer module** (L component).
- LV DCCB model : **Schwarz model** have a great strength in expressing the large current region and the small current region using the four parameters. The LV DCCB specification designed in this paper use a DCCB model that was developed using a parametric sweep method in previous paper **based on Eaton's commercialized DCCB.**



Dc microgrid test-bed model



Inductive shielded core SFCL model



LV DCCB model in DEE

Detailed specifications of dc microgrid

AC Network	
Transformer	22.9 kV / 0.6 kV, 500 kVA
AC/DC Converter	3-Level NPC Converter,
DC loads	150 kW
PV System	
Arrangement	30 × 30 = 900 modules
Temperature / Irradiance	25 °C / 525 W/m²
Capacity	190 kW
Battery System	
Battery Type	Lithium – Ion
Capacity	690 V / 145 Ah, 100 kW

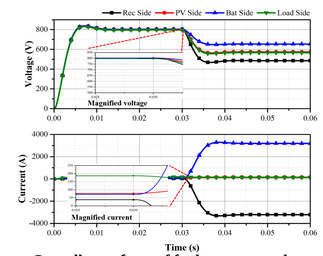
Main parameters of IS SFCL and LV DCCB

IS-SFCL	
R_{SC}	0.05 Ω
Voltage ratio (V_1/ V_2)	400 V / 240 V
Winding Impedance (R_1, R_2 / L_1, L_2)	0.00001 P.U. / 0.0004 P.U.
LV Mechanical DCCB	
Arc time constant (τ)	6.91 e-4
Exponential component of τ (α)	0.166
Cooling Power (P)	846 kW
Exponential component of P (β)	1.65

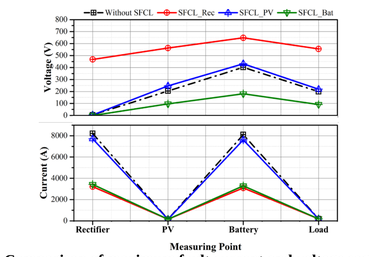
Conclusion

- Simulations of optimal position where SFCL would be most effective were conducted to analyze various fault scenarios. RS SFCL showed superior performance in all cases except voltage sag in BSF at BS SFCL. Thus optimal position of IS-SFCL is selected on the RS.
- In optimal design of LV DCCB, The arc current was reduced 60 % and rise of transient rate was improved. Also, the breaking capacity was reduced 66.5 % and interruption speed was faster 4 ms than without SFCL.
- Therefore, **feasibility of the IS-SFCL in dc microgrid was verified**, and the **optimal position was selected**. In addition, the combination of two reliable protection devices **has led to the advantages of high reliability and efficiency**.

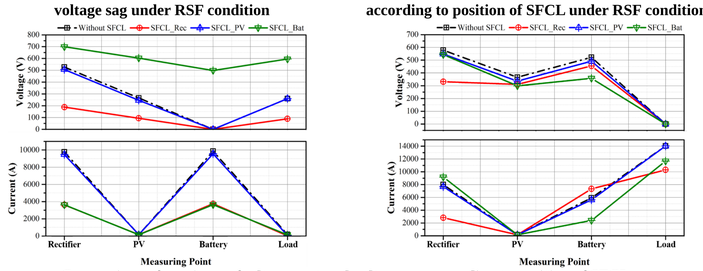
Simulation Results and Discussions



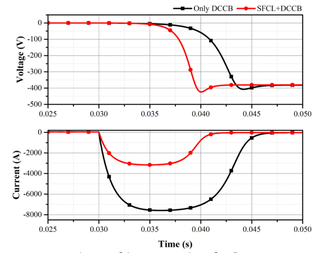
Overall waveform of fault current and voltage sag under RSF condition



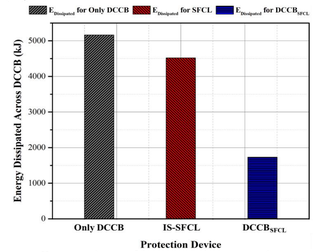
Comparison of maximum fault current and voltage sag according to position of SFCL under RSF condition



Comparison of maximum fault current and voltage sag according to position of SFCL under BSF (left) and LSF (right) condition



Comparison of interrupting fault current and voltage in DCCB



Comparison of interrupting capacity by protection devices

Performance of the IS-SFCL under different simulation conditions

Rectifier Side Fault Condition

Measuring Point	Current limiting ratio			Voltage compensating ratio		
	RS	PS	BS	RS	PS	BS
Rectifier	**60.84**	6.1	58.29	**57.9**	0	-0.41
PV system	**0.72**	1.23	-0.2	**44.79**	5.27	-13.51
Battery	**61.87**	6.16	59.41	**30.81**	3.75	-27.6

Battery Side Fault Condition

Measuring Point	Current limiting ratio			Voltage compensating ratio		
	RS	PS	BS	RS	PS	BS
Rectifier	**62.97**	3.12	**62.88**	-42.33	-2.54	**21.48**
PV system	**-0.28**	0.04	**1.03**	-21.45	-2.52	**42.15**
Battery	**61.96**	3.09	**63.09**	0	0	**62.29**

Load Side Fault Condition

Measuring Point	Current limiting ratio			Voltage compensating ratio		
	RS	PS	BS	RS	PS	BS
Rectifier	**64.61**	3.83	-14.93	**-30.83**	-3.79	-4.31
PV system	**-0.17**	0.05	-0.1	**-6.94**	-3.77	-8.4
Battery	**-23.87**	5.04	59.56	**-8.46**	-3.76	-20.49

A. Optimal Positioning of the IS-SFCL

- **RSF case**: The maximum value of fault current and voltage sag at each terminal **according to SFCL position in RSF condition**. **Without SFCL**, the maximum fault current is **8.2 kA** on **RS terminal**, **157 A** on **PV side (PS)** terminal, **8.1 kA** on **battery side (BS)** terminal and **194 A** on **LS terminal**. Voltage sag was significantly reduced in all sections, including **RS 4.3 V**, **PS 204 V**, **BS 401 V**, and **load side (LS) 199 V**. the **current limiting ratio of RS SFCL was reduced by 60%** in RS and BS and **voltage compensating ratio** was clearly improved by **BS 30%, PS and LS 44%, RS 57.9%** in all sections. Therefore, the most effective location to mitigate fault current and voltage sag is RS SFCL.
- **BSF case** : When SFCL is applied to each position, **the tendency of fault current is similar to the RSF condition**, but **from the viewpoint of voltage sag, it shows superior performance when SFCL is placed on the BS**. Therefore, in case of BSF, BS SFCL can be selected as the optimal position.
- **LSF case** : First, in terms of fault current, the maximum value of the fault current fed to the load side was **the lowest when SFCL was placed on the RS**. Therefore, **it shows better performance than the BS SFCL at all measuring points**. In terms of voltage sag, it was lower in all cases than without SFCL. From this point of view, voltage sag is most affected by placing SFCL at the point where the fault occurred. Therefore, when comparing the voltage sag compensation ratios of RS SFCL and BS SFCL, **PS -6.94%,** while **BS -8.46%,** thus **RS SFCL is the most suitable position** with better voltage sag compensation.

B. Optimal Design of the LV DCCB

- Arc current and voltage : Without SFCL, the fault current has risen to about 8 kA and the interruption time is 16 ms. On the other hand, when SFCL and DCCB were operated together, the interruption time of the fault current of about 3.2 kA was 12 ms, which **shortened the previous interruption time by 4 ms**. Also, rise of transient rate (**70.94 V/ms**) was bigger than the without SFCL (**44.94 V/ms**).
- Energy dissipation : As can be seen from the graph, when SFCL is absent, the breaking capacity that the DCCB must withstand is **5 MJ**, whereas in the case of DCCB combined with SFCL, the breaking capacity requirement is greatly reduced to **1.7 MJ.**