USe R&D Activities for Future Colliders
IFCA Meeting 19-20th November 2018

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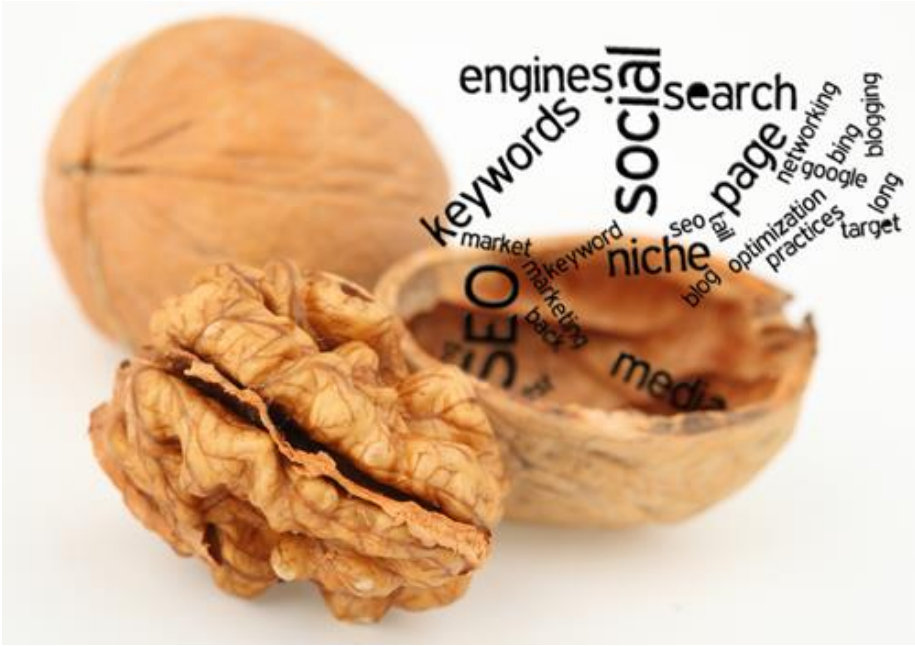
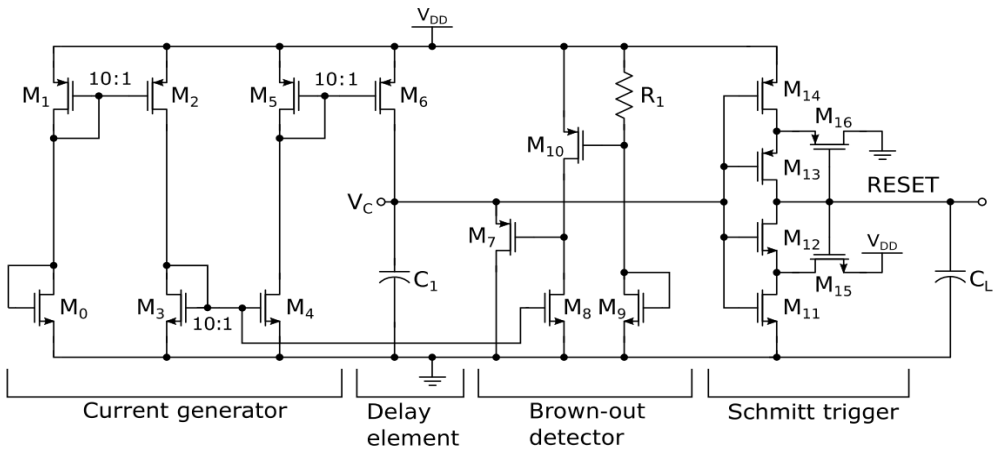
In a Nutshell

- Microelectronics Activities
  - RD53B chip
  - RD53_SEU chip
  - HVCMOS ENGRUN-1
- Discrete Electronics Activities
  - Roc4Sens DAQ Board

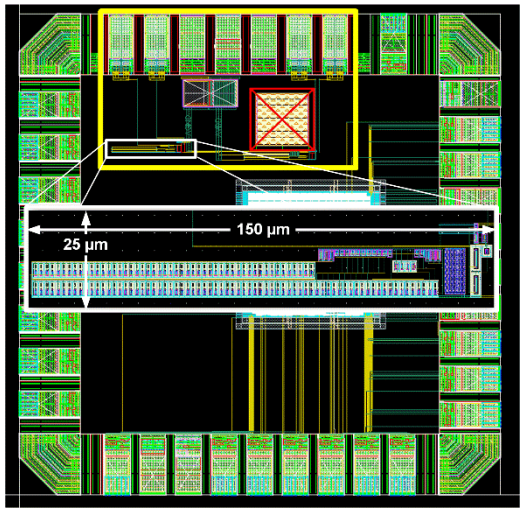


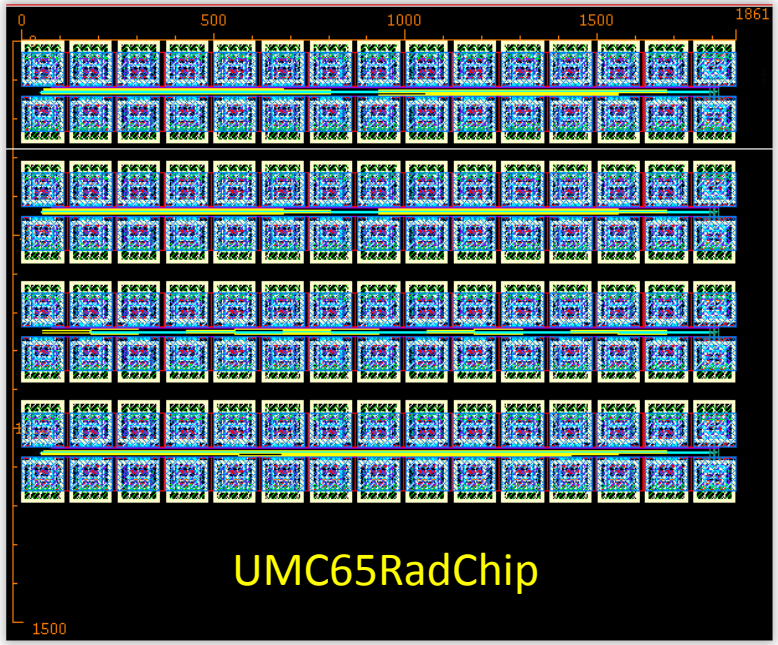
RD53A

- Development of an IP block, PowerOnReset (IEEE TNS Agosto 2018)
  - Delivered and working in RD53A chip
  - TID and SEE characterized, by simulation and radiation testing
- Development of an UMC 65nm mini@sic for TID/SET radiation characterization of transistor technology/layout alternatives
  - Delivered and working in February 2018
  - Now under TID radiation testing analysis at CERN



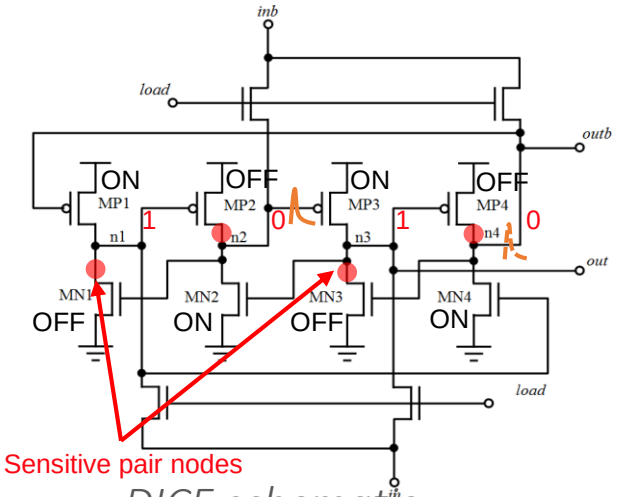
Power On Reset



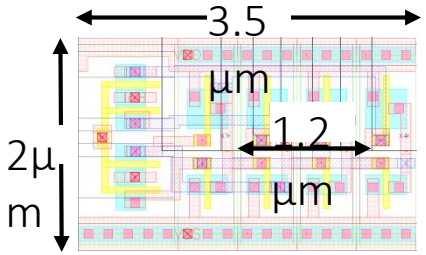


RD53B

- Development of the Data Merger digital block (RD53-CMS chip)
  - In specification phase
  - Master-Slave 1:5 for data sharing hub
- SEE Simulation analysis (AFTU, propietary software)
  - Every digital/mixed block in RD53A chip
  - Configuration Registers (DICE latches and other options)
  - PLL and Clock Generator now under final SEE simulation
- Verification tasks for RD53B digital design (one full time PhD Student)
  - Development of VEPIX2 simulator (evolution from the actual Verilog VEPIX)or VEPIX2 (evolución del actual VEPIX)
  - Verification of every digital design in RD53B



DICE schematic (example of a stored data = 1)

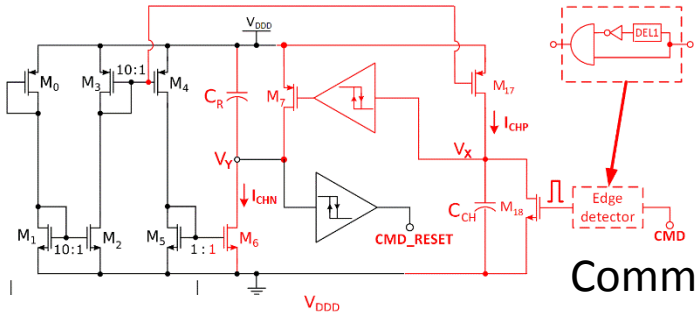


Layout DICE version 1

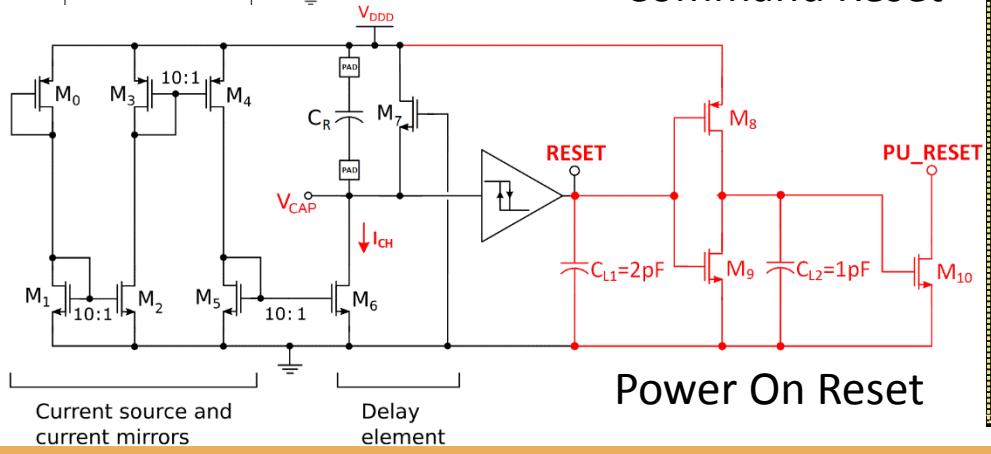
CPPM D.Fourgeron

RD53B

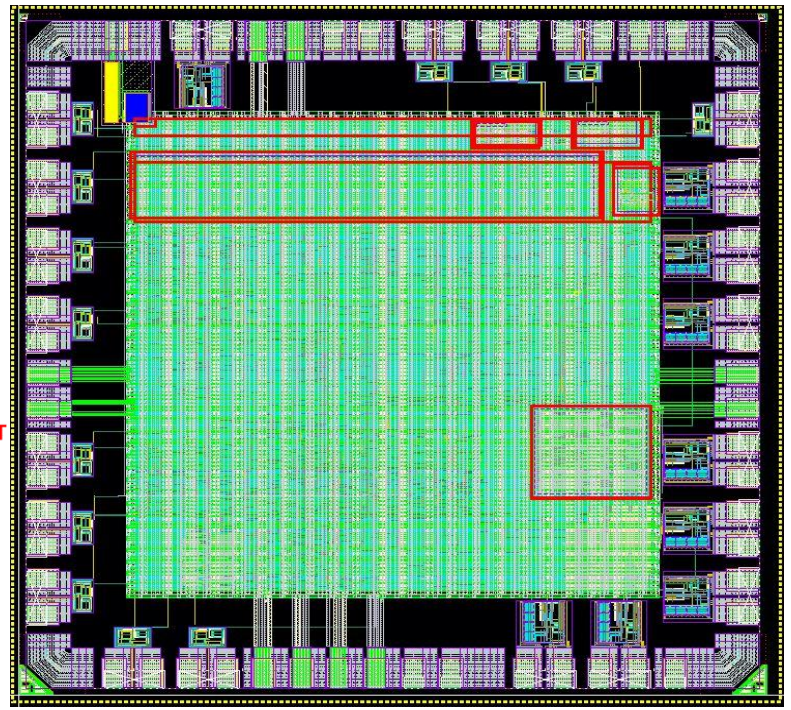
- Development of two IP blocks, PowerOnReset and Command Reset
  - Working in RD53B_SEU chip and delivered for the RD53B floor plan
- Development of RD53B_SEU chip: working to prepare the irradiation campaign (starting in Feb 2019@UCL Louvain)

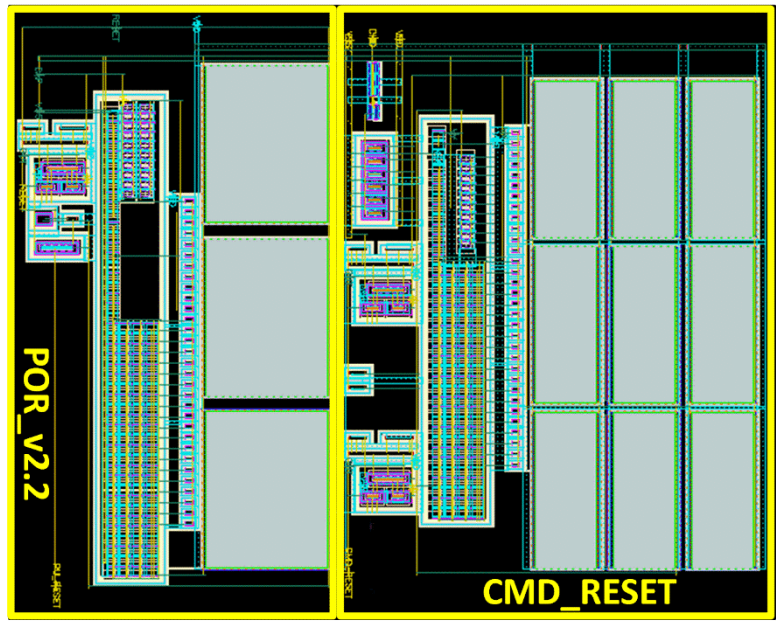


Command Reset



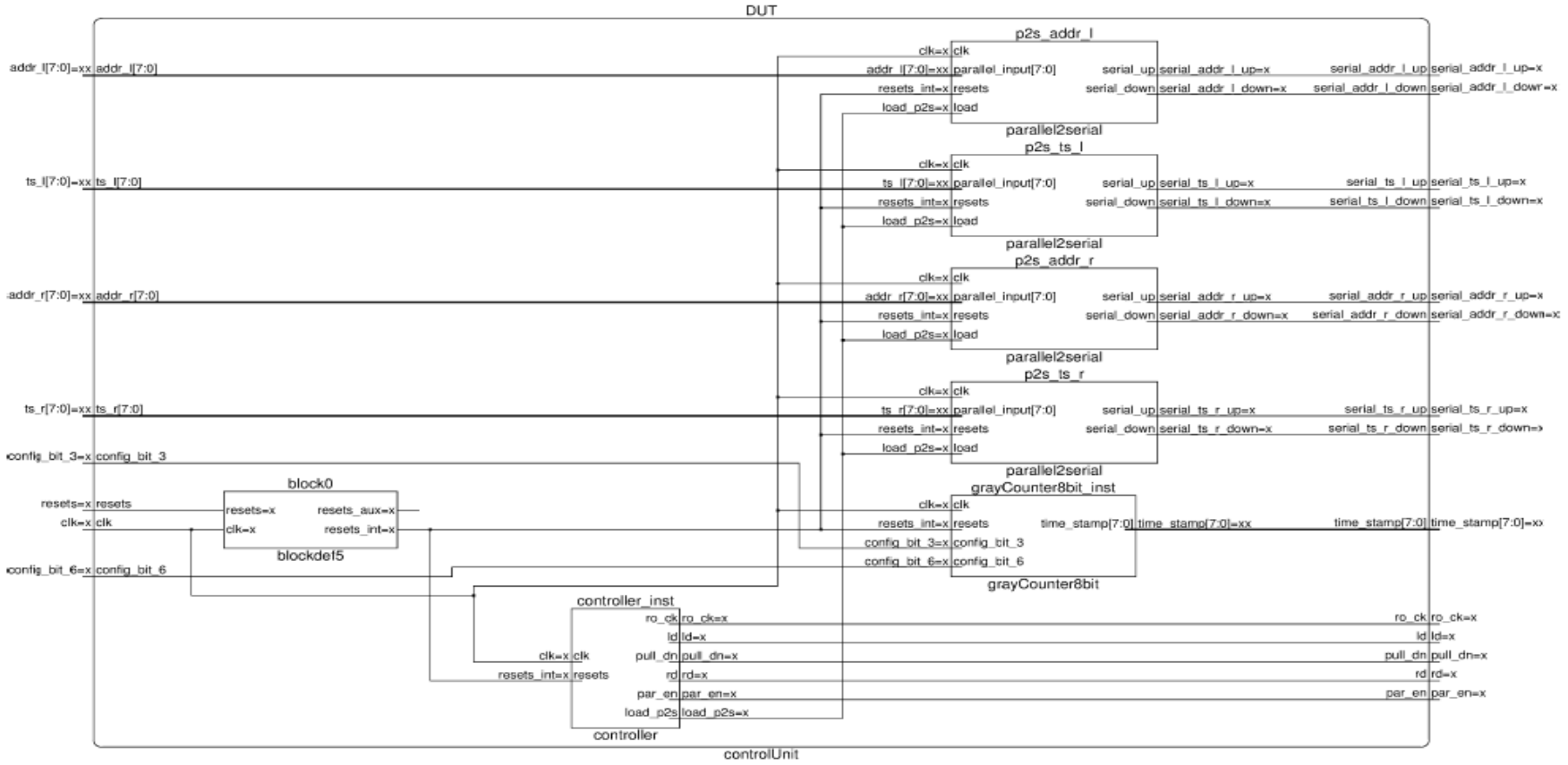
Power On Reset





HVCMOS LFoundry 150nm

- Task associated to RD50 collaboration
- Development of the Digital Bottom for the new chip HVCMOS LFoundry 150 nm “ENGRUN-1” (finite state machines, ports), full custom
- Design now ready for floor planning (matrix nº 3 in principle)



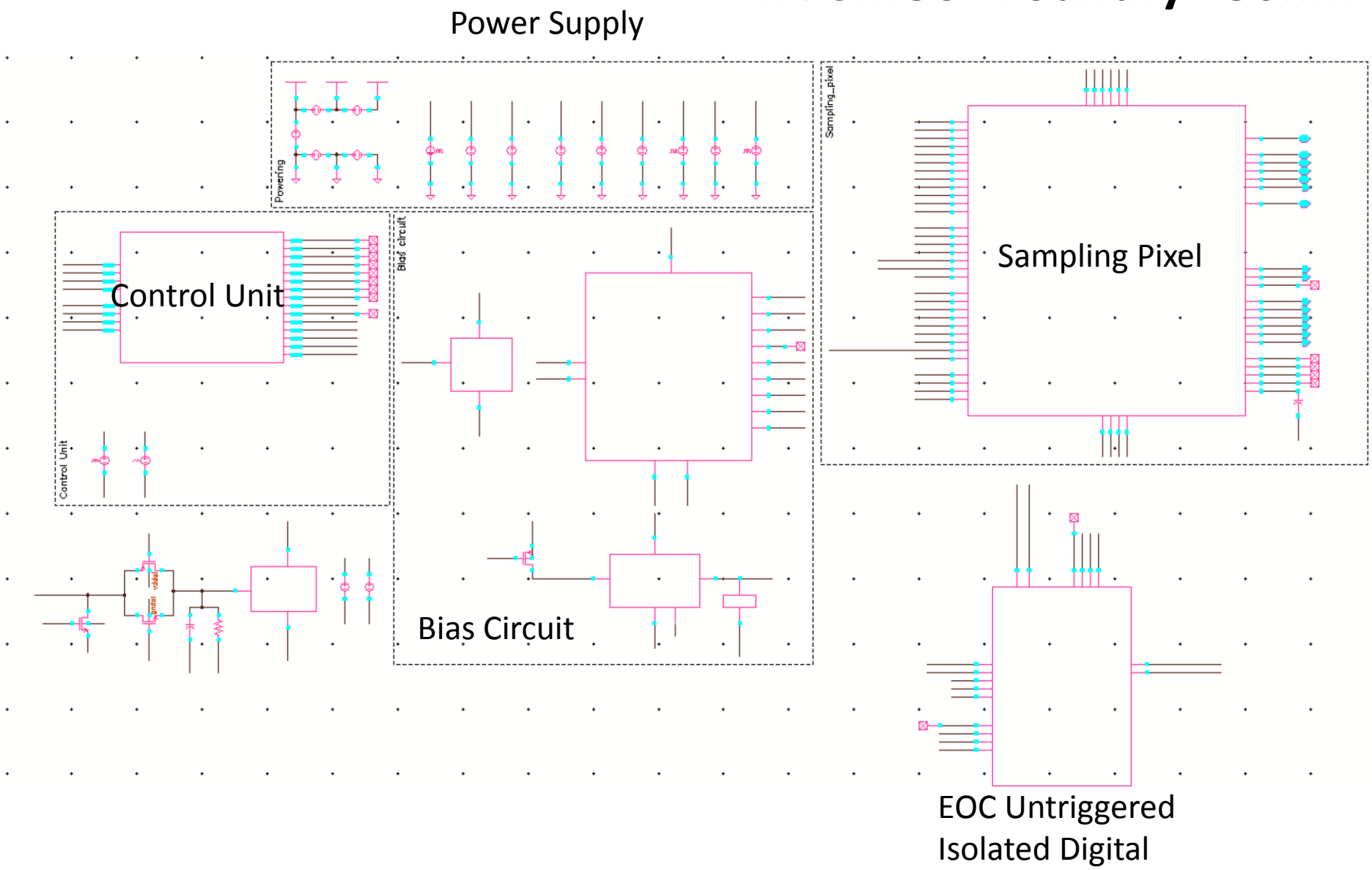
Cadence Simulations

HVCMOS LFoundry 150nm

Testbench for one pixel provided by University of Liverpool

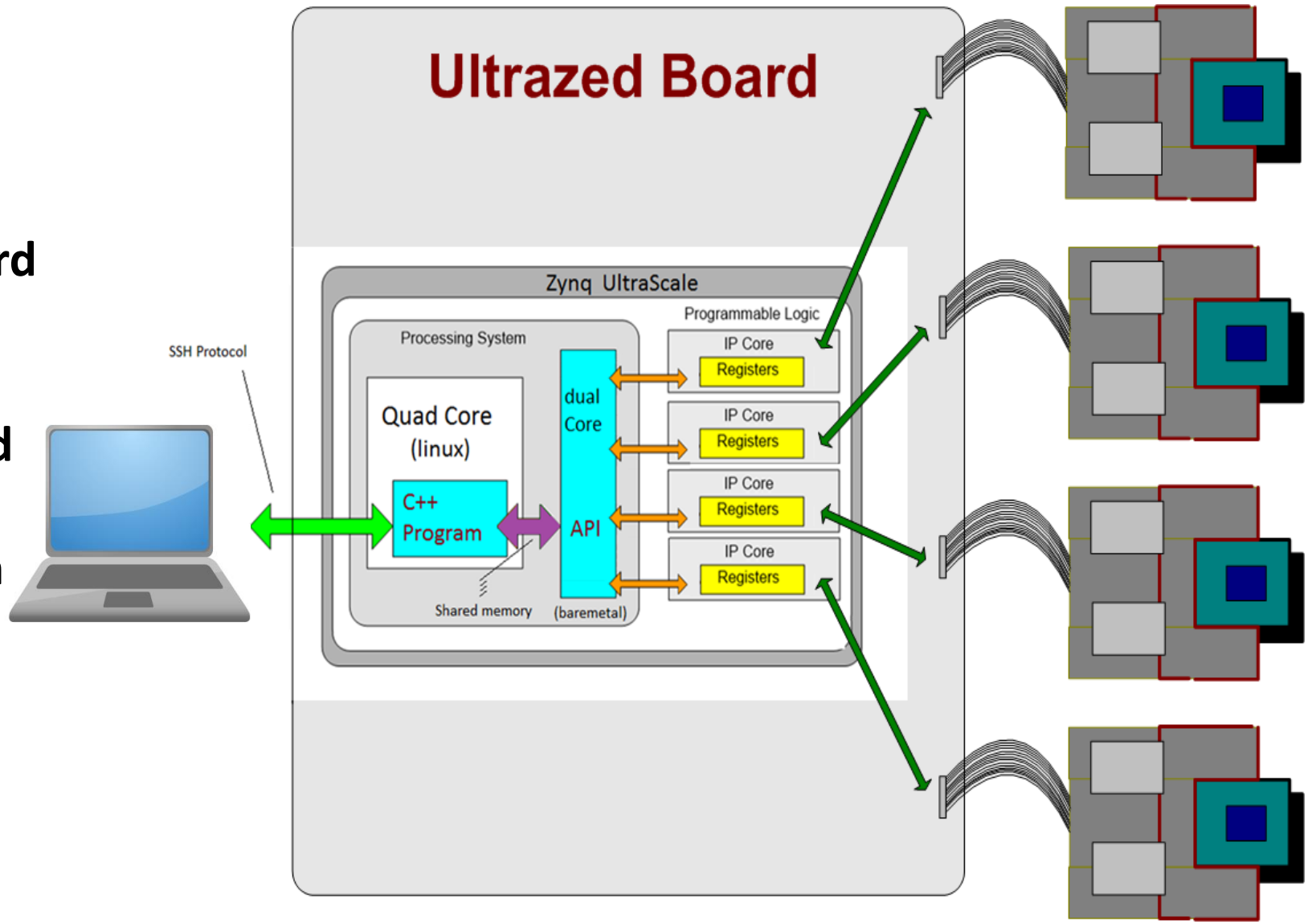
Ideal sources were replaced by the current gate-level implementation of the control unit

Comparison of different signals in order to check the behavior



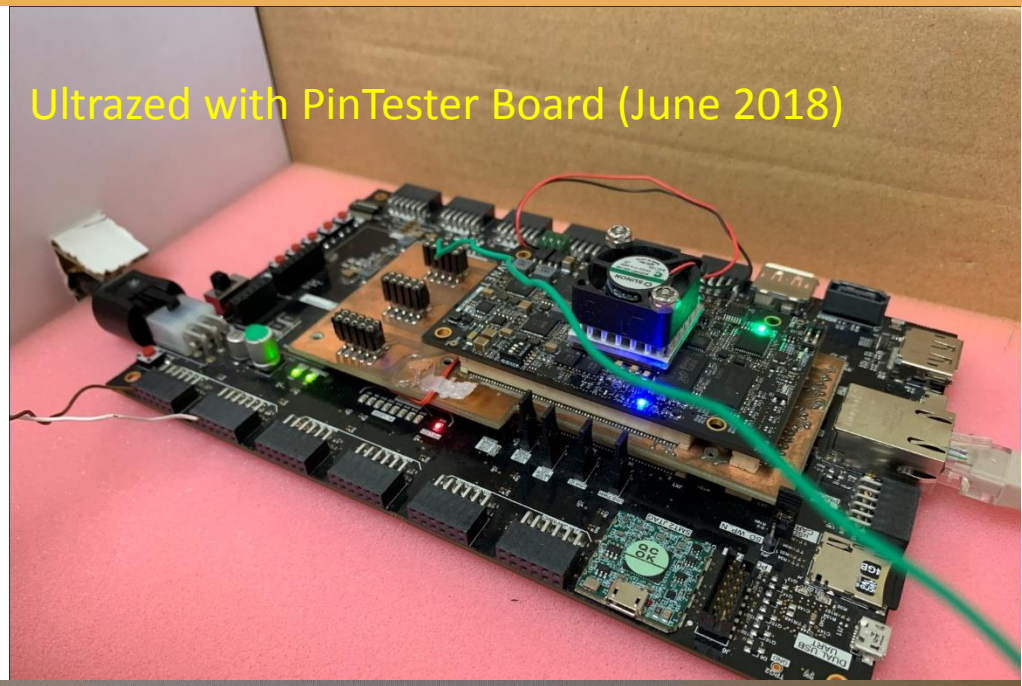
DAQ Roc4Sens

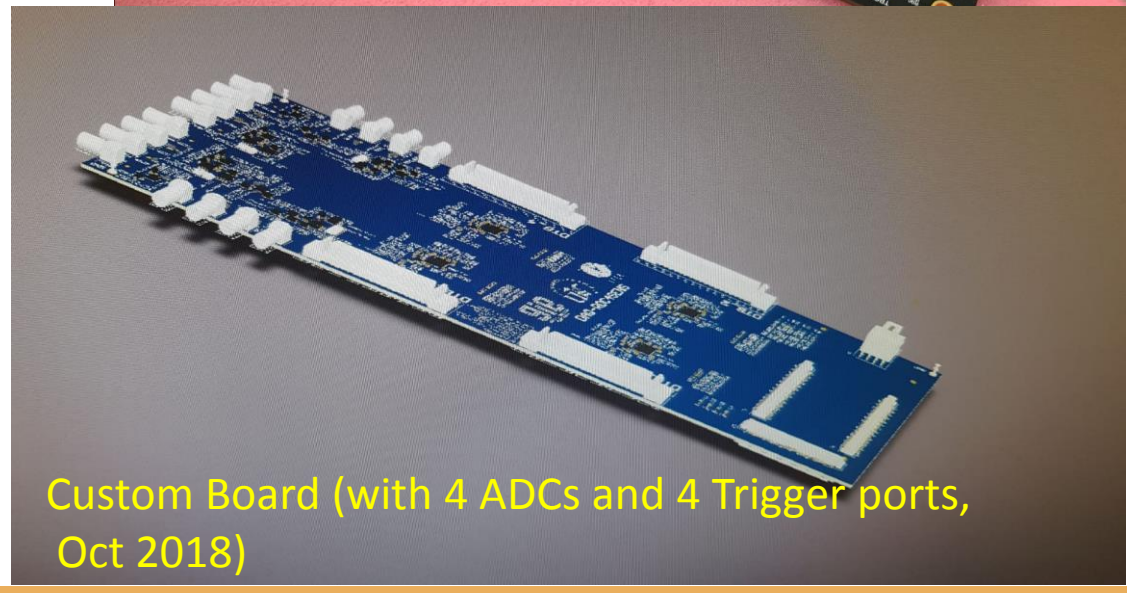
- USe-IFCA-PSI joint task
- Development of a DAQ DTB card for the Roc4Sens chip in Xilinx UltraScale technology)
- Development of the ADC board for DAQ
- System integration and Human Interface development



DAQ Roc4Sens

- USe-IFCA-PSI joint task
- Development of a DAQ DTB card for the Roc4Sens chip in Xilinx UltraScale technology)
- Development of the ADC/Trigger board for DAQ (Custom Board)
- System integration and Human Interface development
- NOW IN PRELIMINARY PRODUCTION PHASE:
  - Digital Design: finished (I2C and Fast Signals)
  - Local software: finished
  - Custom Board: under manufacturing
  - Human Interface: finished

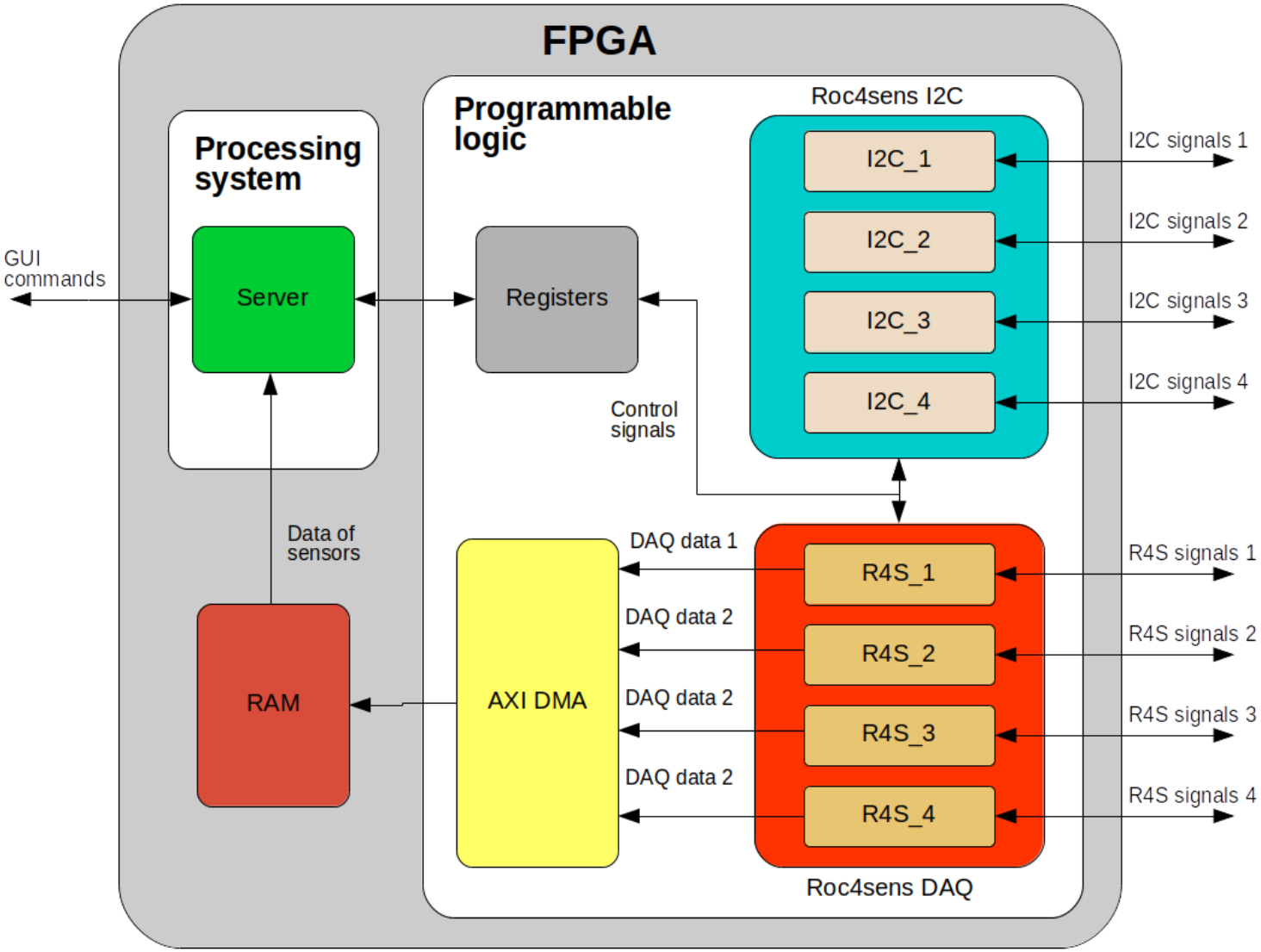

Ultrazed with PinTester Board (June 2018)


Custom Board (with 4 ADCs and 4 Trigger ports, Oct 2018)

DAQ Roc4Sens

- IFCA-USe-PSI joint task
- Up to 4 ROC served by the same DAQ
- No need of local laptop because the system acts like a server
- Drastic simplification of the whole setup (4 ROC4Sens systems served by an unique DAQ-Roc4Sens, no need of local computing)
- Able to manage up to 4 trigger units

Hybrid FPGA: Logical Design Schematics



DAQ Roc4Sens

Hybrid FPGA: Digital Design Signals towards the ROC Roc4Sens

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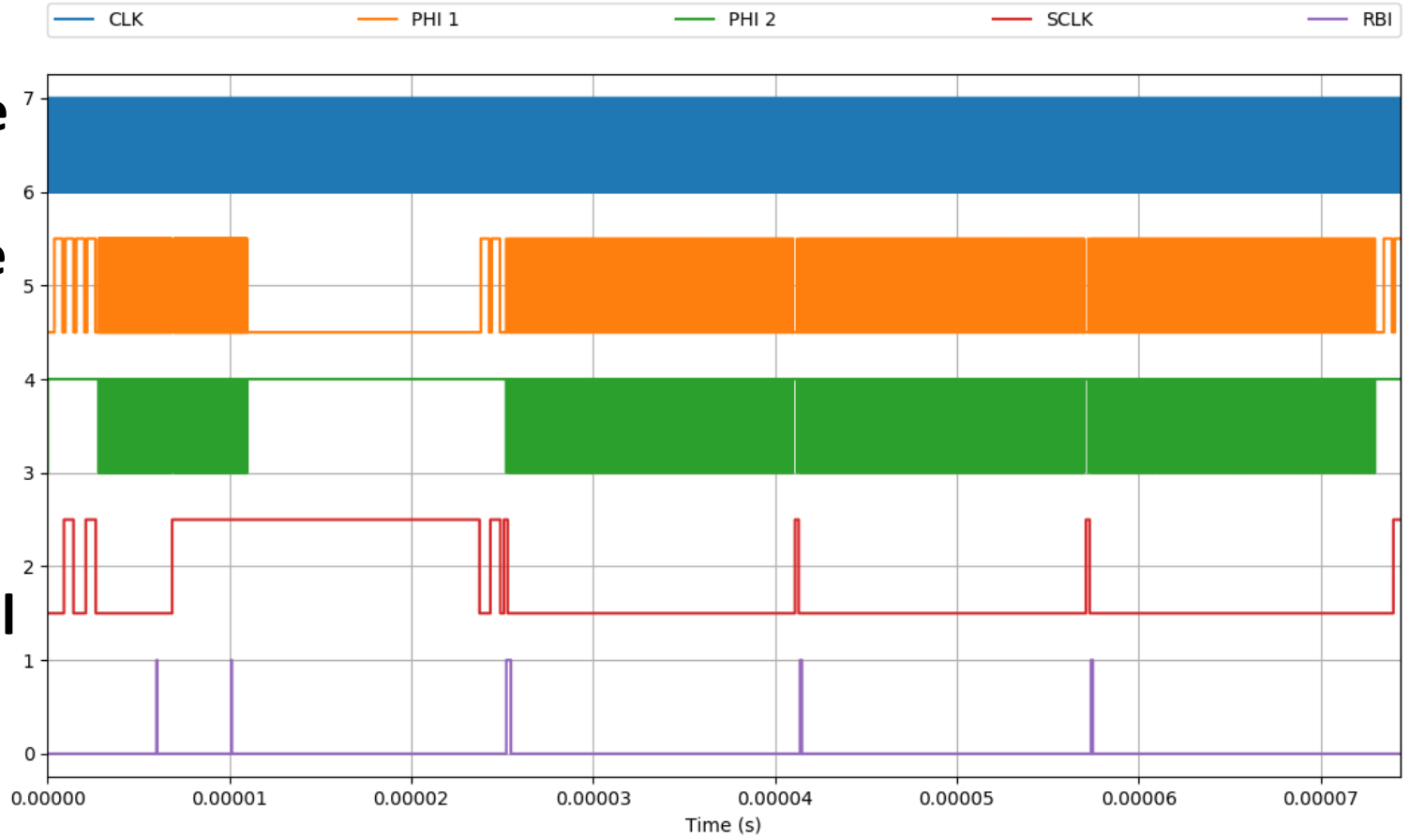

DAQ Roc4Sens

Human Interface (running locally on FPGA)

- IFCA-USe-PSI joint task
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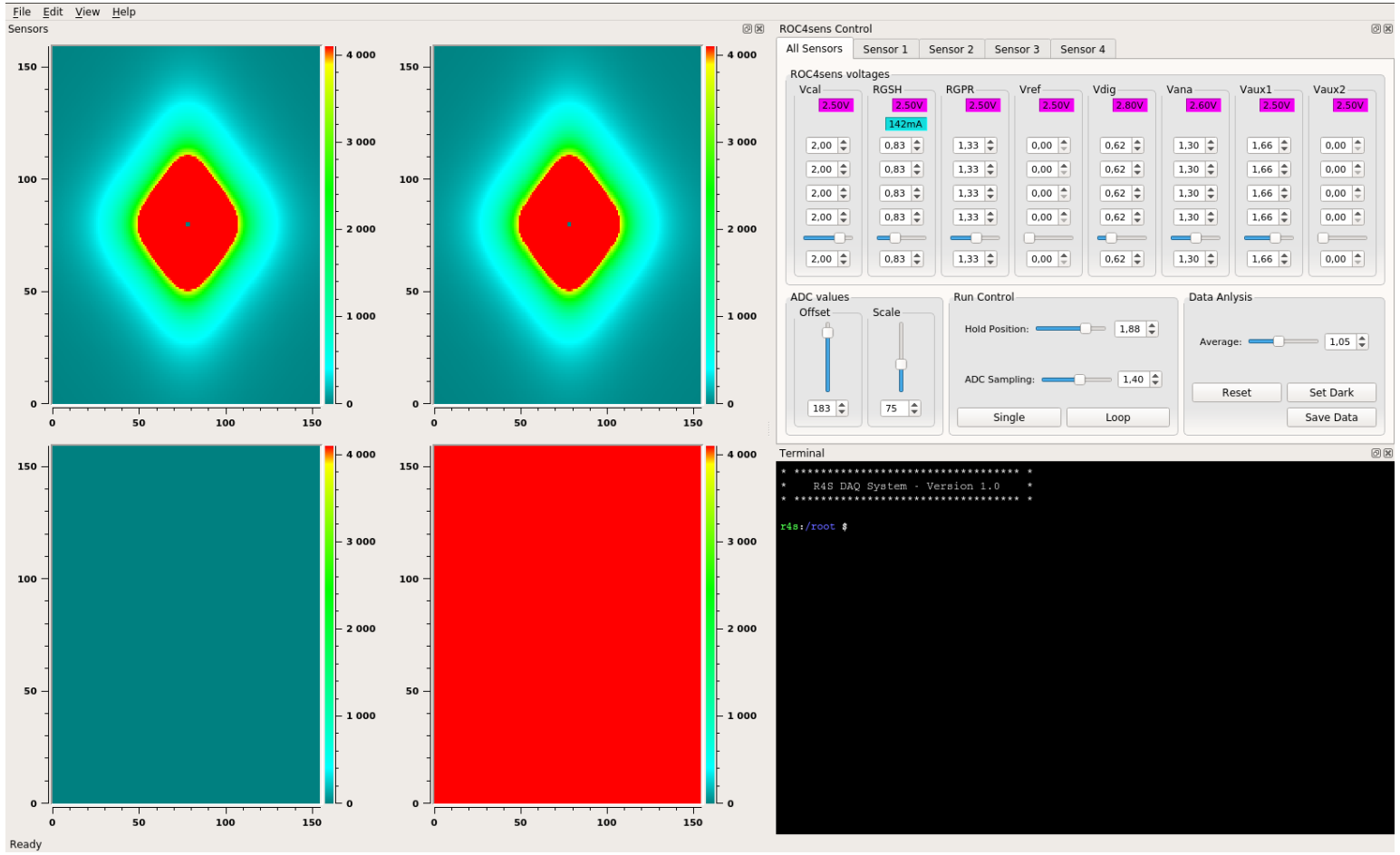

Perspectives

- DAQ-Roc4Sens at 85% of finalization
- Detector simulation activities ongoing (not covered in this presentation)
- Two Photon Absortion Laser activites ongoing (not covered in this presentation)
- mini@sics testing ongoing
- Microelectronic activities ongoing
- DAQ activities ongoing