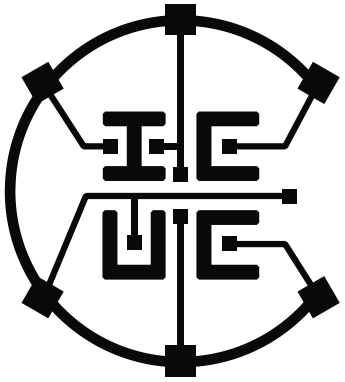

INTEGRATED CIRCUITS UNIVERSIDAD CATÓLICA

Dedicated front-end chip for BeamCal

34th FCAL Collaboration Meeting, March 26-27 2019 @CERN

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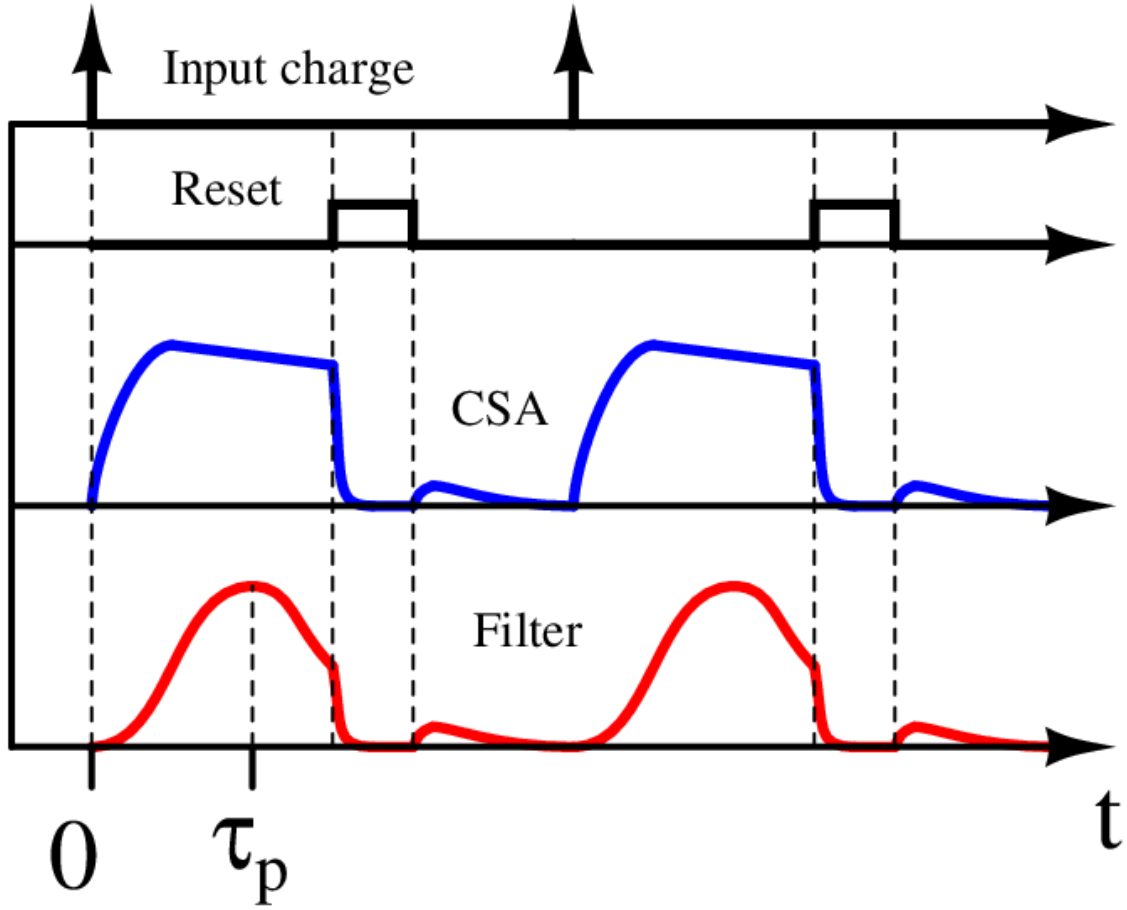
BeamCal front-end chip V3 specifications

Specification	Value
Q_{in}	> 2.8 fC
ENC	< 1000 - 1500 e^- rms
Number of channels	8
Maximum input rate	1 / 554ns
Baseline restoration	1%

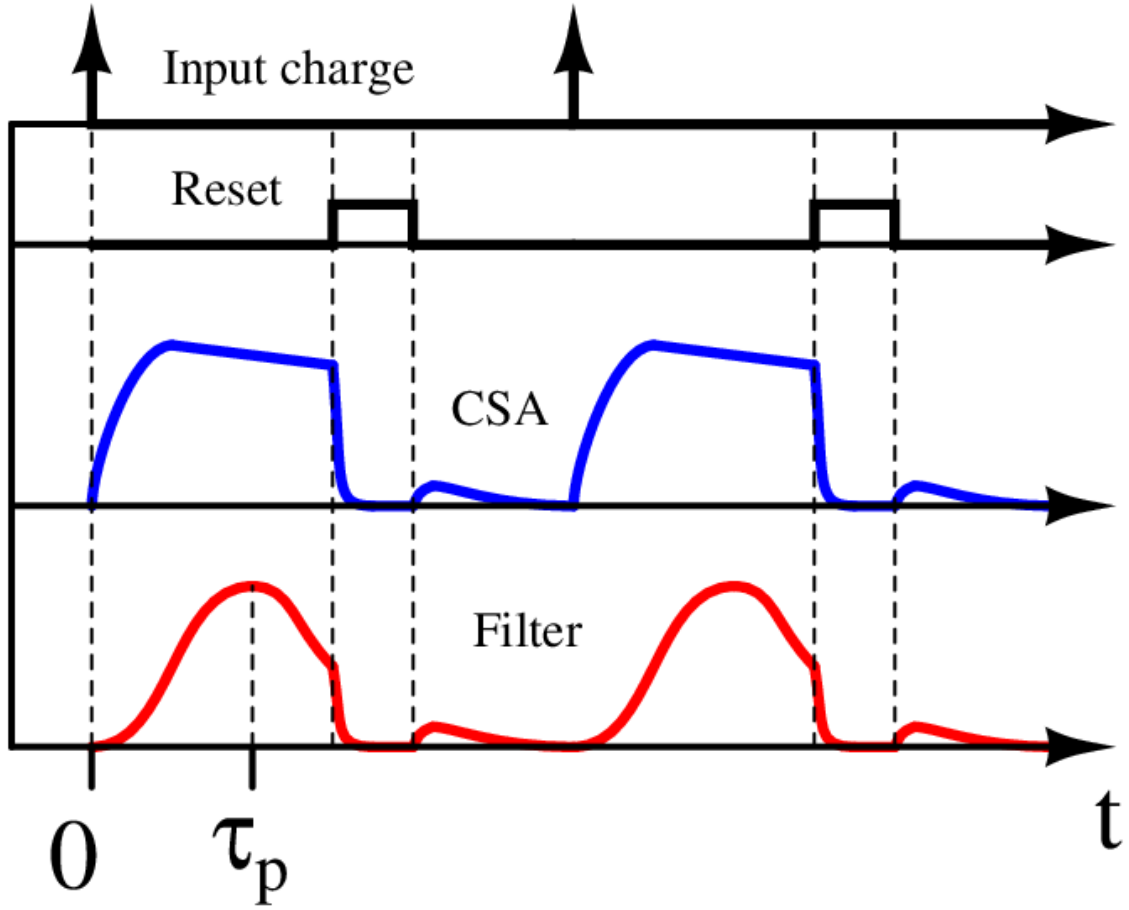
- These specs are intended for **testbeam** purposes only
- Specs for **calibration** and **data taking** will be defined when the sensors are fully defined
  - This ASIC will be a preliminary proof-of-concept

Data taking timing diagram – a reminder



1. CSA gets input charge
2. CSA integrates charge
3. Filter produces semi-gaussian shape
4. After peaking time, both filter and CSA are reset
   a. CSA returns to baseline instantaneously
   b. Filter returns to zero output instantaneously
5. Reset is released
   a. Noise charge is produced and decays due to CSA time constant
   b. Filtered noise charge decays before next input due to filter time constant

Testbeam timing diagram - TBD

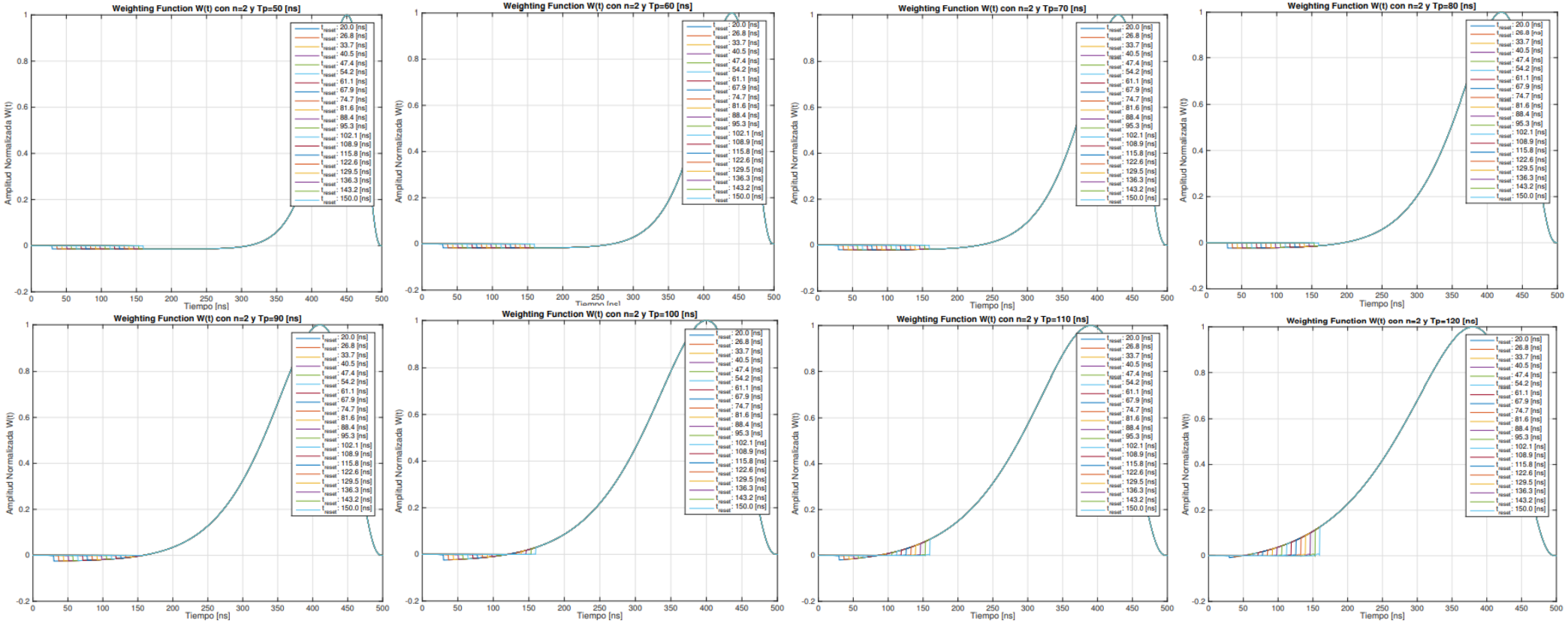


- **Asynchronous** scheme
- Several options:
  - External trigger – may require some work to compensate for trigger delay
  - Fast, external ADC and continuous monitoring
    - Reset still possible to speed up things
  - Deconvolution technique
    - ADC rate requirements are relaxed
  - Peak detector – challenging for such a small (<1-mV) signals

Pulse shaper: why an RC implementation?

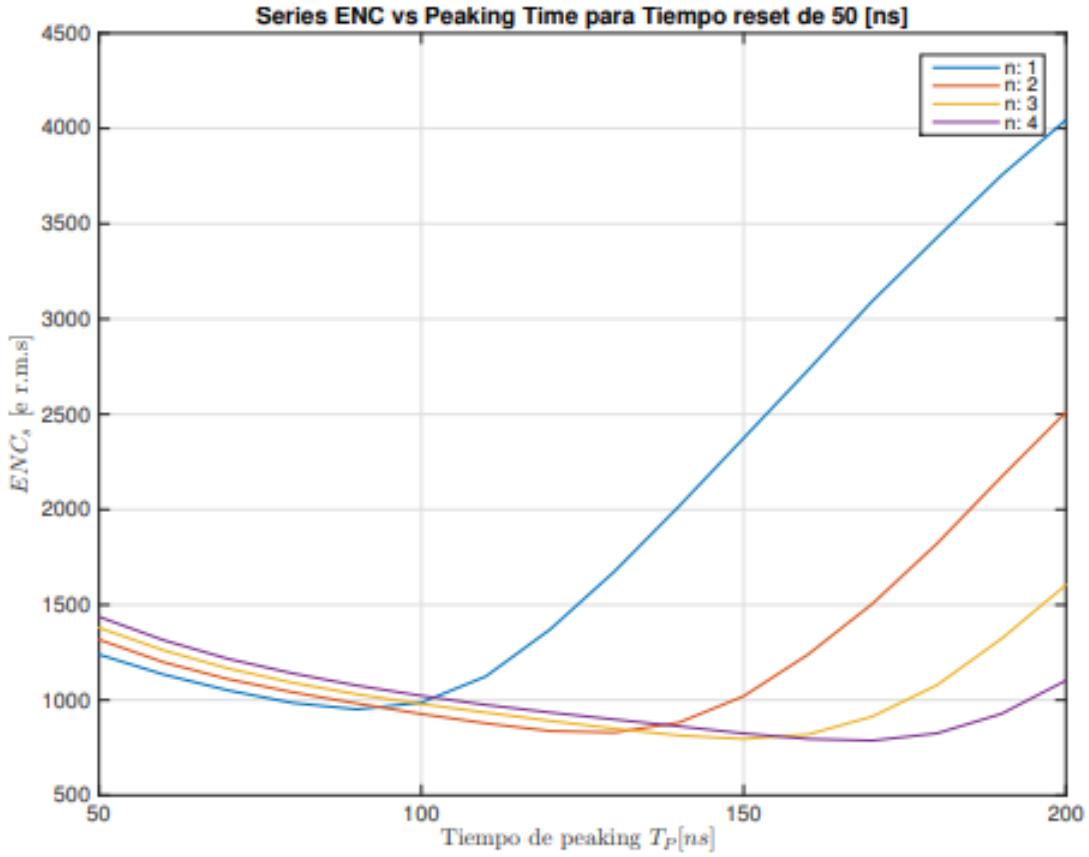
- Suitable for VLSI process
- Better than discrete-time filters for higher bandwidth applications
  - No sampling
  - Smooth weighting function
  - No extra noi
- Lower power than Gm-C option for same specifications
- Tunability will be done in discrete steps

Several behavioral simulations – different filter order (here n=2) and peaking time



Pulse shaper specs (from previous analysis)

- Fully-differential architecture
- 1-V_{pp} output for a 1-V_{pp} input step
- Peaking time in the range 110 ns – 120 ns
- Output integrated noise less or equal than 244 μV_{rms} for a capacitive load of C_L = 0.4 pF
- Standard 180-nm CMOS process



Can reduce this further by increasing CSA current

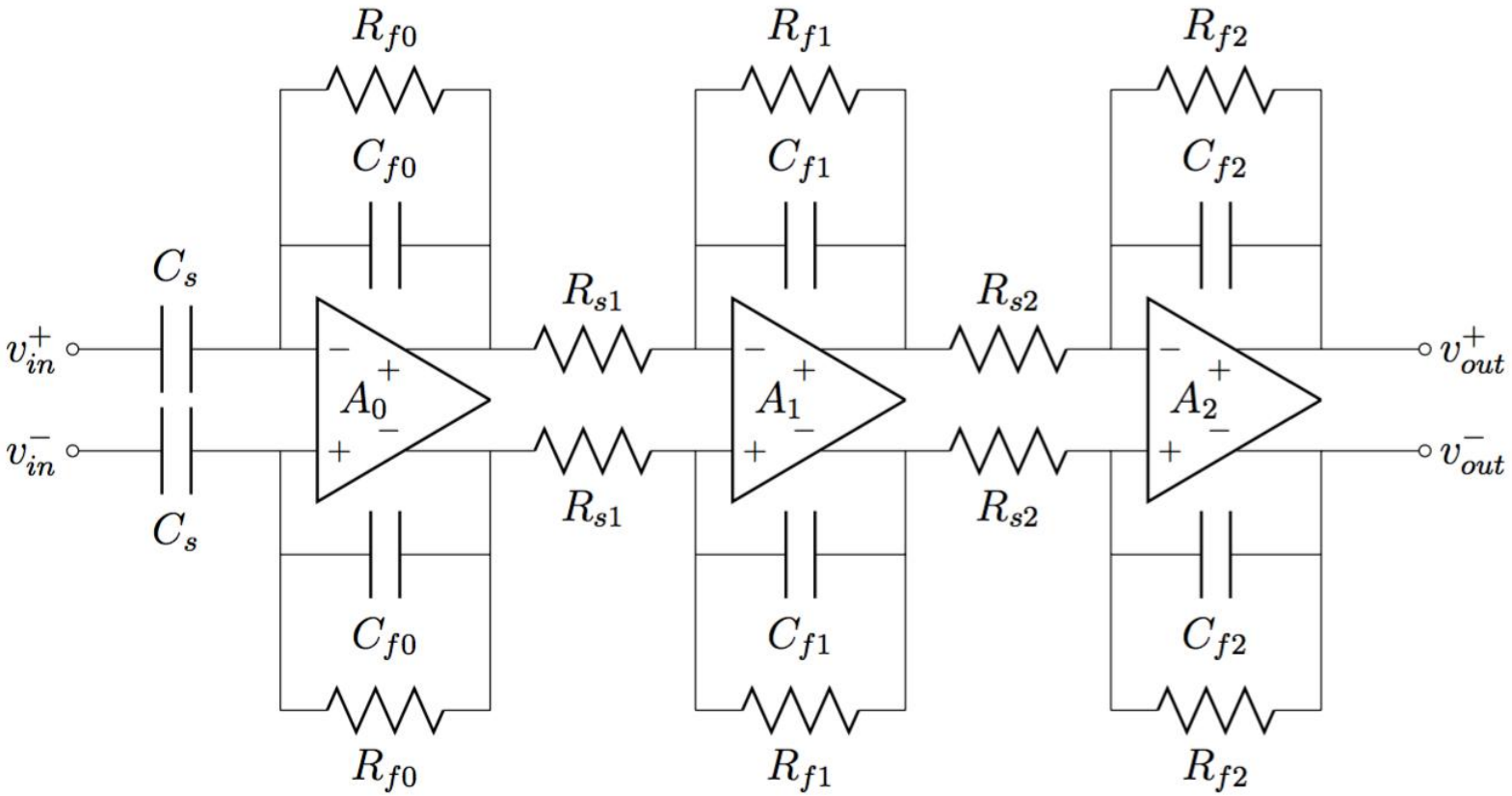
Shaper transfer function

- The shaper transfer function is

$$H(s) = H_0 \cdot \frac{s\tau_d}{1 + s\tau_d} \cdot \frac{1}{(1 + s\tau_i)^2}$$

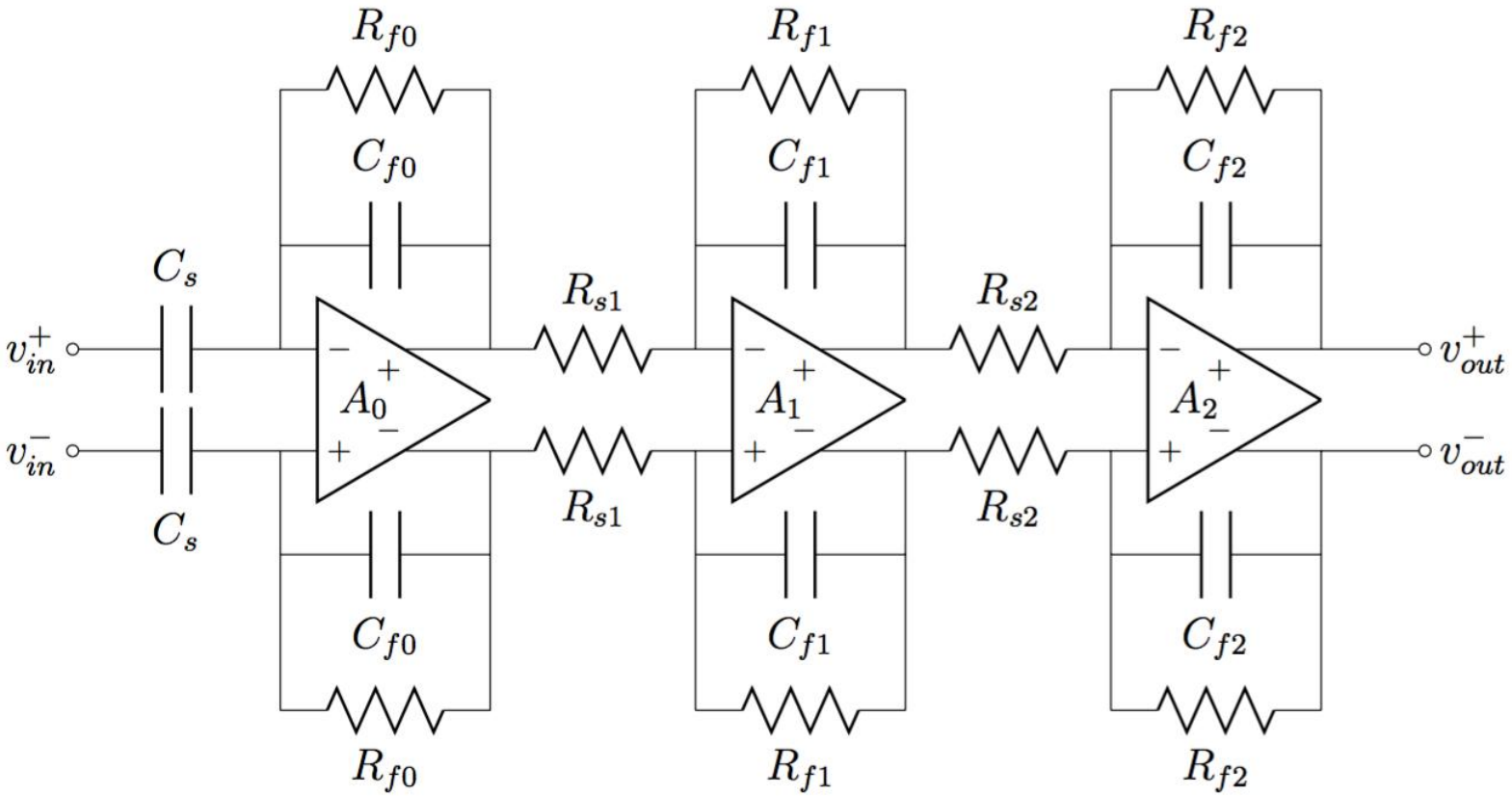
- High-pass time constant τ_d
- Low-pass time constant τ_i
- Passband gain H_0
- We will use $\tau_d = \tau_i = \tau = 50$ ns
  - Some margin left for CSA settling

Filter architecture



- Fully differential
  - SNR, PSRR…
- High-pass on input stage
  - Capacitive input impedance
  - Filter input common mode becomes independent of the CSA baseline

Initial Optimization Procedure



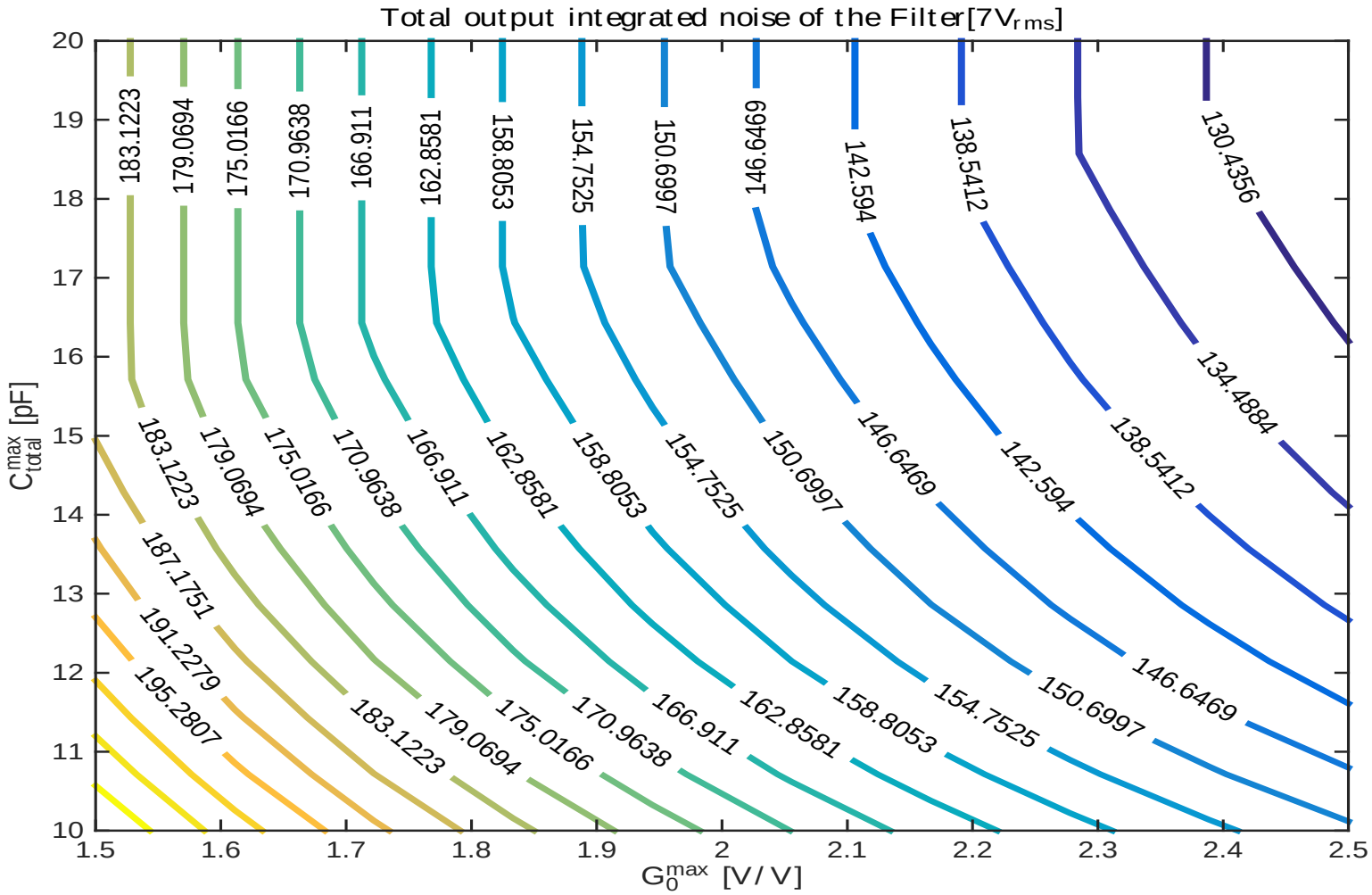
- Resistors and capacitors are carefully chosen – noise considerations
- Amplifier noise can be neglected
  - Their contribution can be reduced by increasing the current

Amplifier optimization formulation

$$\begin{aligned} \text{mín}_{\mathbf{x}} \quad & \overline{v_{no,R}^2}(\mathbf{x}) \\ \text{subject to} \quad & C_{total}(\mathbf{x}) \leq C_{total}^{max}, \\ & G_0(\mathbf{x}) \leq G_0^{max}, \\ & \mathbf{x}_{lb} \leq \mathbf{x} \leq \mathbf{x}_{ub}. \end{aligned}$$

- Filter total integrated noise
- Max cap per channel
- Max gain of 1st stage, set for rail-to-rail output swing to maximize DR (deGeronimo 2011)
- **x** is a vector that includes the amplifier closed-loop gains and resistor values

Noise as function of C_{total}^{max} and G_0^{max}



Opamp or OTA?

- In principle, Opamp deals with resistive loading… but increased power consumption
- Does not matter as long as effective transconductance is large enough (Tsividis, 1994)
- So we go for an OTA (Miller 2-stage)

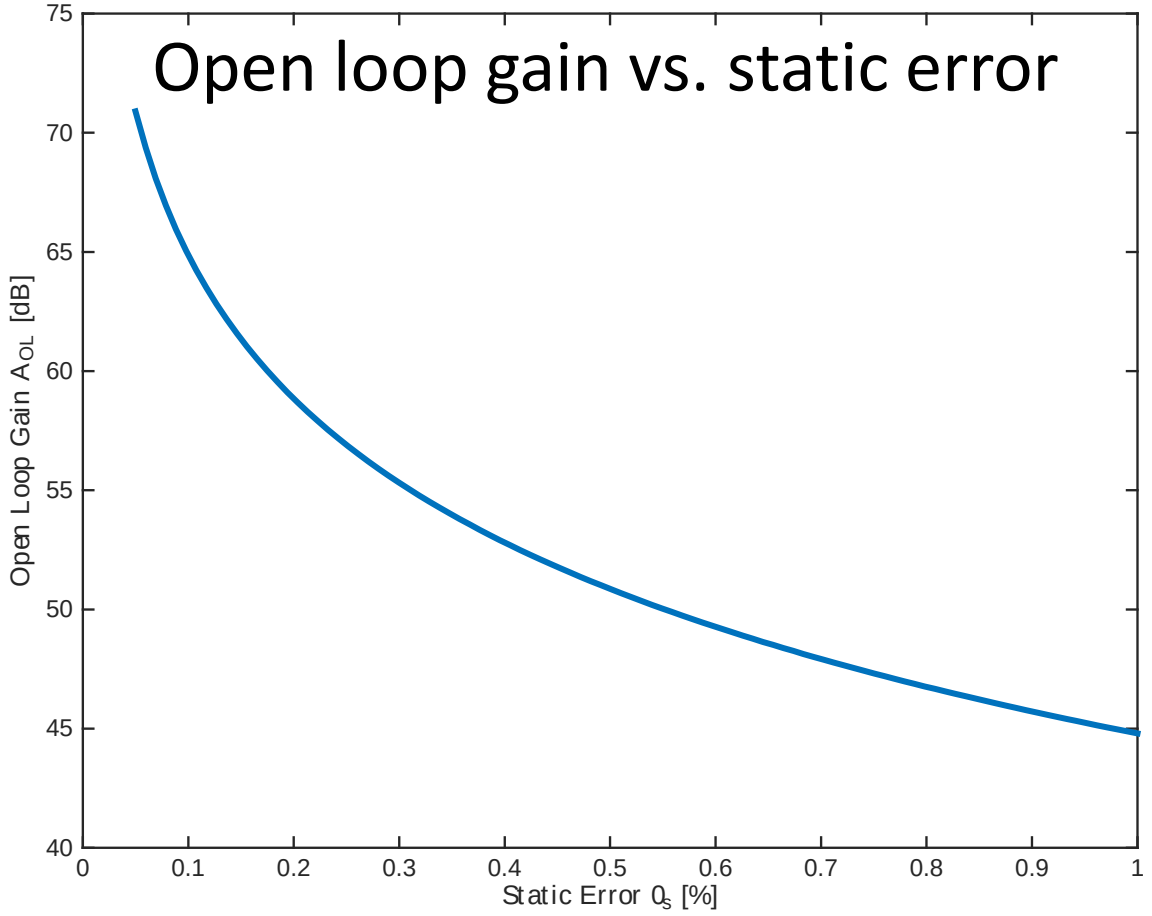
Comparison amplifiers

	I_{TOT} mA	$\overline{dv_{in,eq}^2}$ $\frac{8/3\ kT\ df}{g_{m1}}$		Swing
Volt. OTA (4 Ts)	0.25	4		avg.
Symmetrical (B= 3)	0.33	16		max.
Telescopic	0.25	4		small
Folded casc.	0.5	4		avg.
Miller 2-stage (C_L/C_c= 2.5)	1.1	4	Best	max.

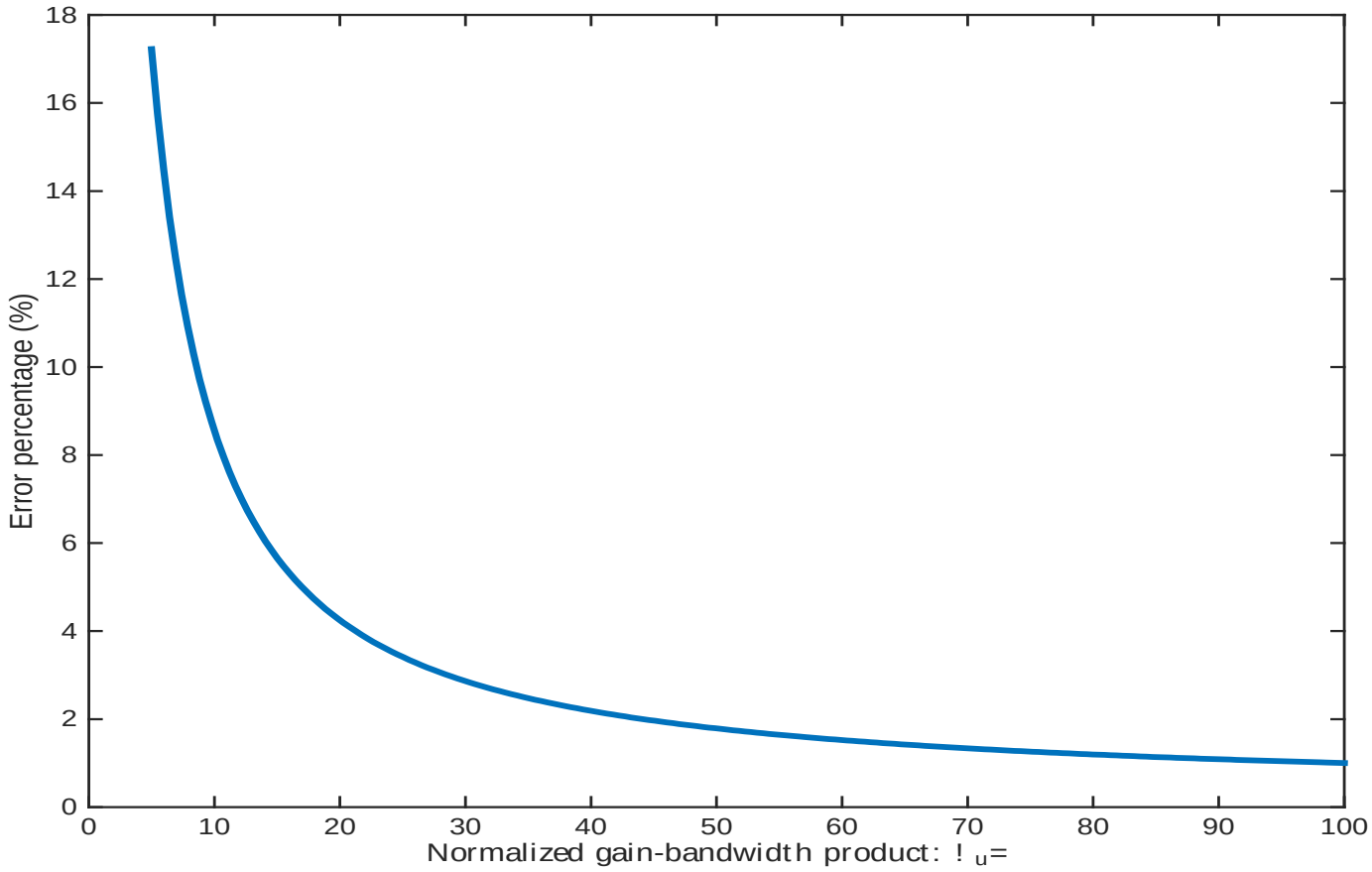
GBW = 100 MHz C_L = 2 pF V_{GS}-V_T = 0.2 V Fully differential

Willy Sansen 10-05 0733

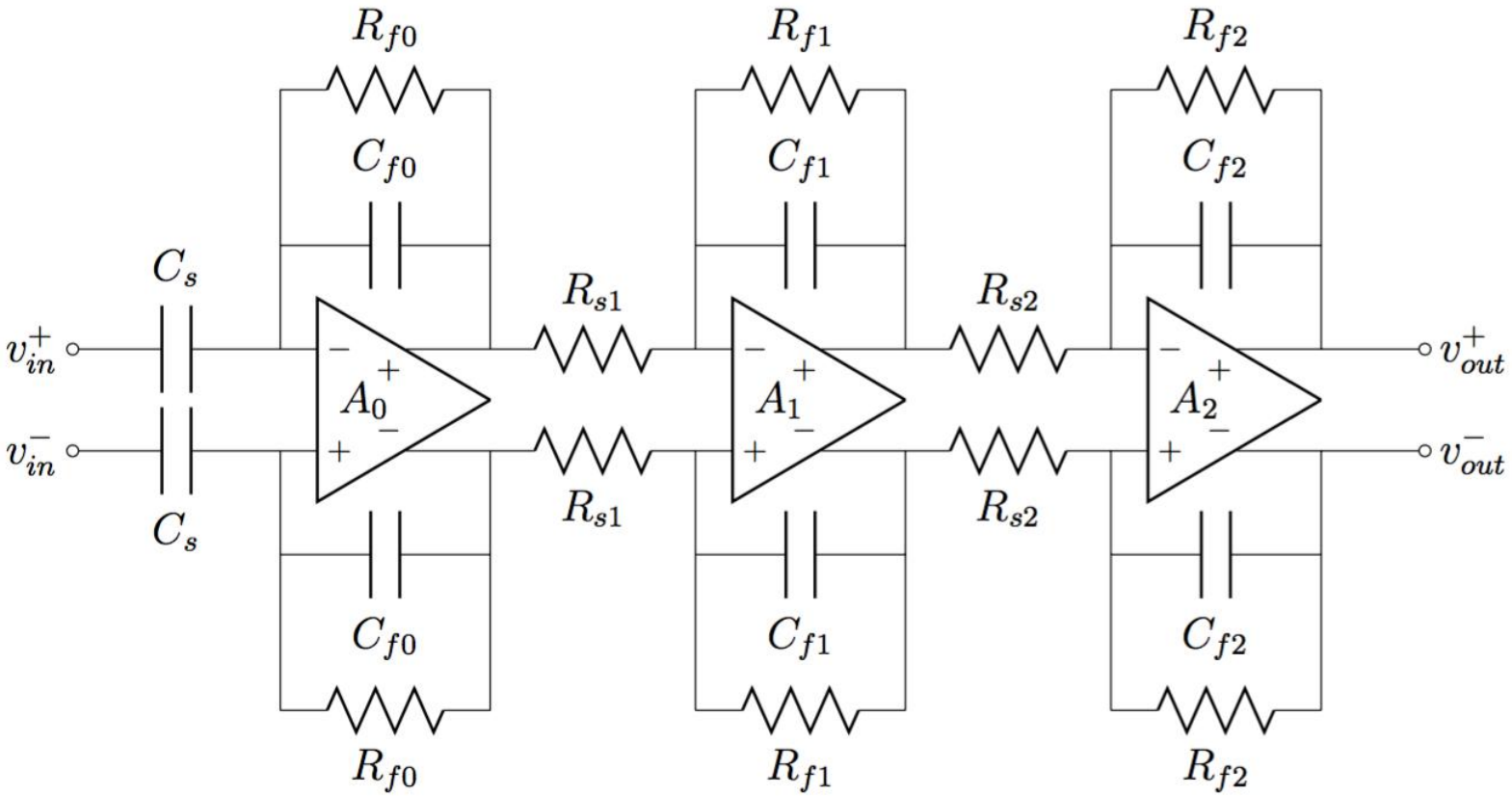
Effect of finite open-loop gain of OTA



Effect of finite OTA bandwidth on 3rd stage



Third stage design is critical



- Final filtering stage
- Therefore, high-frequency poles and zeroes do matter
- This amplifier noise contribution is dominant
  - Can be reduced by increasing Cc

A_2 Input-referred noise

$$\overline{v_{in,Amp}^2}(s) \approx \overline{v_{n1}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{v_{n3}^2} + \frac{(1+s/z_1)^2}{A_1^2} \cdot \left(\overline{v_{n2}^2} + \left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{v_{n4}^2}\right)$$

- Valid for frequencies below GBW
- z_1 < GBW in output impedance expression due to C_1 + C_c
- Noise contribution becomes significant
- z_1 should be pushed towards the GBW by reducing C_1
- Min-length transistor in 2nd stage transconductor to reduce C_1
- 1st stage in moderate inversion to ensure high gain
- C_c as large as possible – here fixed to 2.5 pF

A_2 amplifier design

Specification	Expected value (MATLAB)	LTSpice
A_{OL}	>60dB	62.78dB
GBW	112.65MHz	100MHz
I_{D1}	$148.81\mu A$	$151.12\mu A$
I_{D2}	$274.42\mu A$	$277.06\mu A$
PM	70°	73°
τ	52.5 ns	52.53 ns
$\overline{v_{no,Amp}^2}$	$102.79\mu V_{rms}$	$142.5\mu V_{rms}$

Comparative table between simulation results and expected values from MATLAB, for designed amplifier A_2.

A_1 amplifier design

Specification	Expected value (MATLAB)	LTSpice
A_{OL}	$\geq$62dB	61.99dB
GBW	112.65MHz	118.4MHz
I_{D1}	25.62μA	27.11μA
I_{D2}	179.73μA	177.2μA
PM	$\geq 62°$	66,26°
τ	52.9 ns	54.5 ns

Comparative table between simulation results and expected values from MATLAB, for designed amplifier A_1.

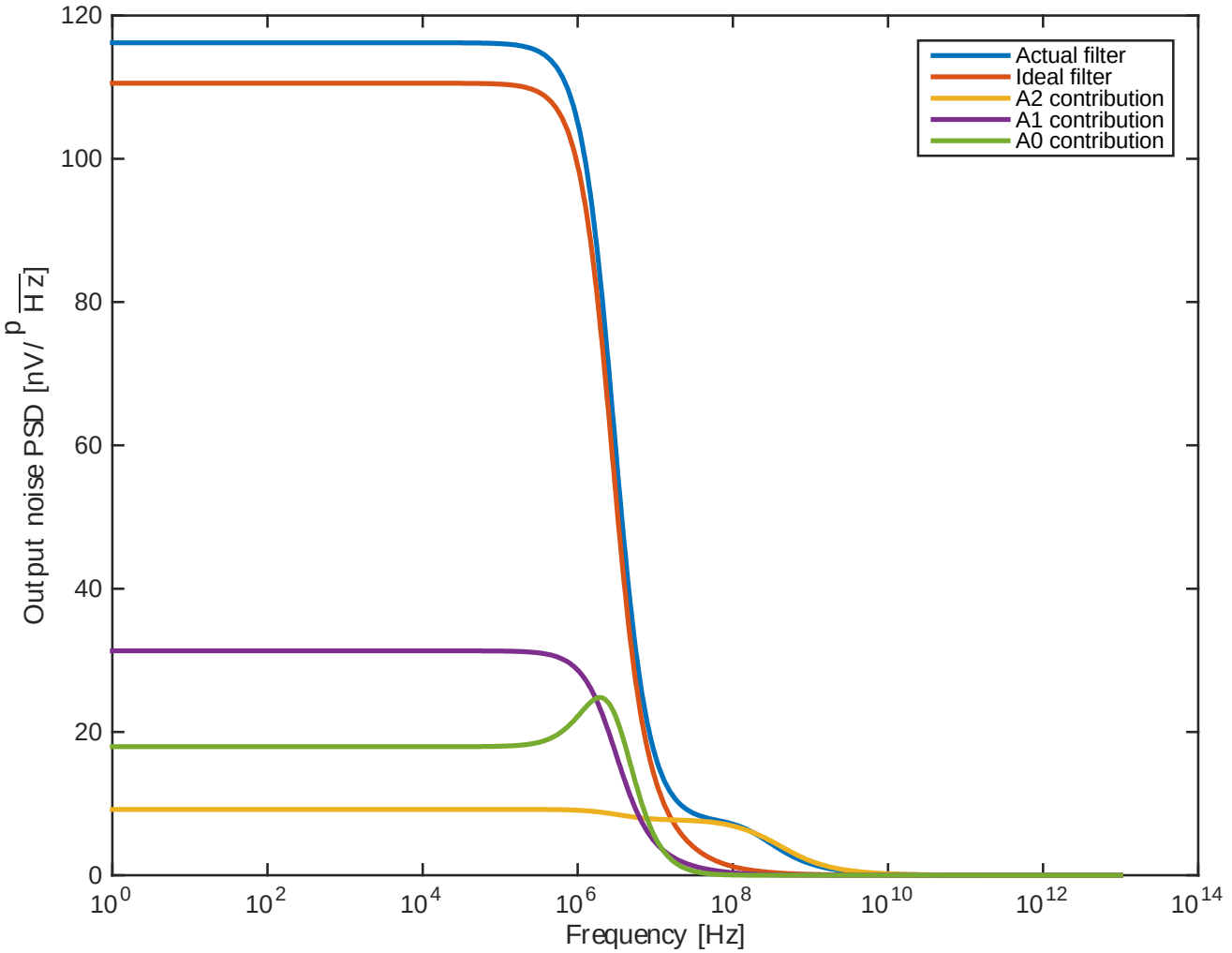
A_0 amplifier design

- In highpass configuration
  - Maximize GBW
- Derivative function
  - High slew rate

Specification	Expected value (MATLAB)	LTSpice
A_{OL}	$\geq$65dB	64.17dB
GBW	160MHz	146.1MHz
I_{D1}	$75\mu A$	$76.04\mu A$
I_{D2}	$224.08\mu A$	$226.33\mu A$
PM	$\geq 70°$	87°
τ	53.4 ns	57 ns
ϵ_s	6.32 %	7.14 %

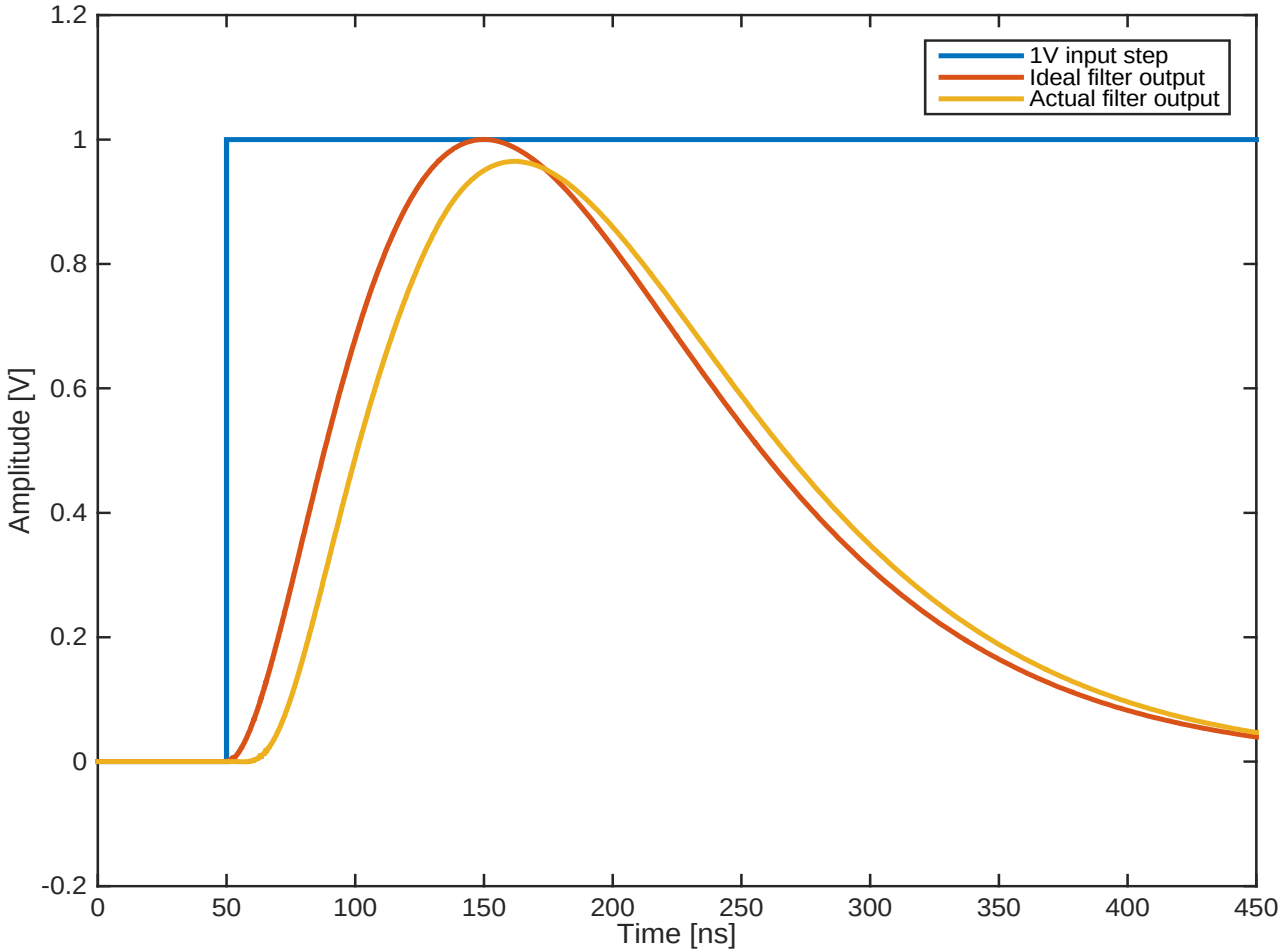
Comparative table between simulation results and expected values from MATLAB, for designed amplifier A_0.

Amp noise contribution – simulation results



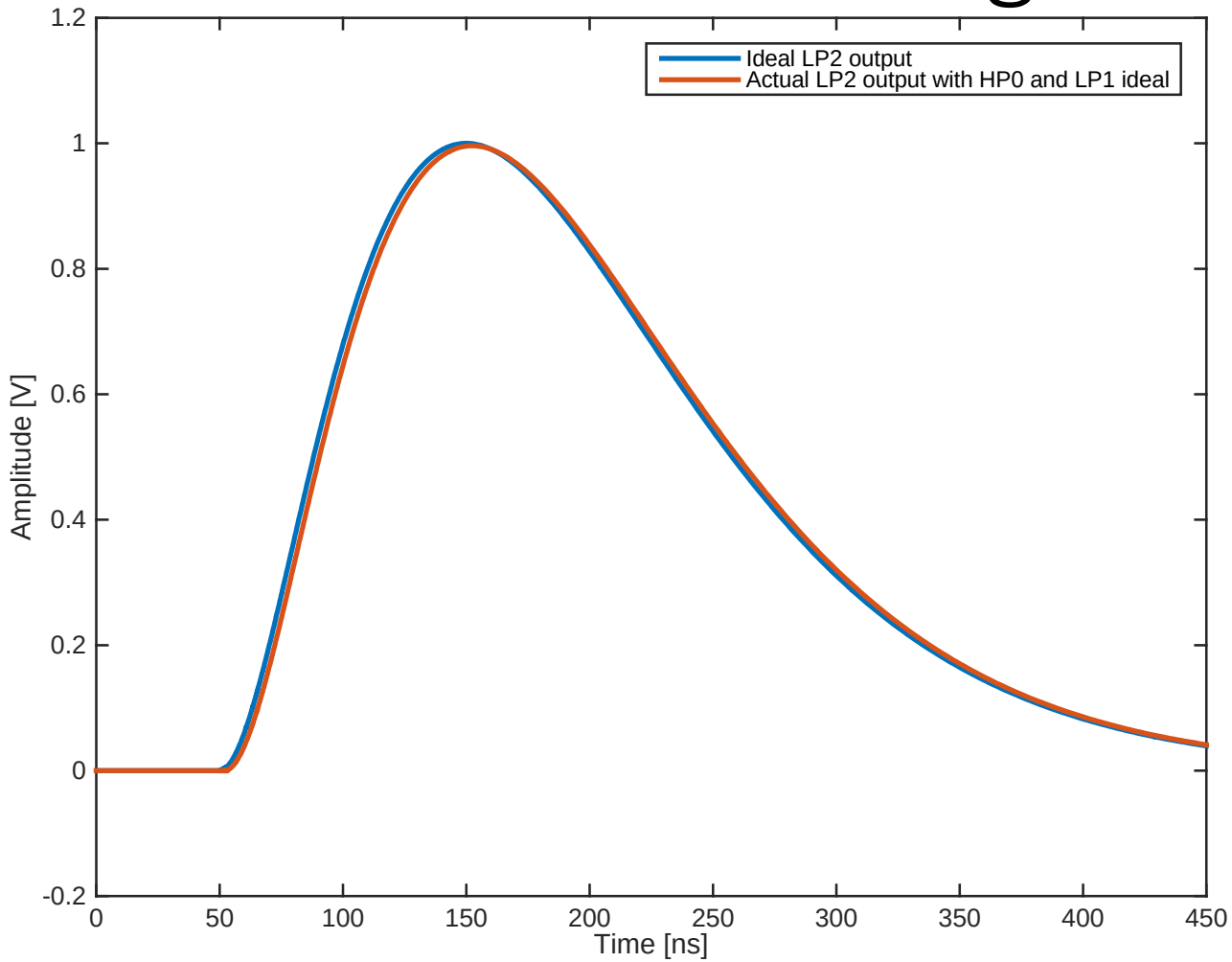
.noise simulation on LTSpice of actual filter, ideal filter and active devices contributions

Transient simulation results



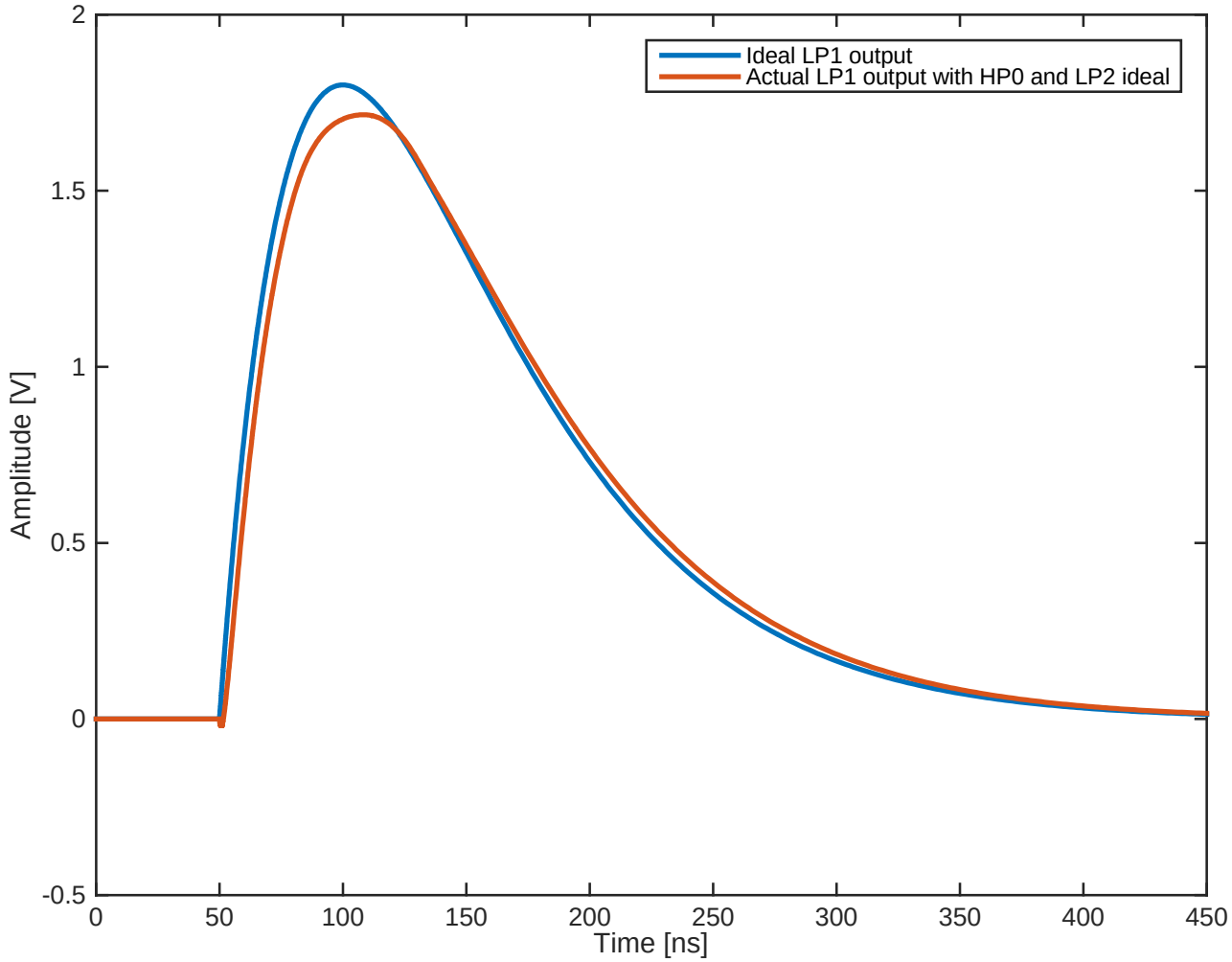
.tran simulation on LTSpice of actual filter, ideal filter and input step applied

Transient simulation – third stage output



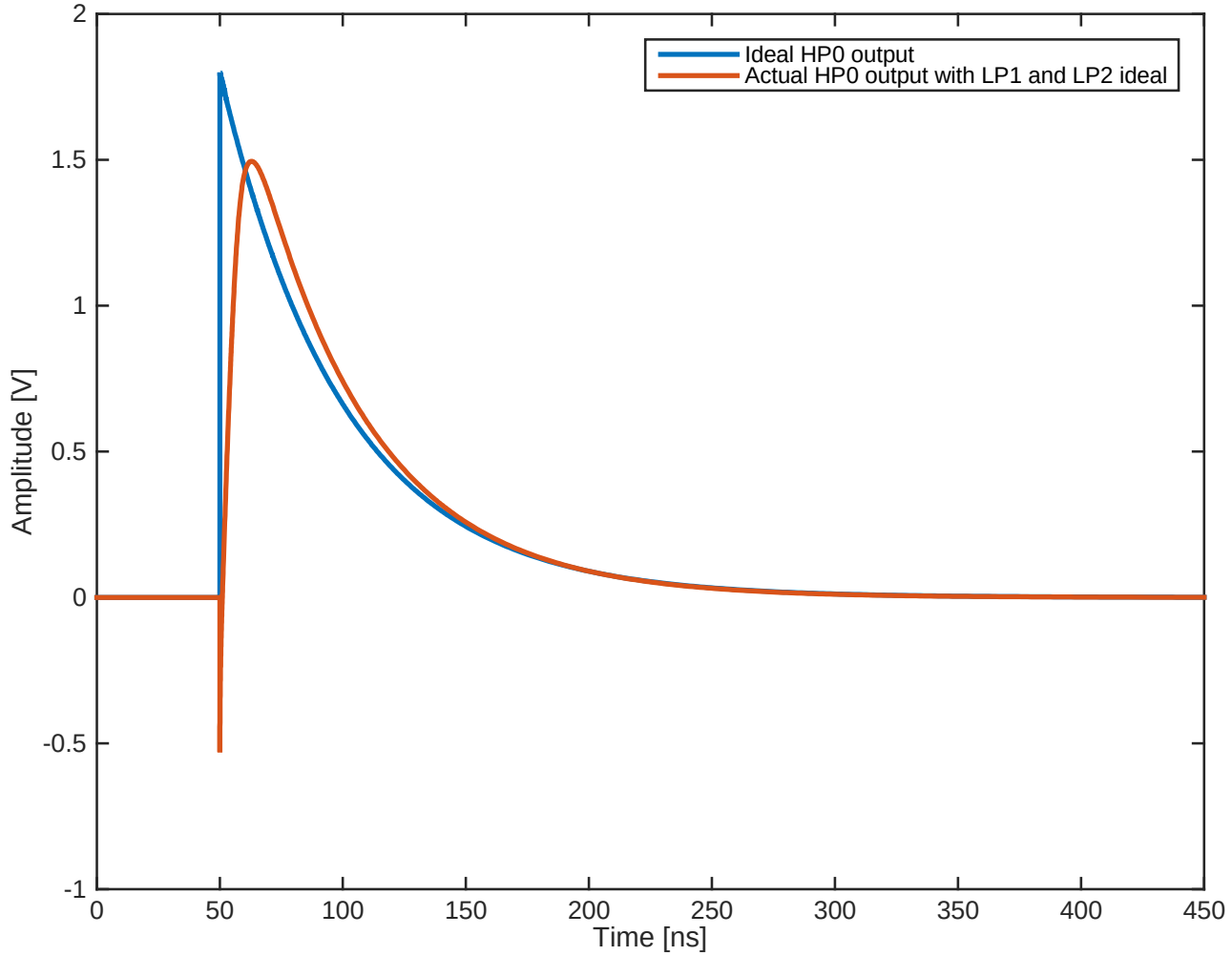
.tran simulation on LTSpice of third stage compared to ideal third stage when **first and second stages are ideal**

Transient simulation – second stage output



.tran simulation on LTSpice of second stage compared to ideal second stage when **first and third stages are ideal**

Transient simulation – first stage output



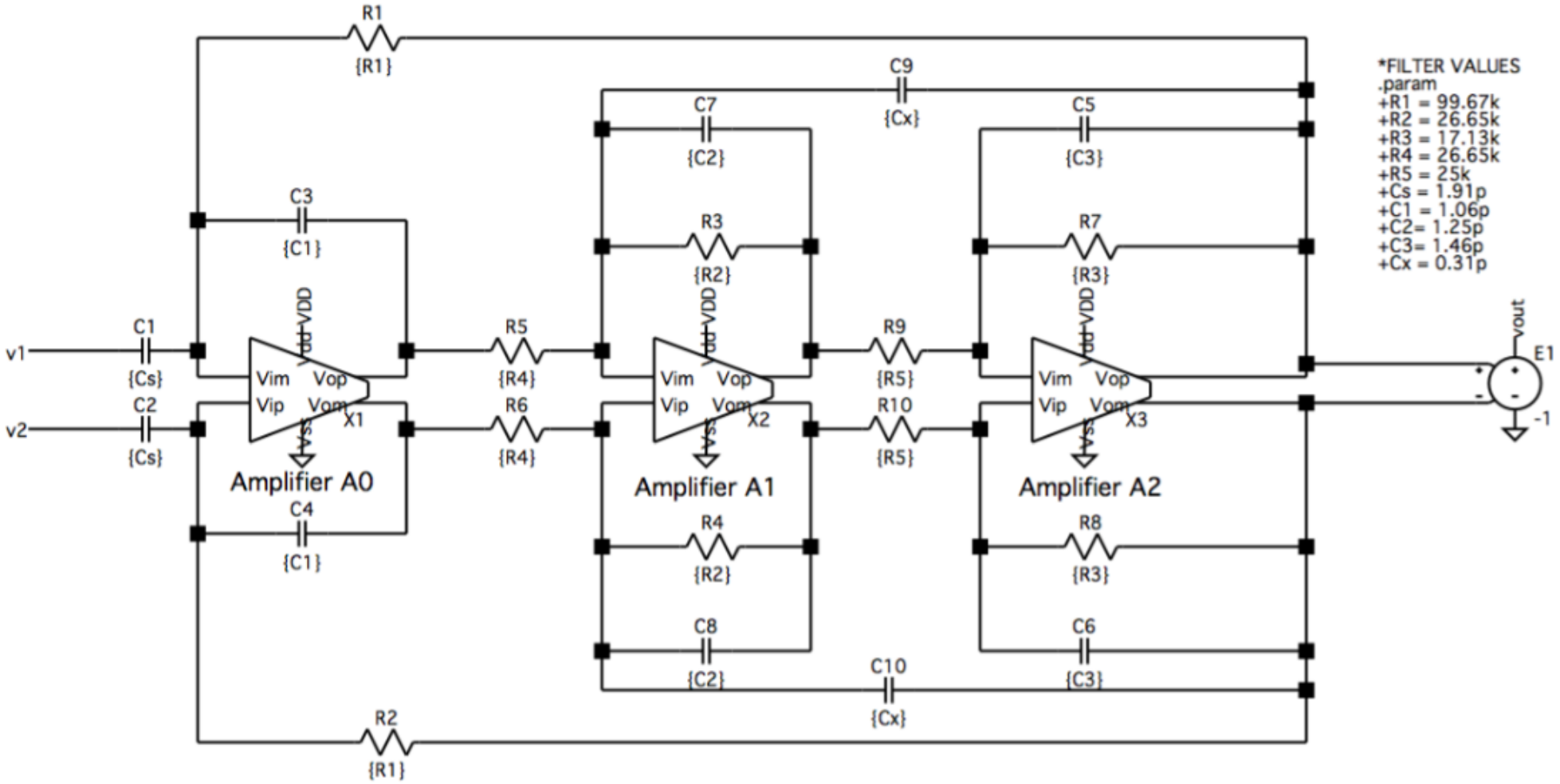
.tran simulation on LTSpice of first stage compared to ideal first stage when **second and third stages are ideal**

Current status and future milestones

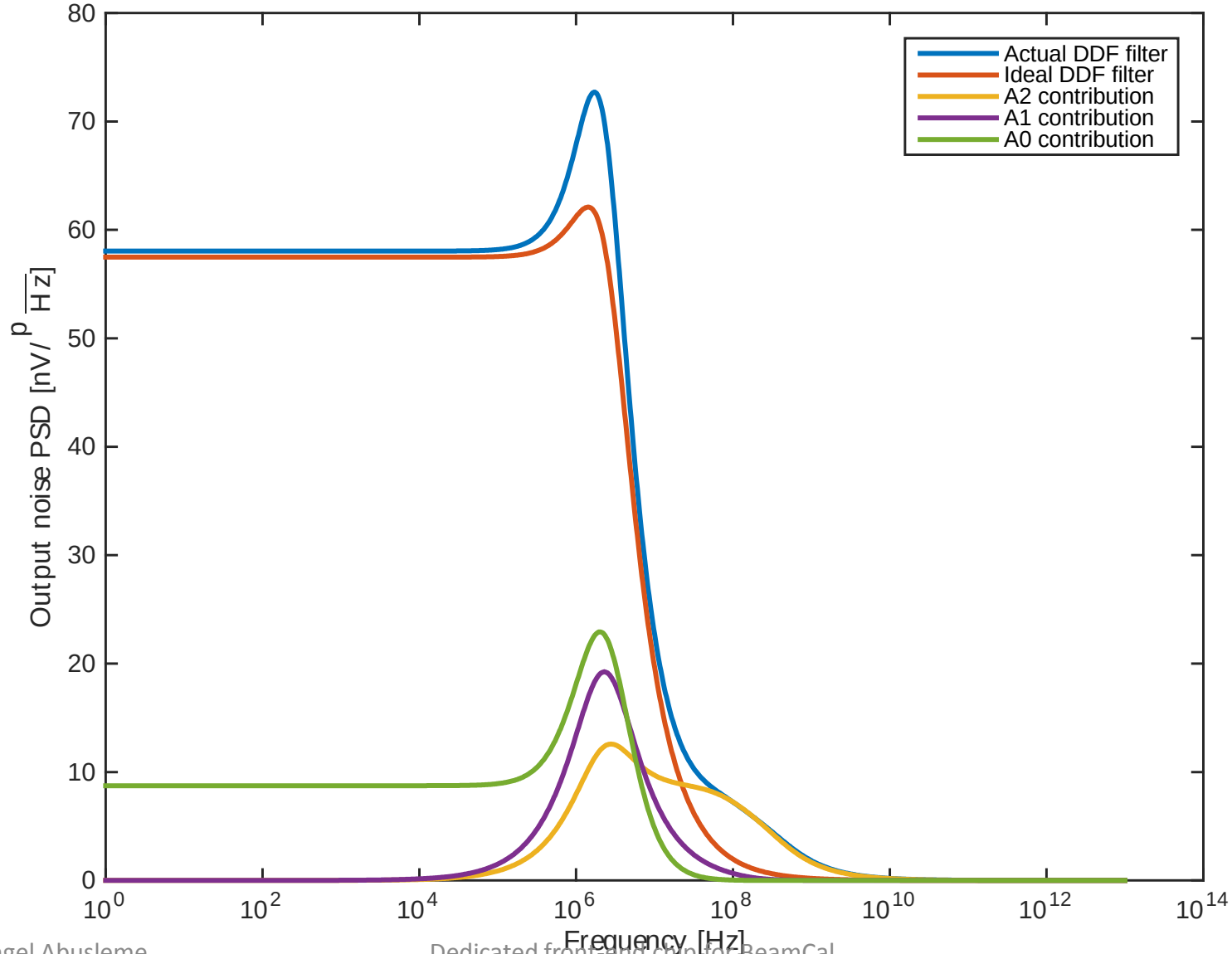
- Filter circuit-level design is complete
- Several ideas were considered and discarded
  - Gm-C filter, Dissipative delayed feedback, discrete time…
- Now fully working on layout
- Tapeout scheduled for May 29th
- Board design and testing in June-July
- Chip testing August-November

Thanks for your attention

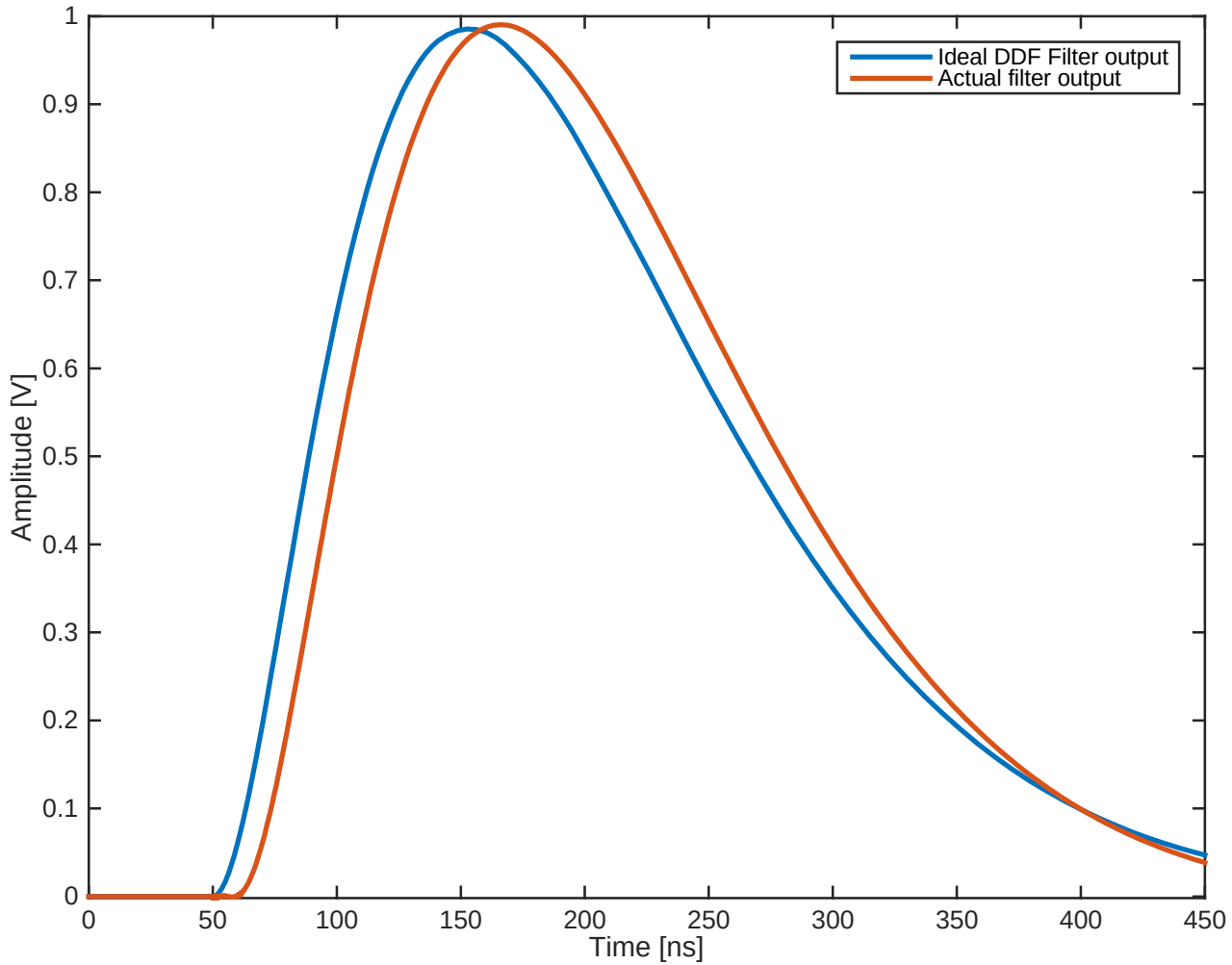
DDF: Dissipative Delayed Feedback (DeGeronimo, 2011)



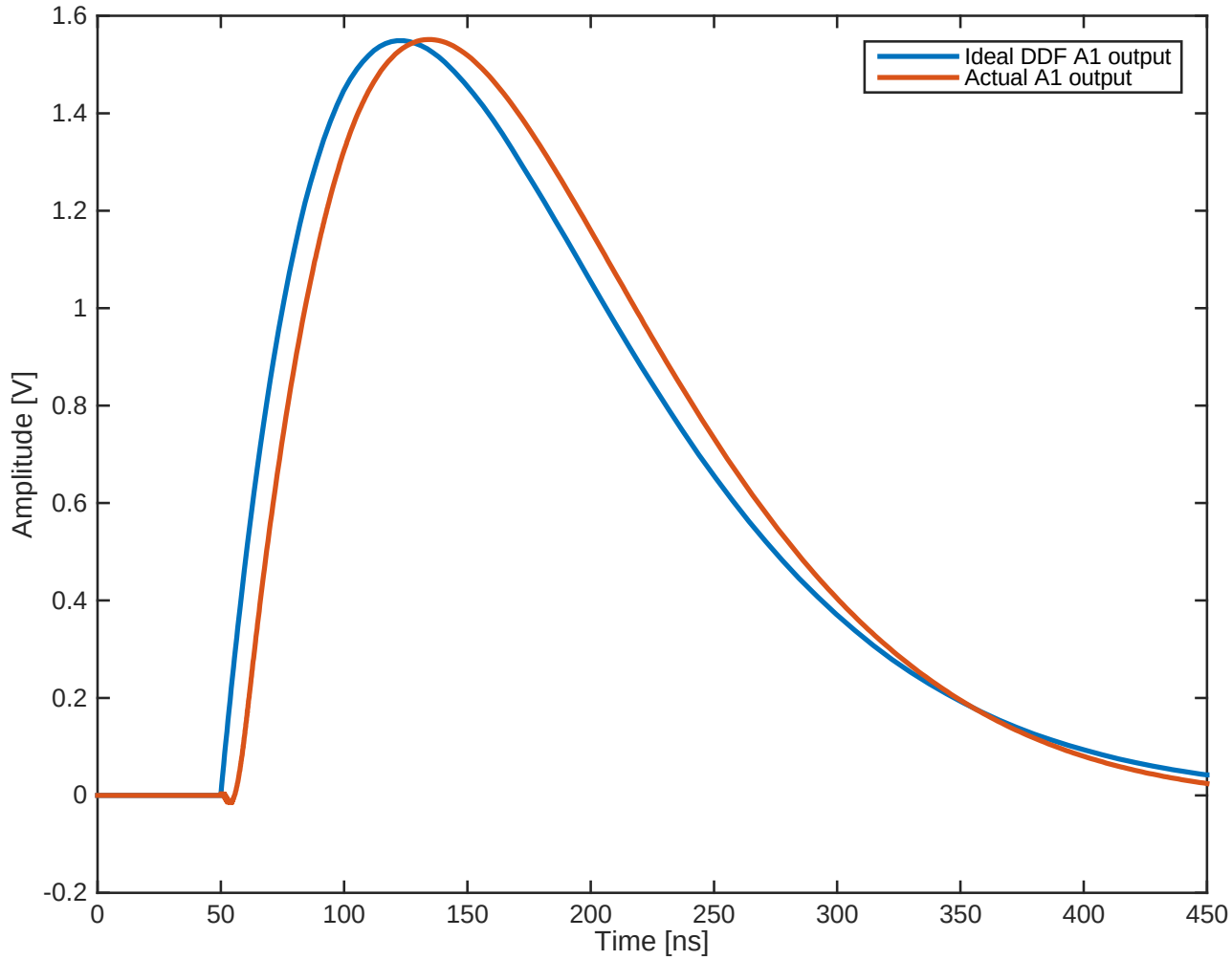
DDF: Noise simulations



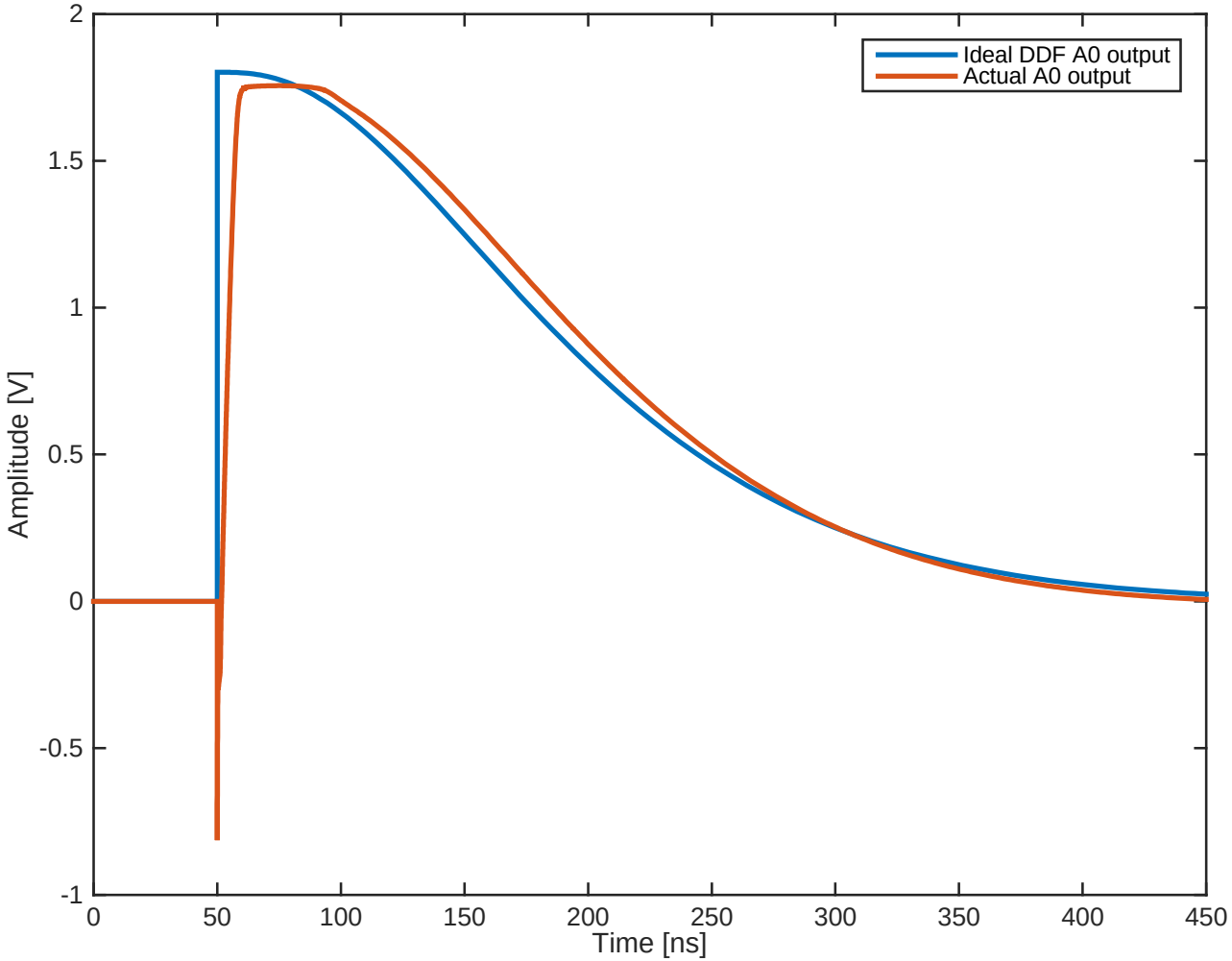
DDF - Transient Simulations – Filter's output



DDF - Transient Simulations – A1's output



DDF - Transient Simulations – A0's output



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