Highlights from TWEPP 2018 conference

TWEPP-18
Topical Workshop on Electronics for Particle Physics
Antwerp, Belgium, 17 – 21 September, 2018
Outline

- Brief overview about the conference
- Summary of some presentations
  - The BRAVE FPGAs: overview and status of the European radiation-hardened FPGAs for space
  - Evaluating the NanoXplore 65nm SRAM based RadHard FPGA for CERN applications
  - Technology and challenges for extreme ultraviolet lithography
  - The CMS High Granularity Calorimeter for HL-LHC
  - SAMPIC-based systems for precise timing detectors: implementation and performance
  - The proton timing system of the TOTEM experiment
  - Radiation tolerance enhancement of silicon photonics for HEP applications
  - Next generation of radiation tolerant Single-Mode Optical Links for Accelerator Instrumentation
- Additional topics
Conference overview

General information:
• Hold annually since 1995
• Covers “all aspects of electronics for particle physics experiments, and accelerator instrumentation of general interest to users”
• Particular focus on LHC experiments

Purpose:
• Present results and original concepts for electronic research and development relevant to experiments as well as accelerator and beam instrumentation at future facilities
• Review the status of electronics for the LHC experiments
• Identify and encourage common efforts for the development of electronics
• Promote information exchange and collaboration in the relevant engineering and physics communities.

Practical information:
• Website: https://indico.cern.ch/event/697988
• Papers will be published in “Proceedings of Science”: https://pos.sissa.it
• Duration: 4.5 days with plenary + 2 parallel sessions + 2 tutorials
• 183 paper submissions, 60 oral presentations & 100 posters

Statistics

TWEPP Participants

Highest ever!
Project collaboration between ESA, CNES with industrial partners (NanoXplore and STMicroelectronics) to develop a range of rad-hard, SRAM-based and ITAR and EAR-free (= no dependant of US regulations) FPGAs.

Important project for ESA since there ~200 FPGAs per satellite.

**BRAVE** = Big Re-programmable Array for Versatile Environments

3 rad-hard device families are planned: with increasing fabric size and number of logic resources.

<table>
<thead>
<tr>
<th>NG-Medium</th>
<th>NG-Large</th>
<th>NG-Ultra</th>
</tr>
</thead>
<tbody>
<tr>
<td>STMicroelectronics' rad-hard 65 nm process (STM C65)</td>
<td>STM C65</td>
<td>28 nm FD-SOI process</td>
</tr>
<tr>
<td>2 packages currently available: a 625-pin, 29x29 mm LGA, and a 352-pin, 48x48 mm MQFP</td>
<td>packaged in a 1752-pin LGA/CGA</td>
<td>packaged in a 1752-pin LGA/CGA</td>
</tr>
<tr>
<td>35k LUTs, 2.8 Mb of embedded RAM</td>
<td>140k LUTs, 10.1 Mb of embedded RAM,</td>
<td>600k LUTs, 32 Mb of embedded RAM</td>
</tr>
<tr>
<td>• 4x PLL, 13 I/O banks</td>
<td>• 24x 6.25 Gbps high-speed serial links</td>
<td>• The target logic and DSP performance is 500 and 800 MHz respectively</td>
</tr>
<tr>
<td>• 1x 430 Mbps SpaceWire CODEC and</td>
<td>• 1x 400 Mbps SpaceWire interface</td>
<td>• 1 Gbps differential I/O</td>
</tr>
<tr>
<td>• 112 DSP blocks</td>
<td>• Embedded DSP blocks</td>
<td>• 12.5 Gbps SERDES links</td>
</tr>
<tr>
<td>• 16 SW PHY</td>
<td>• A rad-hard ARM Cortex-R5x core</td>
<td>• 600 MHz quad-core ARM R52.</td>
</tr>
<tr>
<td>Already available</td>
<td>• 24 I/O banks.</td>
<td></td>
</tr>
<tr>
<td>First parts available in Q3 of this year</td>
<td></td>
<td>Slightly less total dose tolerance than the large (&gt;50kRad )</td>
</tr>
<tr>
<td>First parts available towards the end of 2020</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NG** = **N**-Medium, **NG** = **N**-Large, **NG** = **N**-Ultra
Radiation Hardened by Design (RHBD) and simulated TFIT software 
TID >300 krad TID
No SEL for LETth > 60 MeV cm$^{-2}$/mg
SER / device.day : 1.7e-4 (GEO).

Diff. harden techniques : TMR for logic cells, DMR for clock tree, 
DICE for configuration Memory and EDAC for register file +
embedded Configuration Memory Integrity Check (CMIC)

CMIC (Configuration Memory Integrity Check) :
On initialization, a bit stream reference is saved into a memory
protected by ECC. 
CMIC can be periodically activated (period can be set by the user
between 5.3ms-65days):
1. Reads the configuration data (~4ms)
2. Calculates the signature
3. Compares the result with the signature of the CMIC reference.
4. If mismatch is detected it can correct it.

Note: Tested up to 300krads TID (ESA qualifies up to 100krads).
NG-medium specs

### Performance
- Logic: 200 MHz
- DSP: 333 MHz
- I/O: 800 Mbps

### Evaluation board
Evaluation board for NG-medium available. To be used interactively through JTAG or standalone from an EEPROM board (Atmel Dump Model EEPROM or a standard SPI EEPROM).
(NG-medium Eval kit ~3.2k€)

NanoXPython: Python wrappers scripts for making the different steps: synthesis, P&R, etc.
They provide an embedded logic analyser IP core (VHDL)
The BRAVE FPGAs: overview and status of the European radiation-hardened FPGAs for space. (5/5)

Current market

1. **Microsemi**: RTAX2000, Antifuse, 150nm, ~35k LUT4, 50MHz.
2. **RT Proasic3**: Flash, 130nm, ~35k LUT4, more configurable, ~50 MHz
3. **Xilinx**: V4QV, RadTolerant, 90nm, obliged to triplicate, so similar resources to previous after triplication.
4. **Xilinx**: V5QV, 65nm, ~60-80k€
5. **Microsemi**: RTG4, ~150k LUT4, ~150MHz, 60-70k€ (space qualified)
6. **NanoXplore**: NG-medium, RHBD 65nm, ~35k LUT4, 150MHz
7. **NanoXplore**: Future NG-Large, RHBD 65nm, 140k LUT4
8. **NanoXplore**: Future NG-Ultra, RHBD 28nm.

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**NanoXplore Rad-Hard FPGA Roadmap**

- **2017**: 65nm
- **2018**: 65nm
- **2019**: 65nm
- **2019**: 28nm

- **Low-End FPGA**
  - 35kLUTs / 3Mb RAM
  - 112 DSP
  - No HSSL
  - No Hard IP Processor

- **Mid-End FPGA**
  - 364 DSP
  - HSSL 6G
  - Single-core ARM-IPS
  - No Peripherals

- **High-End FPGA (+ Soc architecture)**
  - 1760 DSP
  - HSSL 12G
  - Quad-core ARM-IPS
  - Full Soc architecture
Evaluating the NanoXplore 65nm SRAM based RadHard FPGA for CERN applications. (1/2)
Salvatore Danzeca (CERN)

FPGAs are needed in CERN regions affected by radiation
COTS FPGAs are divided in 2 families:

<table>
<thead>
<tr>
<th>SRAM</th>
<th>FLASH</th>
</tr>
</thead>
<tbody>
<tr>
<td>TID immunity (&gt;1kGy for most COTS)</td>
<td>TID is limiting the lifetime of the FPGA</td>
</tr>
<tr>
<td>Configuration Memory very sensitive to SEUs</td>
<td>Configuration Memory SEU immune</td>
</tr>
</tbody>
</table>

NanoXplore FPGAs seems a good Compromise, since memory cells have been Rad-hardened

Irradiations test at PSI:

1\textsuperscript{st} test - CRAM cells. Disable CMIC → Program FPGA → Irradiate → Check. No SEUs observed in 2 runs up to 1.72x10\textsuperscript{11} p

2\textsuperscript{nd} test - DSP blocks: 32x 24-bit x 24-bit multiplication of 2 fixed numbers → Check @clk → Update error counters → tx. counters every second. 3 runs of 1.72x10\textsuperscript{11} p

\[ \sigma = \frac{\# \text{errors}}{N_{\text{dsp}} \times \text{fluence}} \]

<table>
<thead>
<tr>
<th>setup</th>
<th>SEUs</th>
<th>SEFI</th>
<th>(\sigma_{\text{SEU}}(\text{cm}^2/\text{dsp}))</th>
<th>(\sigma_{\text{SEFI}}(\text{cm}^2/\text{dsp}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP</td>
<td>5</td>
<td>12</td>
<td>(8.6 \cdot 10^{-13})</td>
<td>(2.08 \cdot 10^{-12})</td>
</tr>
</tbody>
</table>
3rd test – BRAM in 3 diff. config. Modes: No ECC (6 runs), Fast ECC (3 runs) and Slow ECC (3 runs).
@ every Run: Write into the memory → Irradiate up to $3 \times 10^{10}$ p → Read back and tx. wrong data

$$\sigma = \frac{\text{#errors}}{N_{\text{bits}} \times \text{fluence}}$$

4th test – FF: 2 setups:

a) 8 chains of 3072 flip-flops initialized with an alternating pattern. → 4 runs up to $3 \times 10^{10}$ p
b) 8 inversors interfered between every flip-flop column. (More sensitive to SETs) → 1 run up to $1.72 \times 10^{10}$ p
@ every Run: Results check at every clock → tx. to a computer.

<table>
<thead>
<tr>
<th>Setup</th>
<th>SEUs</th>
<th>MBUs</th>
<th>$\sigma_{\text{SEU}} (\text{cm}^2/\text{bit})$</th>
<th>$\sigma_{\text{MBU}} (\text{cm}^2/\text{bit})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>No ECC</td>
<td>17641</td>
<td>289</td>
<td>$8.01 \cdot 10^{-14}$</td>
<td>$1.31 \cdot 10^{-15}$</td>
</tr>
<tr>
<td>Fast ECC</td>
<td>94</td>
<td>109</td>
<td>$8.85 \cdot 10^{-16}$</td>
<td>$1.04 \cdot 10^{-15}$</td>
</tr>
<tr>
<td>Slow ECC</td>
<td>0</td>
<td>0</td>
<td>$&lt; 9.4 \cdot 10^{-18}$</td>
<td>$&lt; 9.4 \cdot 10^{-18}$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Setup</th>
<th>SEUs</th>
<th>SEFI</th>
<th>$\sigma_{\text{SEU}} (\text{cm}^2/\text{bit})$</th>
<th>$\sigma_{\text{SEFI}} (\text{cm}^2/\text{chain})$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Simple FF</td>
<td>1</td>
<td>3</td>
<td>$1.3 \cdot 10^{-15}$</td>
<td>$1.25 \cdot 10^{-11}$</td>
</tr>
<tr>
<td>NOT gate FF</td>
<td>0</td>
<td>0</td>
<td>$&lt; 2.36 \cdot 10^{-16}$</td>
<td>$&lt; 7.26 \cdot 10^{-13}$</td>
</tr>
</tbody>
</table>

* All in the 1st run
Presentation of main techniques used to solve the challenges to obtain EUV lithography at 7nm.

- CO₂ laser hits small Sn droplets (~30um diameter) x2 at ~50kHz. This creates a ionized gas plasma and a 13.5 nm radiation is then produced and collected by a special ~0.5 meter mirror in order to selectively reflect and direct the 13.5nm light to the Intermediate Focus (IF) position at the entrance to the scanner system.
- Since EUV light with 13.5 nm wavelength can be absorbed by almost any matter, EUV lithography has to be done in vacuum.
- Lenses cannot be used with EUV, instead, specialized multilayer mirrors are used. Even those, absorb ~30% of the light, so the laser should be very powerful.
- Every chip in the wafer is scan individually and the system should produce 125 wafers/hours. For a 7 nm node there is an on-product overlay requirement of 3.5 nm, so scanners have to support an overlay budget of 2.5 nm (<10 silicon atoms!!) and this with acceleration ~100m/s².
The CMS High Granularity Calorimeter for HL-LHC. (1/7)

David Barney (CERN, EP-CMX)

Existing CMS endcap calorimeters cannot cope with the expected radiation or pileup @ HL-LHC

CMS @ HL-LHC:

- $10^{16}$ 1 MeV $n_{eq}$ cm$^{-2}$ @ 3ab$^{-1}$
- in forward calorimeters, with pileup $\sim$200
- And up to 2 MGy absorbed dose

HL-LHC:

- $L = 5 \times 10^{34}$ cm$^{-2}$s$^{-1}$
- and pileup 140, with potential for 50% higher L & pileup

Good jet identification and measurement: crucial for HL-LHC
Precise reconstruction of each particle within the jet: Particle Flow Algorithms and imaging calorimeters e.g. CALICE detectors for linear colliders (CLIC, ILC), CMS HGCAL

Granularity is more important than energy resolution
Active Elements:

- Hexagonal modules based on Si sensors in CE-E and high-radiation regions of CE-H
- Scintillating tiles with SiPM readout in low-radiation regions of CE-H
- Full system maintained at -30°C
- ~600m² of silicon sensors
- ~500m² of scintillators
- 6M Si channels, 0.5 or 1.1 cm² cell size
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all layers in CE-H
- ~27000 Si modules
- ~110 kW per endcap
The CMS High Granularity Calorimeter for HL-LHC. (4/7)

Wire bonding from PCB to silicon through holes

7 hexagonal modules for 2017 beam test
3 modules connected to a single “motherboard” providing power, data concentrator and optical links.
The CMS High Granularity Calorimeter for HL-LHC. (6/7)
Linear winch crane (custom made)
- Similar in principle to original CMS crane
- Calorimeter can be rotated in this system (no need for separate rotating table)
SAMPIC-based systems for precise timing detectors: implementation and performance. (1/2)

Jihane Maalmi (CNRS/LAL Orsay)

**SAMPIC** : SAMpler for PICosecond time.

Based on the concept of “Waveform TDC” (WTDC).

SAMPIC is designed to digitize a short signal or only a small part of a longer one (e.g. rising edge) to extract timing information.

Time information is obtained combining 3 acquired time stamps:

- Coarse → Counter → few ns step
- Medium → DLL locked on the clk to define region of interest → ~100ps step
- Fine → Digital algorithms applied on samples of the waveform → few ps

- Discriminator is used only for triggering, not for timing → no jitter added on measurement, low power
- Digitized waveform available to extract other parameters (Q, amplitude,...)
- One Common 12-bit Gray Counter (FClk up to 160MHz) for Coarse Timestamping.
- One Common servo-controlled 64-cell DLL : (from 1 to 10 GHz) used for medium precision timing & analog sampling
- 16 independent WTDC channels each with :
  - 1 discriminator for self triggering
  - Registers to store the timestamps
  - 64-cell deep SCA analog memory
  - One 11-bit ADC/ cell (Total : 64 x 16 = 1024 on-chip ADCs)
- One common 1.3 GHz oscillator + counter used as time base for all the Wilkinson ADCs.
- Read-Out interface

- Waveform continuously recorded (circular buffer), then stopped on trigger
- Main limitation is the dead time of conversion once the channel is triggered.
- Only the triggered channels are in dead time.
Several trigger modes programmable for each channel:

- External
- “Central” trigger (only OR in V1)
- Edge selection
- Enable/disable
- Internal/external threshold
- Posttrig (0,1,2 elementary delays)
- Fast Global Enable for common deadtime

- @ Trigger: simultaneous digitization of all the cells of all the triggered ch.
- Ramp slope is tunable: speed/precision tradeoff => 1.6μs for 11bits down to 100ns for 7 bits => main contribution to the Dead Time

- Module with several mezzanines (32/64/256-channels) + software and C libraries available
The proton timing system of the TOTEM experiment (1/2)

Edoardo Bossini (CERN)

On each arm:
- 4 tracking RP equipped with TOTEM strip detectors (210 and 220 m from the IP)
- 2 timing RP equipped with UFSD and readout with the SAMPIC chip

Reconstruction of primary vertex, they require to measure the p-p TOF in the two arms with a resolution of ~50 ps
The proton timing system of the TOTEM experiment (2/2)

**SAMPIC:**
- 16 channel/chip
- Up to 64 sample(hit) @ 10 GSa/s
- 1.5 GHz bandwidth
- 8-11 bit resolution
- 0.25-1.6 µs channel dead time

**SAMPIC chip was operated at 7.8 Gsa/s, with 8 bit voltage resolution. 24 samples were collected for each waveform (recording window of ~3.1 ns)**

**Very good quality of the collected waveform.**
Charact. of the 65nm pixel readout ASIC with on-chip quick transverse momentum discrimination capabilities. Davide Ceresa (CERN)

Phase-II upgrade of CMS Outer Tracker requirements:

- Increase granularity \(\rightarrow\) Introduction of a pixelated sensor
- Increase radiation tolerance \(\rightarrow\) Radiation tolerance up to 100 Mrad
- Participate in the L1 trigger \(\rightarrow\) Quick and on-chip particle discrimination
- Improve trigger performance \(\rightarrow\) Higher trigger rate and longer latency
- Reduction of material budget \(\rightarrow\) Power density < 100 mW/cm²

Tracker modules require the “intelligence” to discriminate particles locally and send only the interesting particle hits to the back-end.
Radiation tolerance enhancement of silicon photonics for HEP applications. (1/3)
Andrea Kraxner (CERN, EP-ESE)

Laser based transceivers reach their limit after HL-LHC and no optical links possible so far at the innermost pixel detectors and parts of the endcap calorimeter.

SiPh for future optical links for LHC and beyond

Why Silicon Photonics?:
- Compatibility with CMOS electronics (high density integration)
- small footprint
- higher bit rates
- reduced power consumption
- Possibility of customization

BUT what about radiation hardness???
Proposal for a Silicon Photonics optical Transmitter
Very resistant against displacement damage
BUT strong degradation due to ionization

No degradation up to 3 MGy → Compensation of irradiation effect during irradiation
Next generation of radiation tolerant Single-Mode Optical Links for Accelerator Instrumentation. (1/2)

Carmelo Scarcella (CERN, EP-ESE)

BE-BI roadmap for project requiring RH HS optical links

<table>
<thead>
<tr>
<th>Rad-Hard Link</th>
<th>Red-Hard DFE</th>
<th>Users</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBTx + SM VTRx</td>
<td>GEFE &amp; S-GEFE</td>
<td>New SPS BPM system (&quot;ALPS&quot;)</td>
</tr>
<tr>
<td>New collimator motor system (&quot;MCD&quot;)</td>
<td>Distributed IO Tier (BE-CO) or S-GEFE 2</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total links</th>
<th>Data-rates</th>
</tr>
</thead>
<tbody>
<tr>
<td>~ 300</td>
<td>GBTx</td>
</tr>
<tr>
<td>Tx 4.8 Gbps</td>
<td>Rx 4.8 Gbps</td>
</tr>
<tr>
<td>~ 5000 - 10000</td>
<td>LpGBT</td>
</tr>
<tr>
<td>Tx up to 10 Gbps</td>
<td>Rx 2.5 Gbps</td>
</tr>
</tbody>
</table>

Single-mode Versatile Link Transceiver VTRx

Front-End pluggable module Receiver:
- COTS InGaAs Photodiode
- Transimpedance amplifier GBTIA v3

Transmitter:
- COTS Edge emitter DFB laser
- Laser driver GBLD v4.2

TOSA Displacement damage test:
- SM TOSAs exposed to neutron beam at UC Louvain facility
- Irradiation with fluence up to $5 \times 10^{14}$ n/cm$^2$ 20 MeV neutrons
- Output optical power decreases due to threshold current rising
- Best in class with optical power drop of 40% at 40 mA bias current

10 Gbps VTx operation

All evaluated TOSAs rated for 10 Gbps operation

- Custom rad-hard ASIC – GBDL V4.2
- $I_{bias} = 2 + 43 \text{ mA}$
- $I_{modulation} = 4 + 24 \text{ mA}$
- $I_{emphasis} = 0 + 24 \text{ mA}$
- $T_{emphasis} = 60 + 90 \text{ ps}$

Enhancing the frequency response

BER Test

Wide 10 Gbps open eye diagram and negligible receiver sensitivity penalty compared to 5Gbps operation
• **Implementing the High Precision Timing IP for Xilinx Ultrascale FPGA’s (E. Mendes, CERN)**
  Interesting recipes to setup the GTH transceivers for Kintex Ultrascale so that they start with fixed-phase after link start-up. [https://gitlab.cern.ch/HPTD/tx_phase_aligner](https://gitlab.cern.ch/HPTD/tx_phase_aligner)

• **Introduction to the LpGBT-FPGA (J.M. Mendez, CERN)**
  The new FPGA IP implements the encoding/decoding schemes supported by the front-end ASIC, meaning that it can be configured using two decoding schemes and two line rates (10.24 or 5.12Gbps). The LpGBT-FPGA is not anymore given as a generic module that can be implemented in one block. It is now proposed as a set of modules with implementation example and reference notes to help the user in designing its own system. The “Mgt” block is not included in the LpGBT-FPGA folder as it is device and user dependant. However, reference notes are provided to show the typical / recommended configuration for different FPGAs. [http://lpGBT-fpga.web.cern.ch/doc/html/](http://lpGBT-fpga.web.cern.ch/doc/html/)

• **Fast Inference of Deep Neural Networks in FPGAs for Particle Physics (J. Duarte, Fermilab)**
  Implementation of machine learning methods (neural network models) into FPGA to identify b-quark jets, Higgs candidates, etc. They develop hsl4ml translates ML models from common open-source software packages into RTL abstraction for FPGAs using High-Level Synthesis (HLS) tools. ([arXiv:1804.06913](https://arxiv.org/abs/1804.06913), [hls-fpga-machine-learning.github.io/hls4ml](https://hls-fpga-machine-learning.github.io/hls4ml))

• **2 tutorials:**
  • SERDES Design in Advanced CMOS Technologies (MIROMICO)
  • LpGBT, a user's perspective (Paulo Moreira, CERN)
Thank you