The Upgraded LHC Interlock BPM System

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BE-BI-BP

BI Day 2018
04.12.2018

iBPM

Outline

- Introduction
- The proposed architecture
- Beam Position Estimation
- Preliminary beam results

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- Introduction
  - LHC Interlock BPM system
  - The upgrade goals
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  - Front-end concept
  - Digital acquisition chain
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  - Position normalization
  - Proposed algorithms
  - Doublet bunches case
- Preliminary beam results

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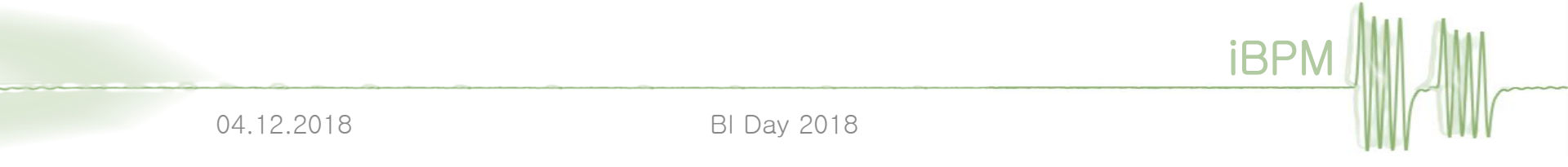
- Beam Position Estimation
- Preliminary beam results
  - Beam Acquisitions
  - Position Error Resolution and Offset

Introduction



LHC Interlock BPM system

BPM dedicated for machine protection purposes

- Beam dump protection
- Safe beam extraction

iBPM

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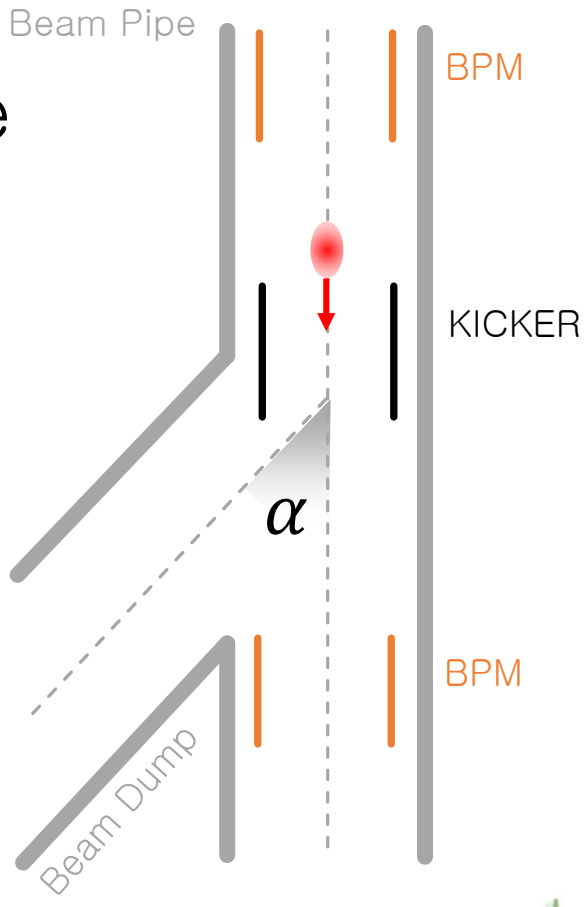

iBPM

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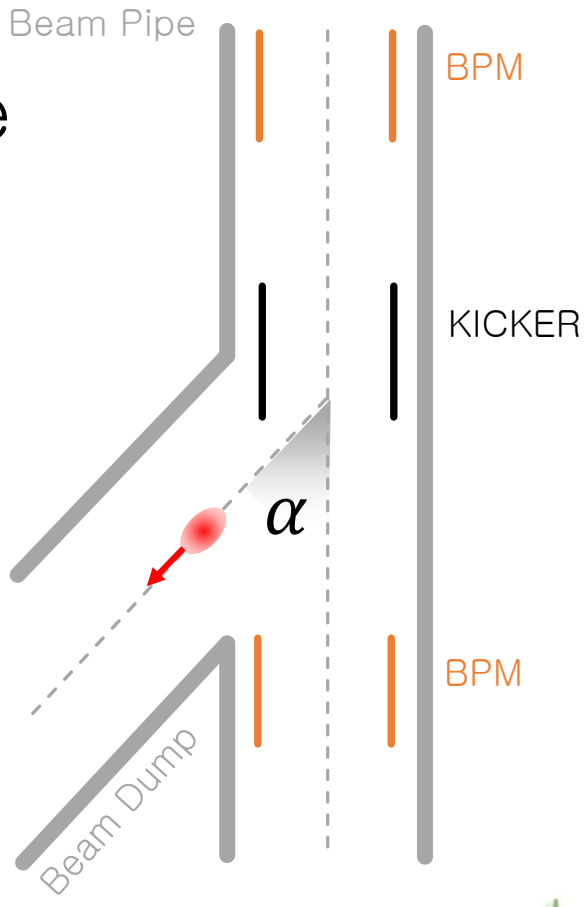

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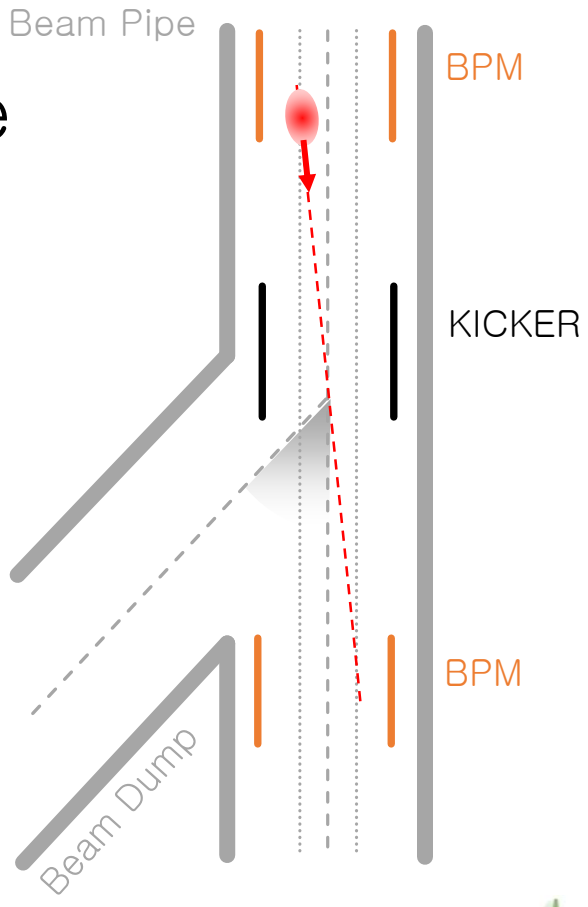

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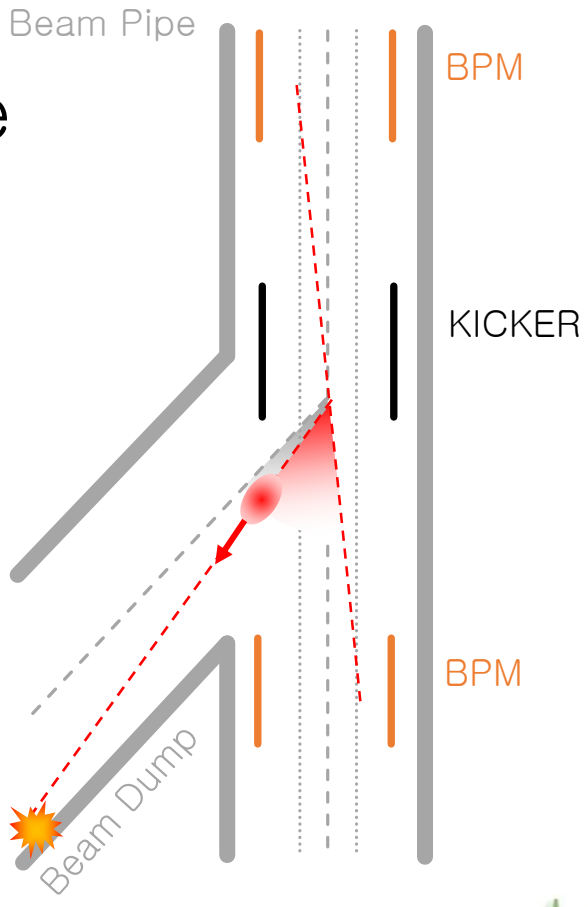

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LHC Interlock BPM system

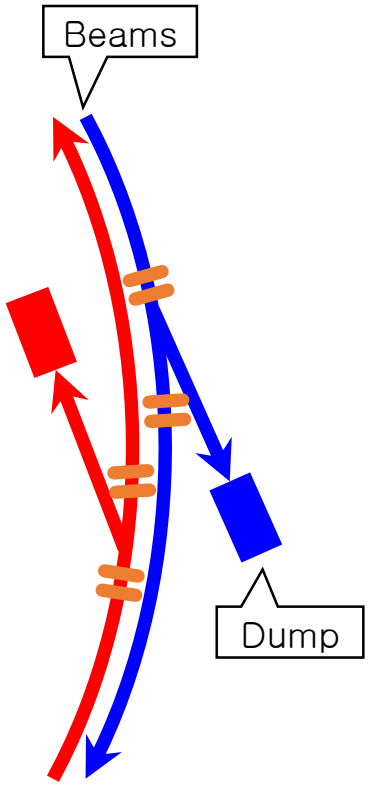
BPM dedicated for machine protection purposes

- Beam dump protection
- Safe beam extraction

- Real time
- Bunch-by-bunch

BPM channels:
- 2 beams
- 2 locations
- 2 planes
- 2x redundancy

→ 16 channels



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The Upgrade Goals

- No gain switching within a single fill
  - Intensity range 1e10 – 2e11 ppb
  - Resolution < 200 µm

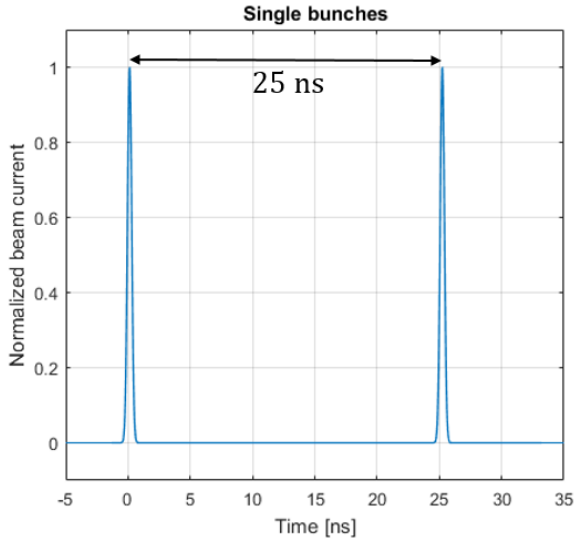
The Upgrade Goals

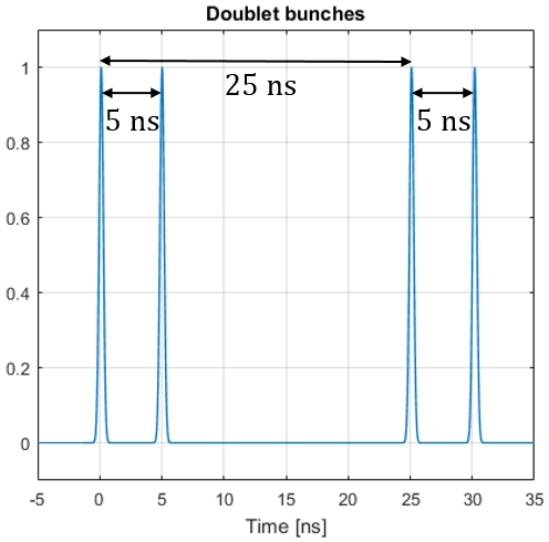
- No gain switching within a single fill
- Beam intensity independent position offset

  Measurement offset can generate false trigger

The Upgrade Goals

- No gain switching within a single fill
- Beam intensity independent position offset
- Doublet bunches (5 ns spaced)





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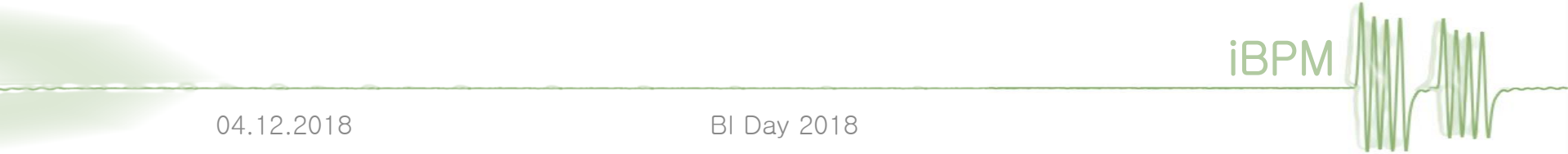
The Proposed Architecture



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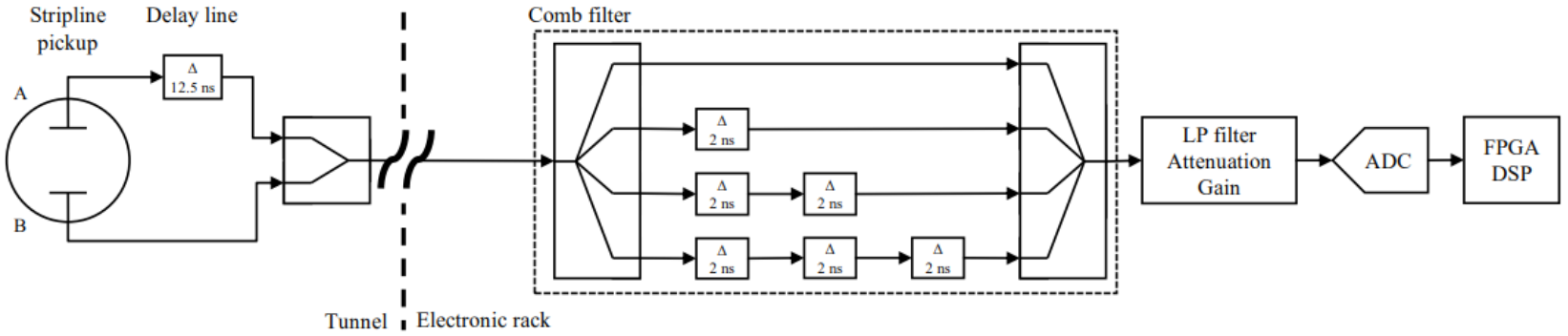

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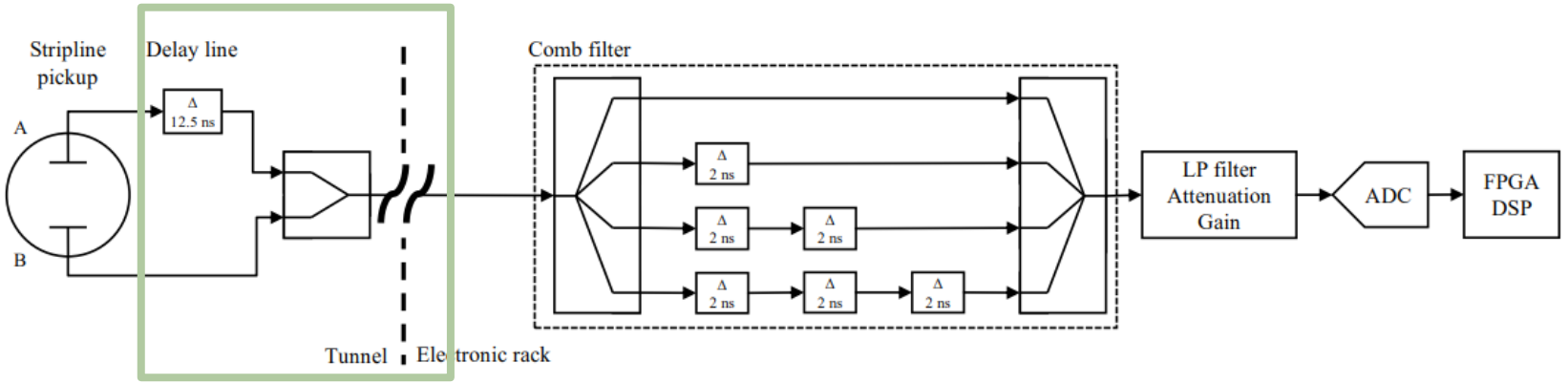
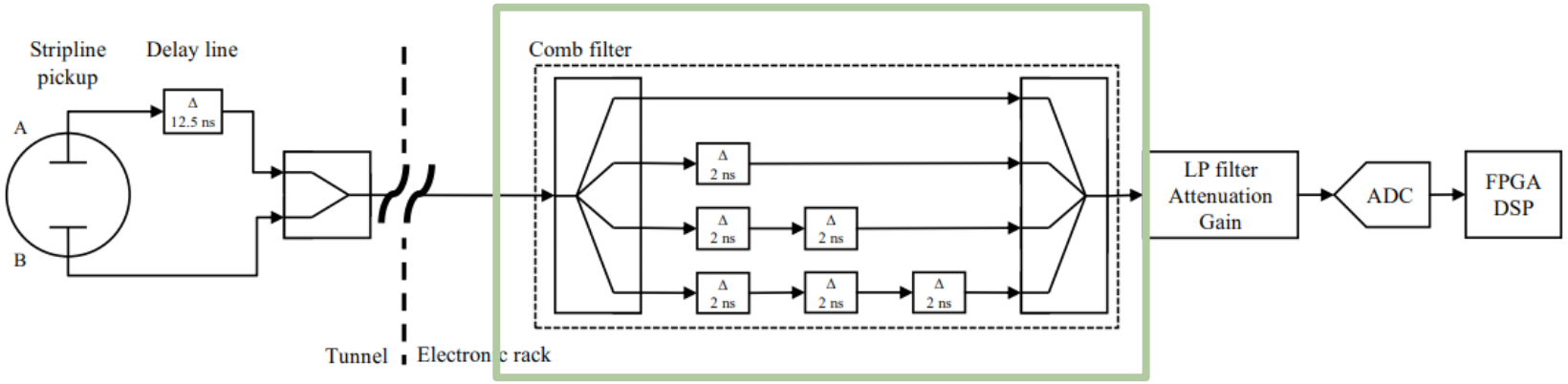


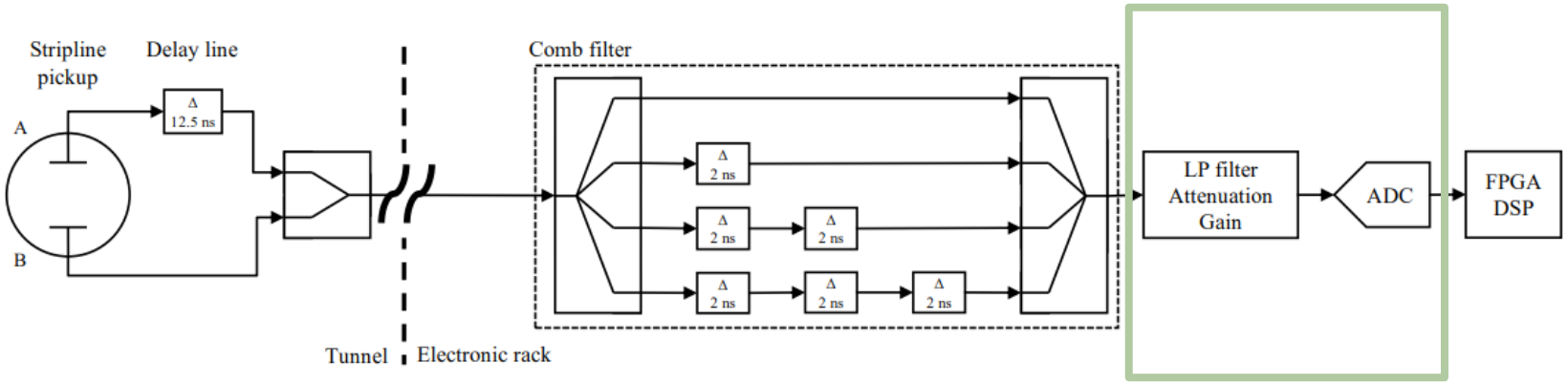
- Time-multiplexing
  - Single processing chain for both electrodes
  - Independent on channel to channel aging and drift effects

The Proposed Architecture



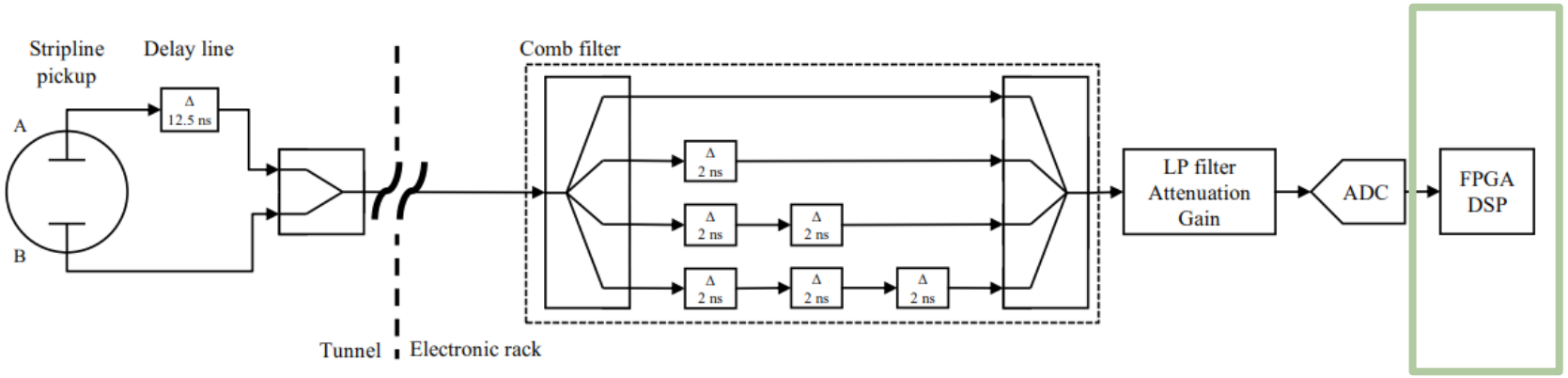
- Time-multiplexing
- Comb-filter
  - Signal extension through replicas

The Proposed Architecture



- Time-multiplexing
- Comb-filter
- Signal digitization

The Proposed Architecture



- Time-multiplexing
- Comb-filter
- Signal digitization
- Processing in FPGA

Front-End Concept

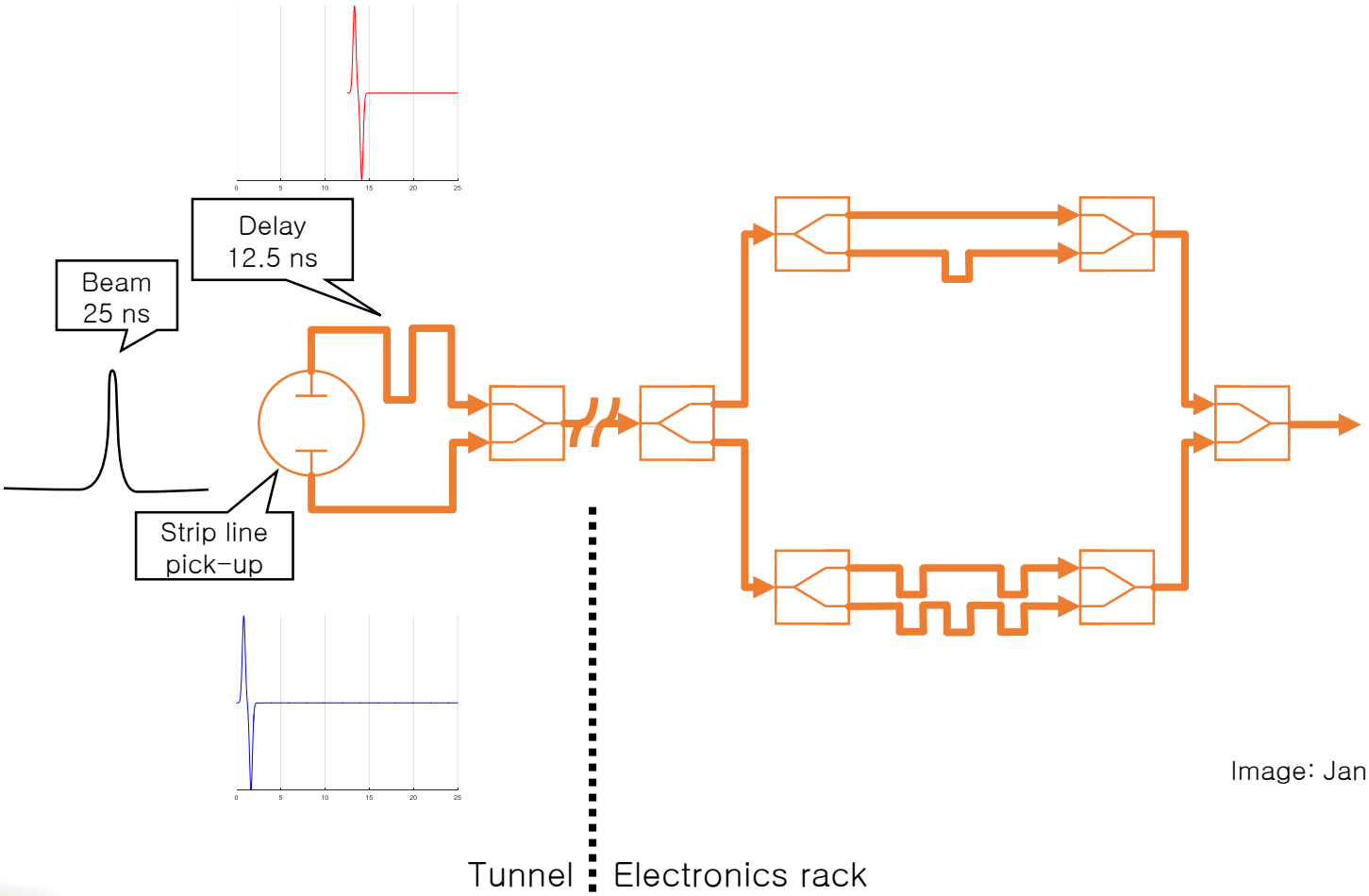
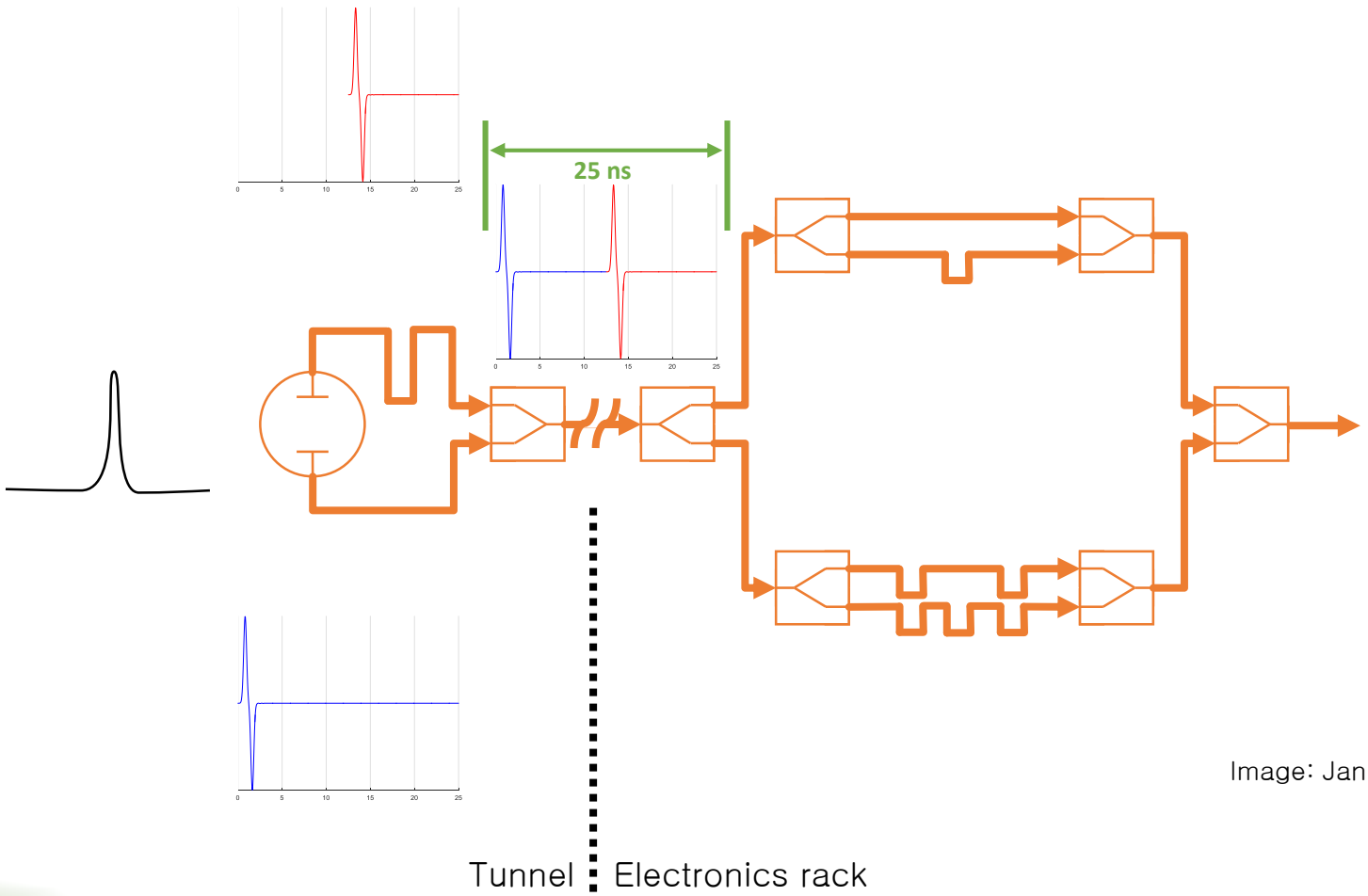


Image: Jan Pospíšil

Front-End Concept



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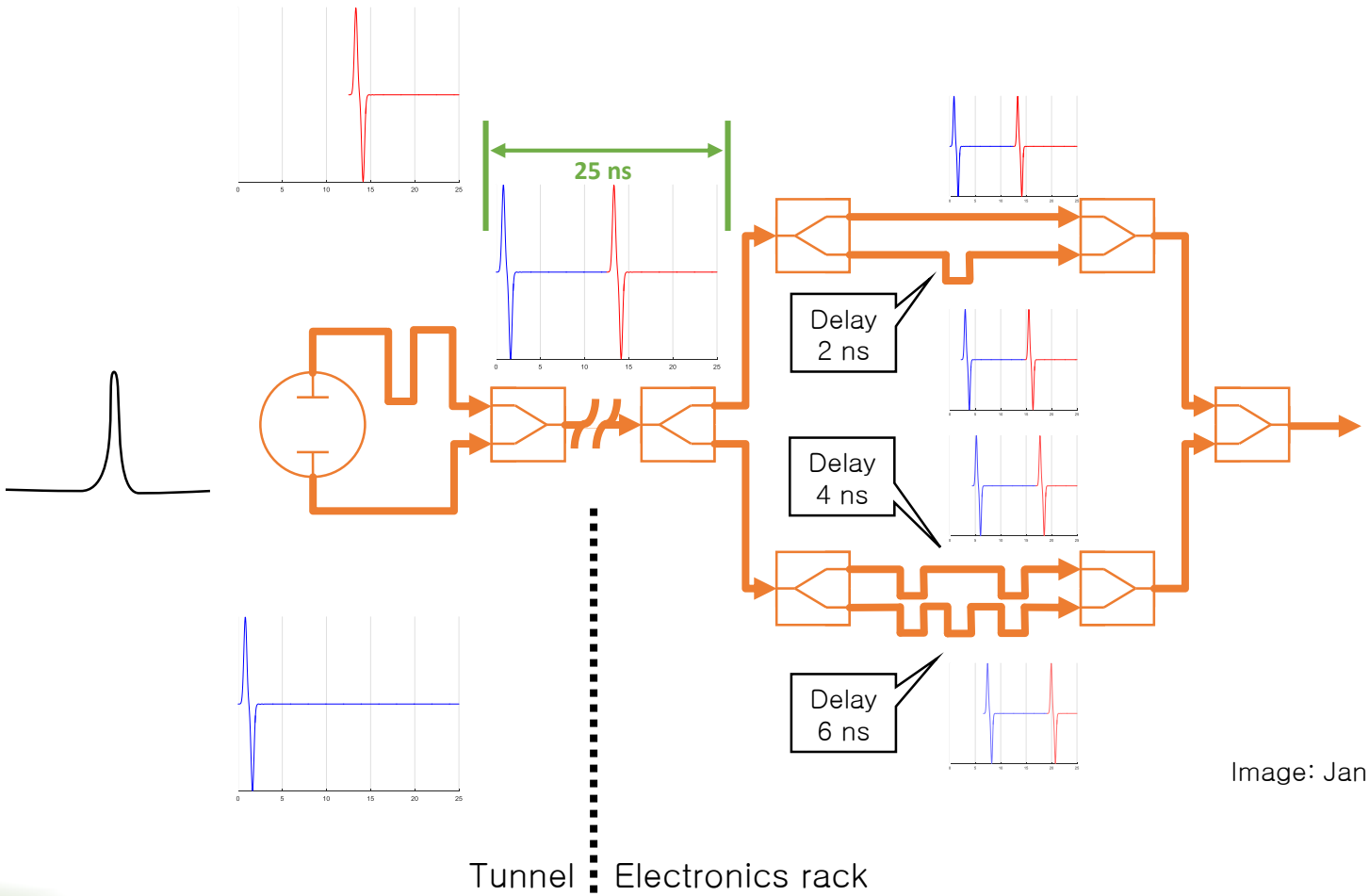
iBPM

Front-End Concept



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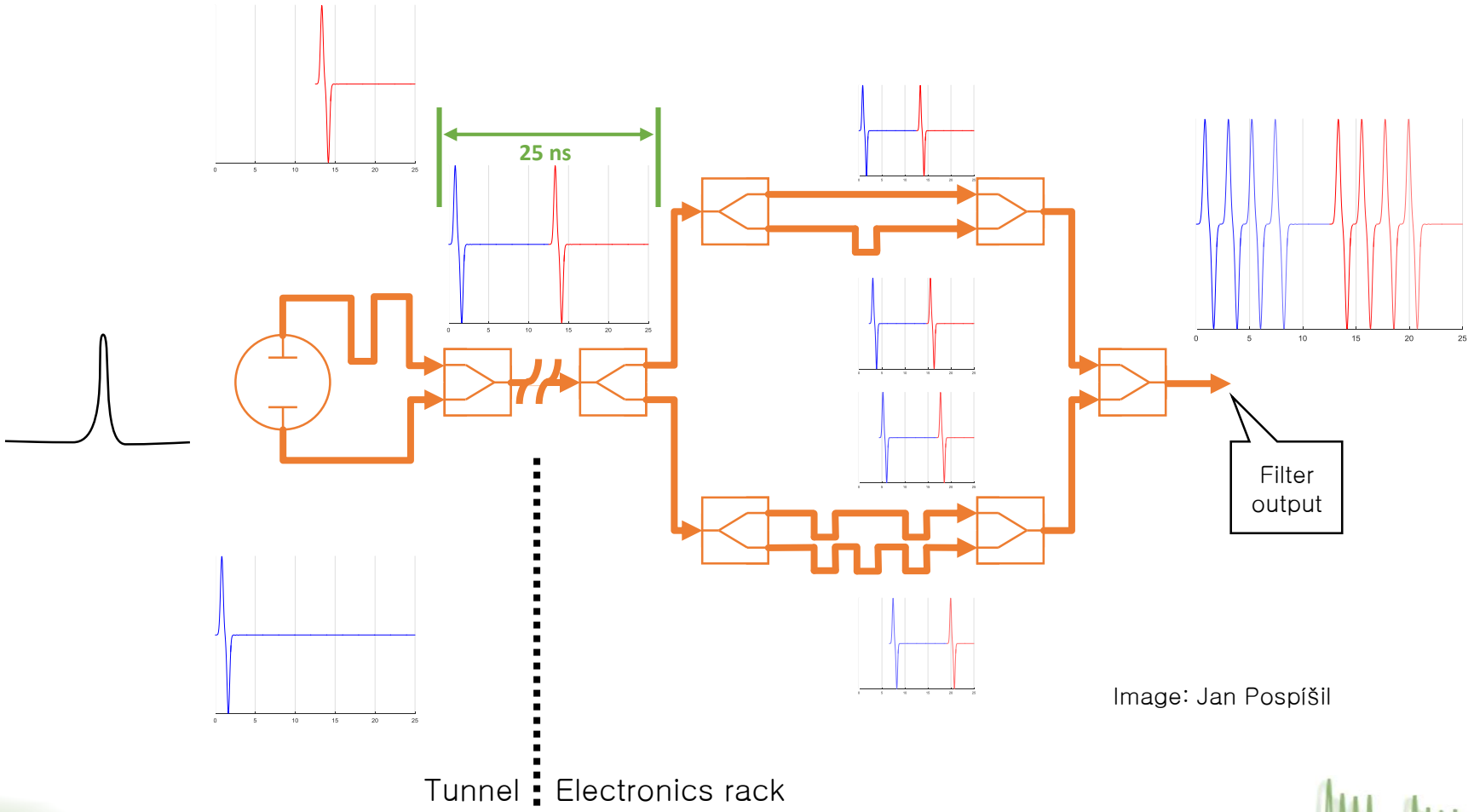
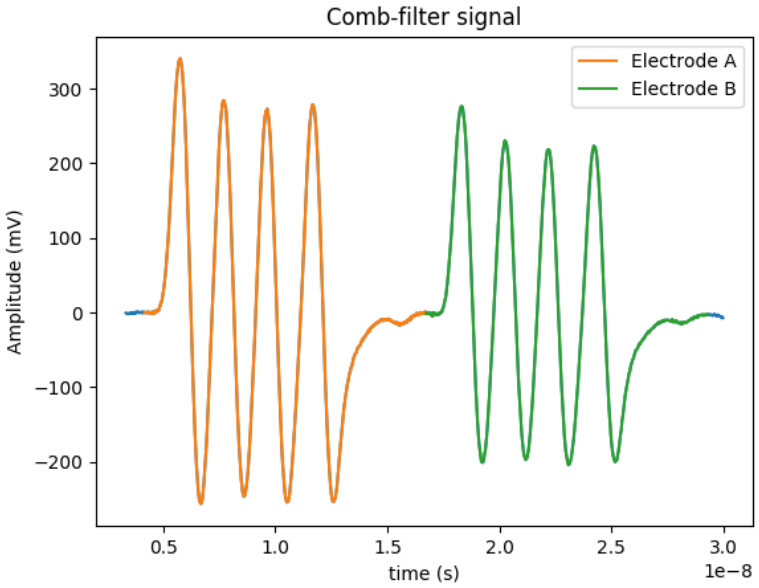
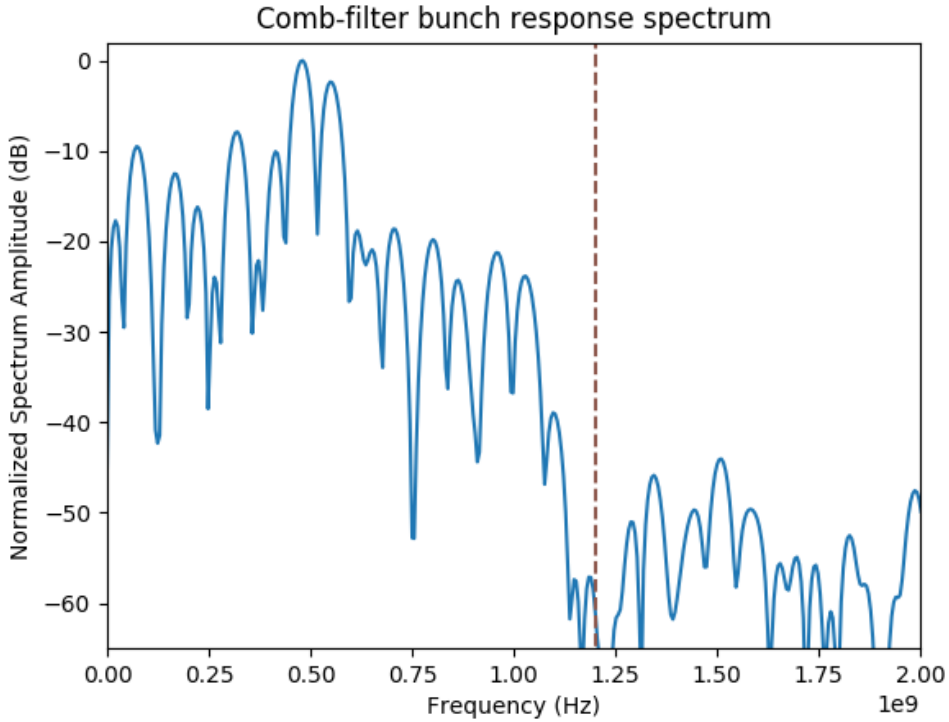


Image: Jan Pospíšil

iBPM

The Filter Output Signal

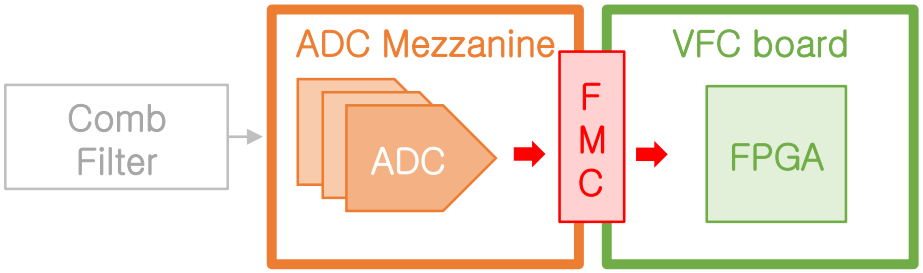




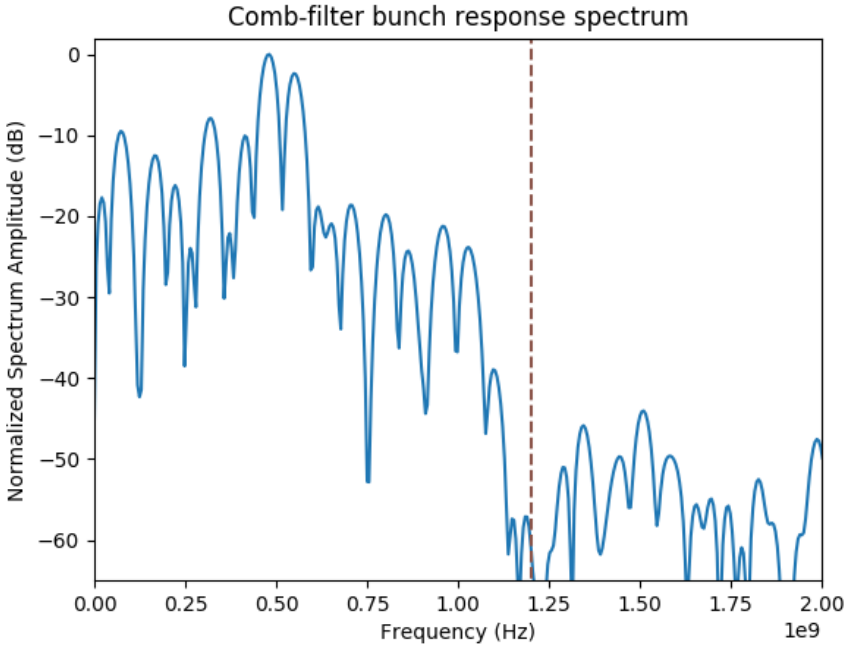
LHC P5, USC55, BPMSY4L5 (Stripline)
1.24e11 Bunch Intensity
Acquired with 8 bit – 18 GHz scope

iBPM

Digital Acquisition Chain



ADC sampling frequency bounded by FPGA transceivers max lane rate (6.5536 Gbps on VFC-HD).



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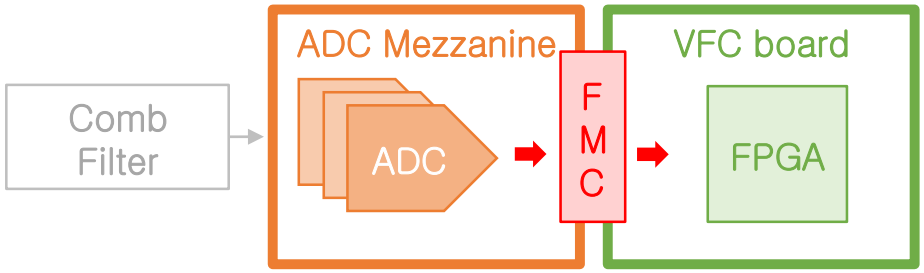
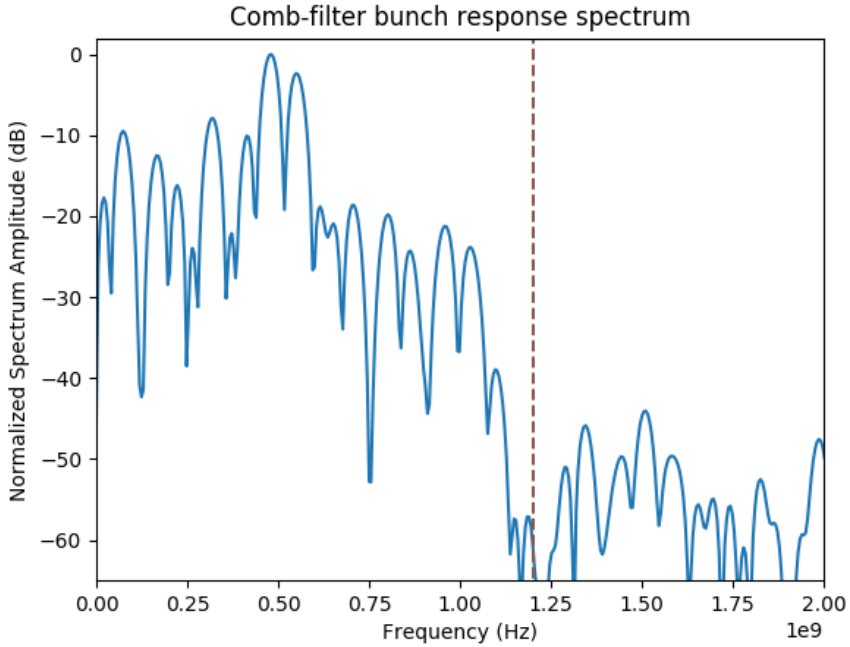


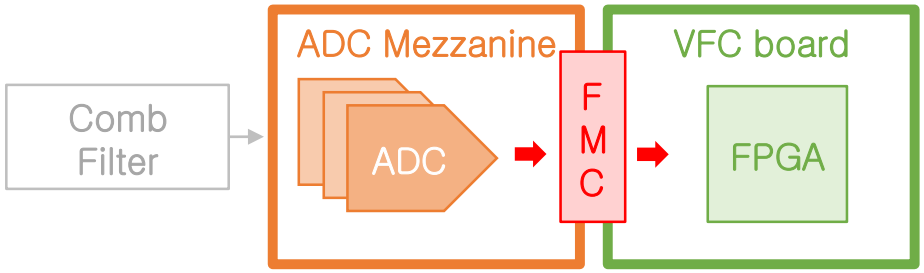


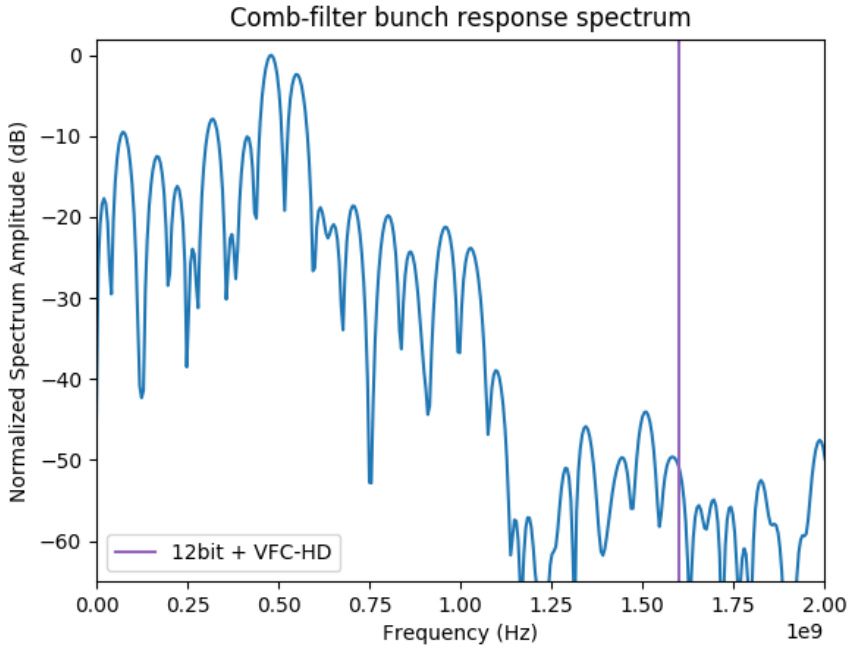
ADC sampling frequency bounded by FPGA transceivers max lane rate (6.5536 Gbps on VFC-HD).

Two mezzanines under test:

- Vadatech FMC225: 12 bits (8.8 ENOBS) up to 4 Gsps
  → operating @ 3.2 Gsps
- HTG-FMC-14ADC: 14 bits (9.6 ENOBS) up to 3 Gsps
  → operating @ 2.6 Gsps

Digital Acquisition Chain





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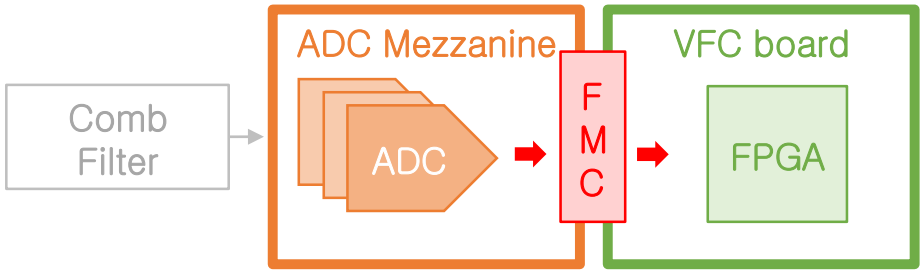

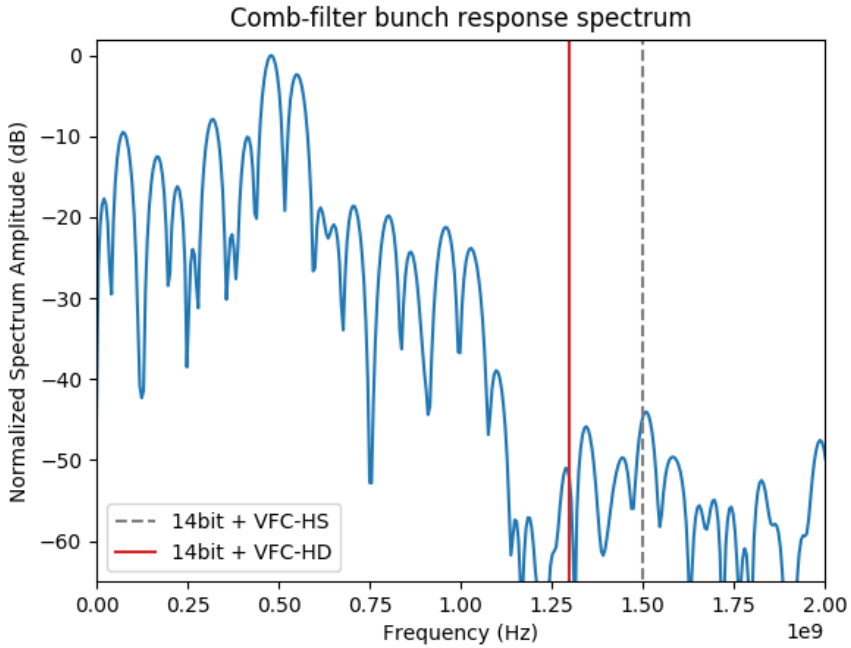

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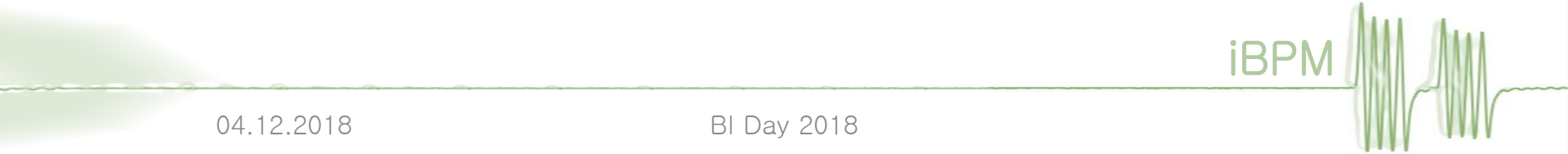
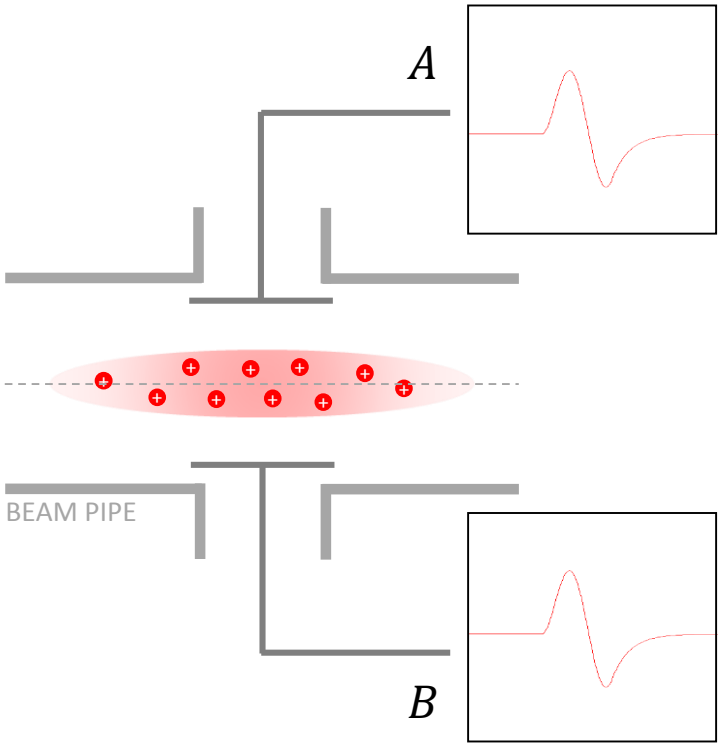
  → operating @ 2.6 Gsps (3 Gsps on VFC-HS)

iBPM

Beam Position Estimation

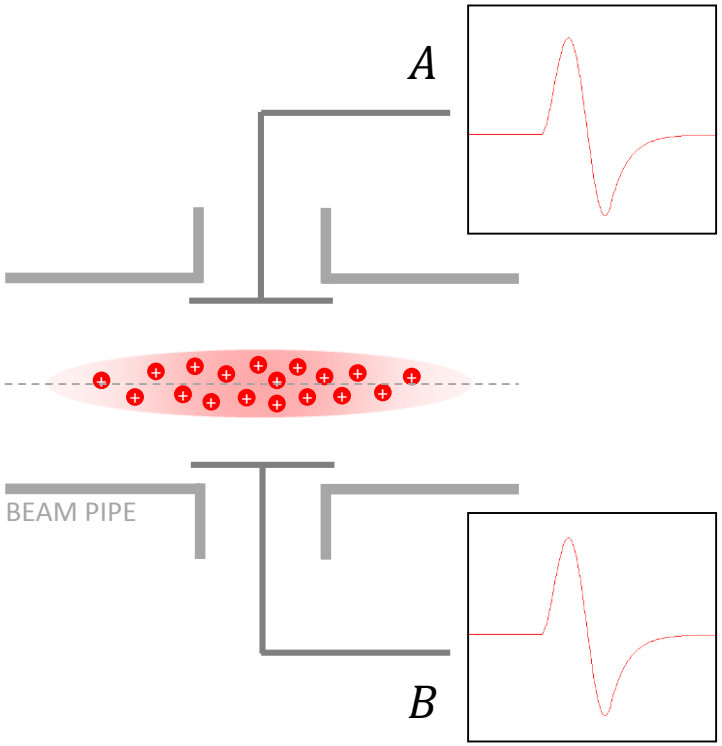


Position Normalization



$$\begin{cases} P_A = \alpha \cdot I \\ P_B = \alpha \cdot I \end{cases}$$

Position Normalization



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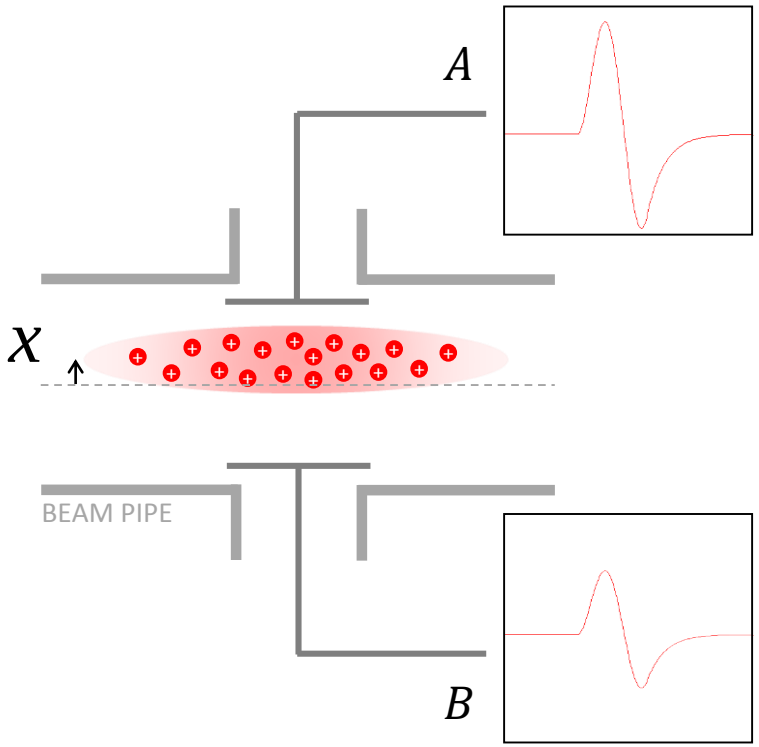
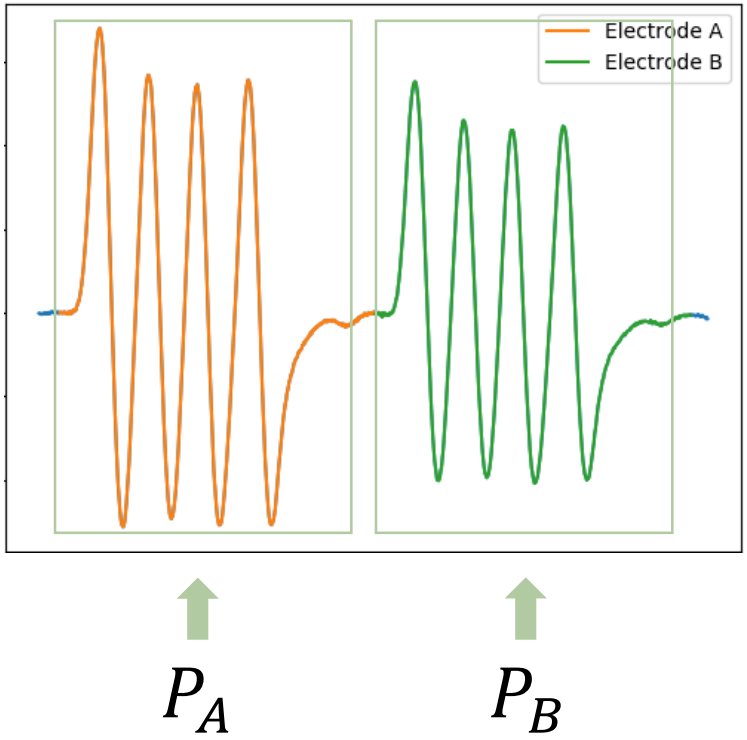
Position Normalization



$$\begin{cases} P_A = \alpha \cdot I(1 + \beta x) \\ P_B = \alpha \cdot I(1 - \beta x) \end{cases}$$

$$x = k \frac{P_A - P_B}{P_A + P_B}$$

Position Normalization



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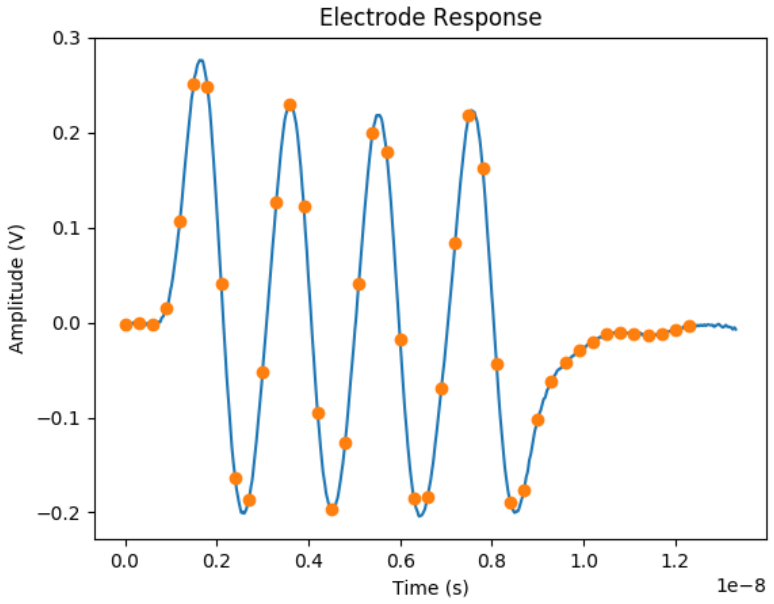
Proposed Algorithms

Signal power estimation algorithms:

- Root Mean Square

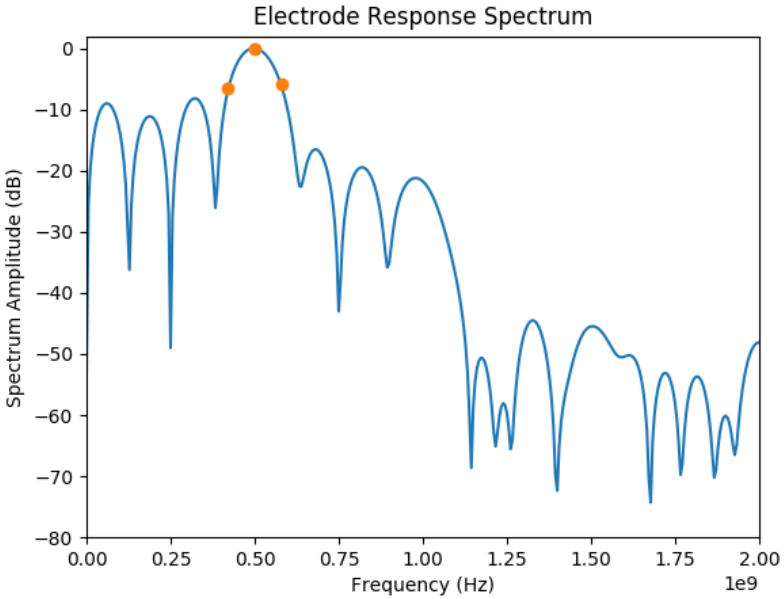


$$P = \sqrt{\frac{1}{N}\sum_{i=0}^{N} x_i^2}$$

Proposed Algorithms

Signal power estimation algorithms:

- Root Mean Square
- Frequency Domain



$$P = \sqrt{\frac{1}{2N}\sum_{i=peak-N}^{peak+N} |X_i|^2}$$

iBPM

Proposed Algorithms

Signal power estimation algorithms:

- Root Mean Square
- Frequency Domain
- Linear Fitting (LLS)

Proposed Algorithms

Signal power estimation algorithms:

- Root Mean Square
- Frequency Domain
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- Correlation

Proposed Algorithms

Signal power estimation algorithms:

- Root Mean Square
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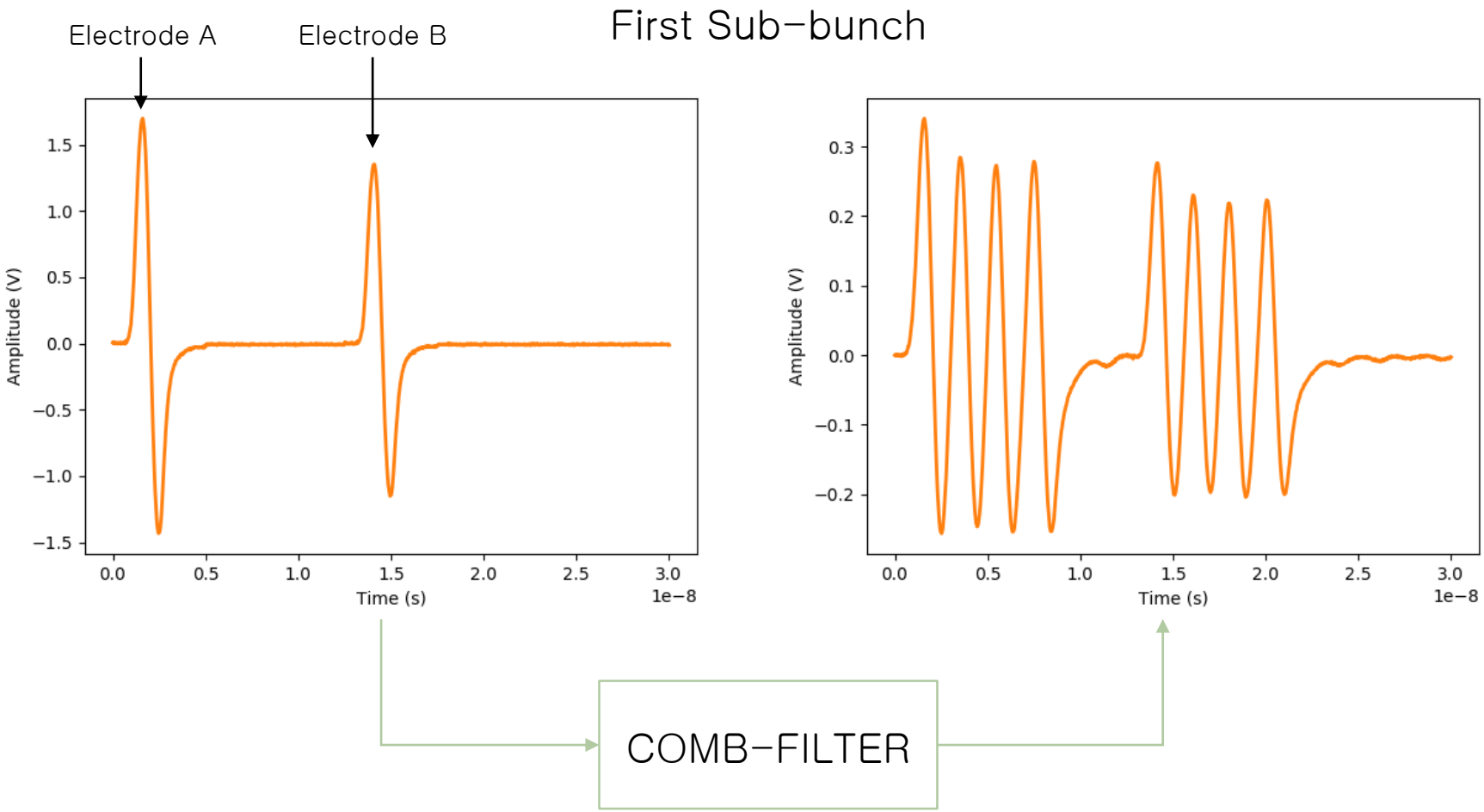
- Correlation

. . . work in progress!

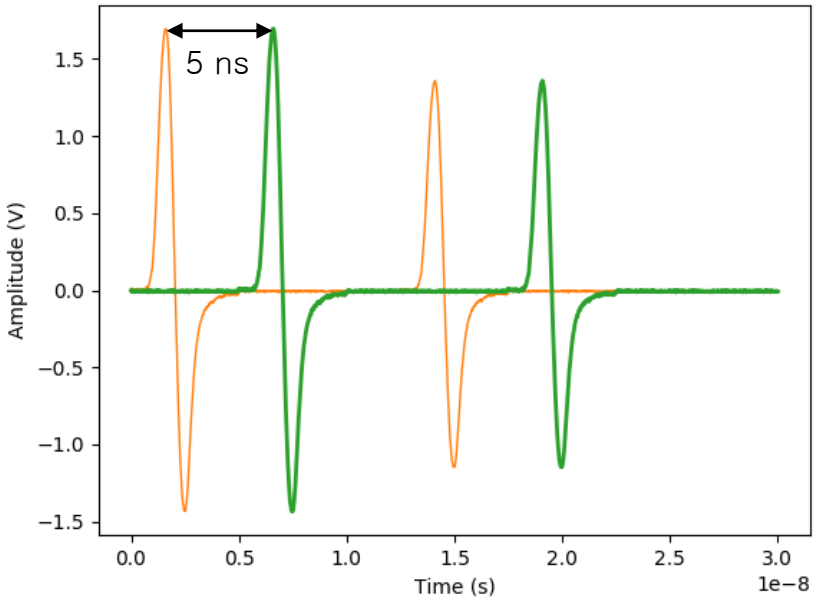
Best performances → RMS

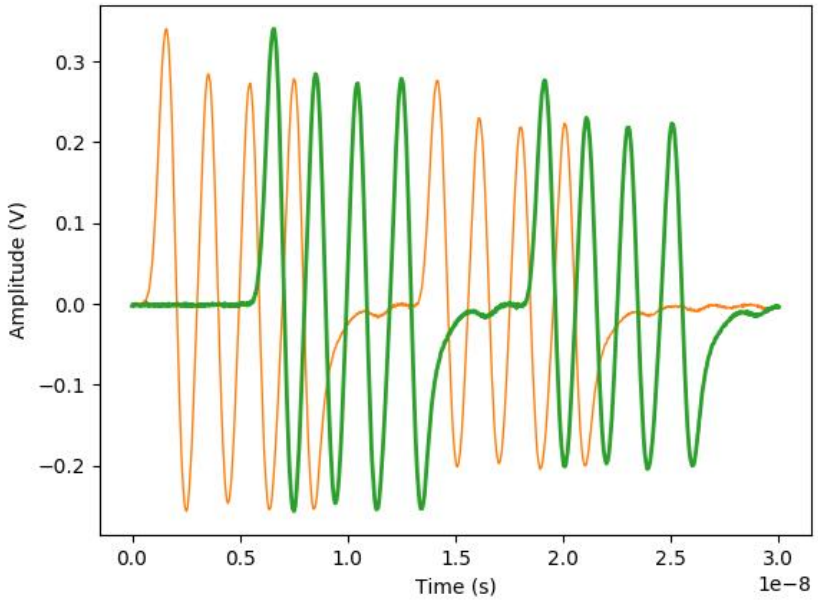
Doublet Case



Doublet Case

Second Sub-bunch



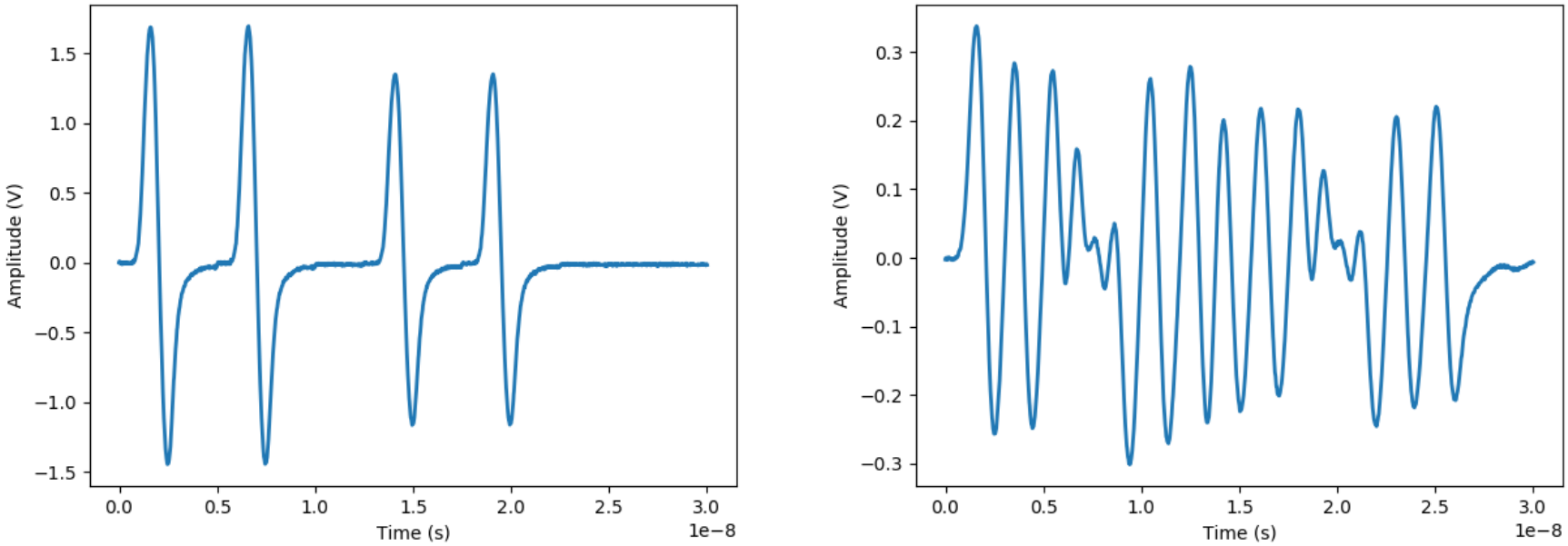


COMB-FILTER

iBPM

Doublet Case

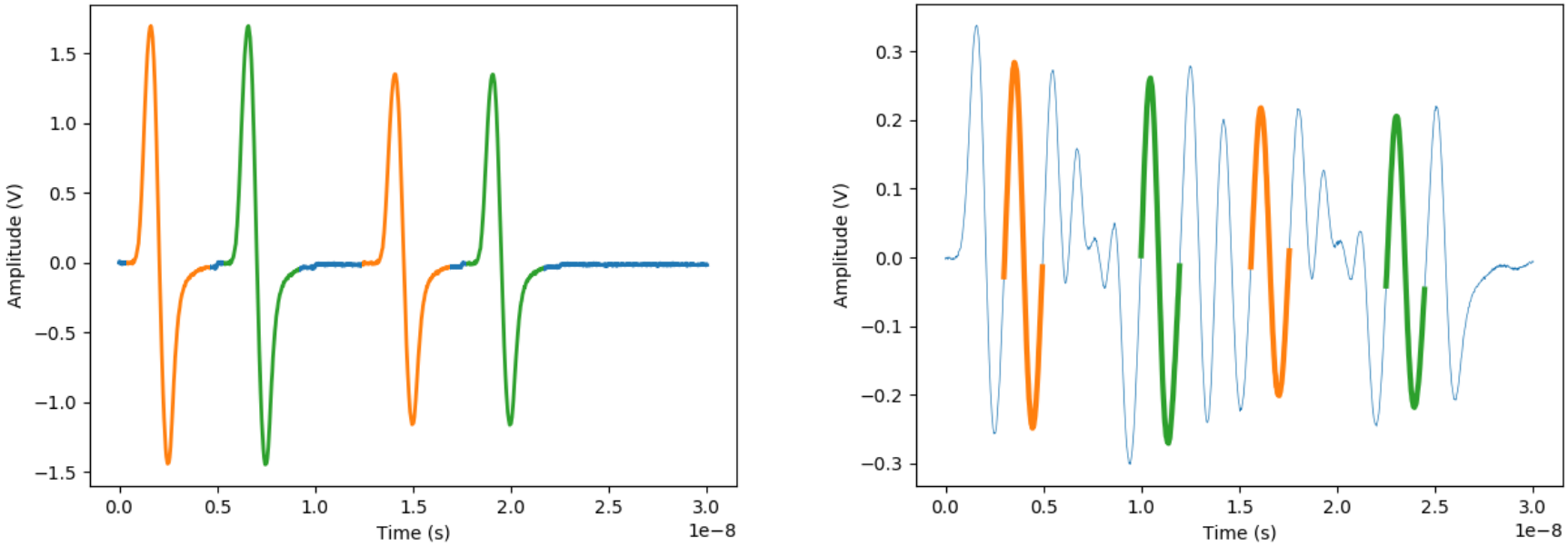
Doublet signal



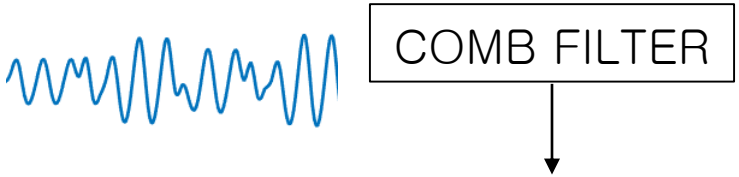
COMB-FILTER

Doublet Case

Doublet signal



Doublet Case



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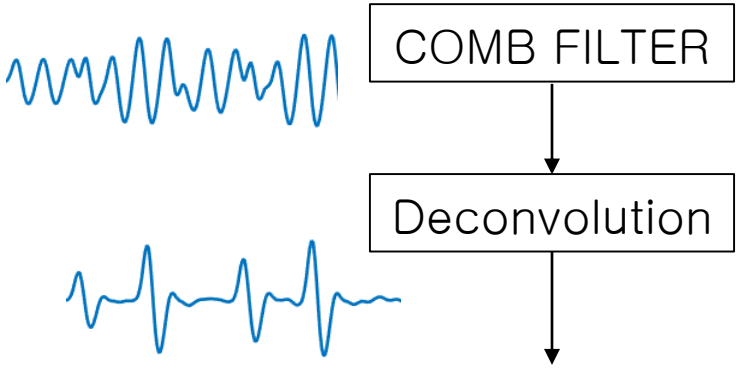

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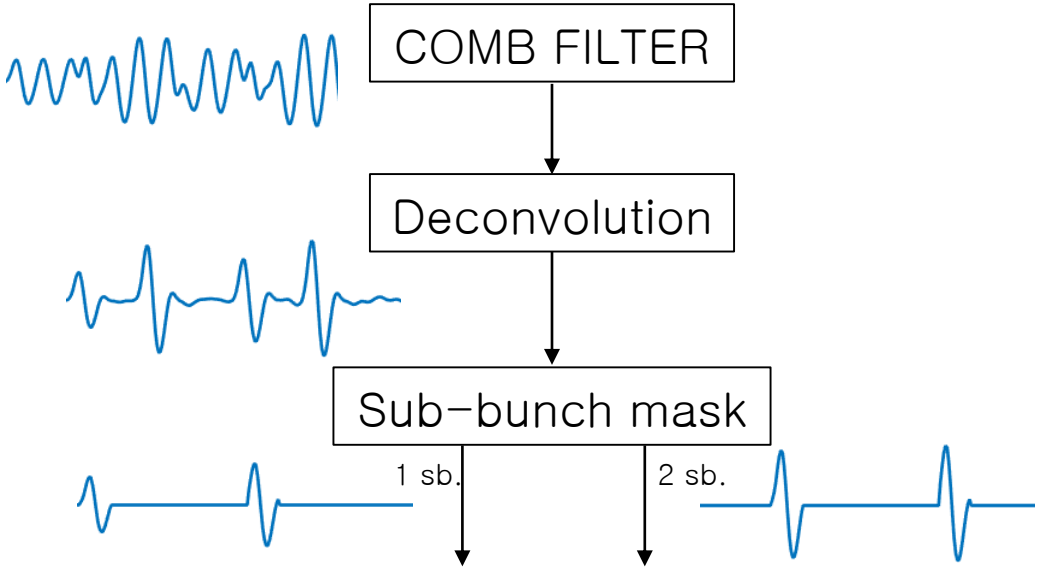

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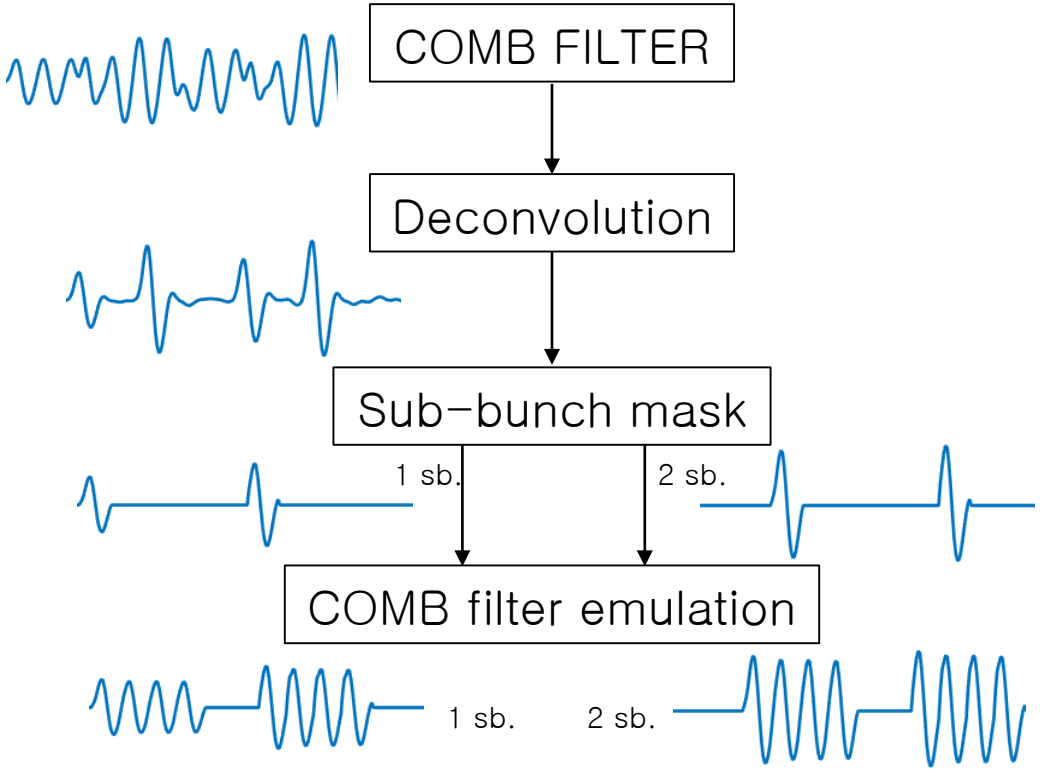

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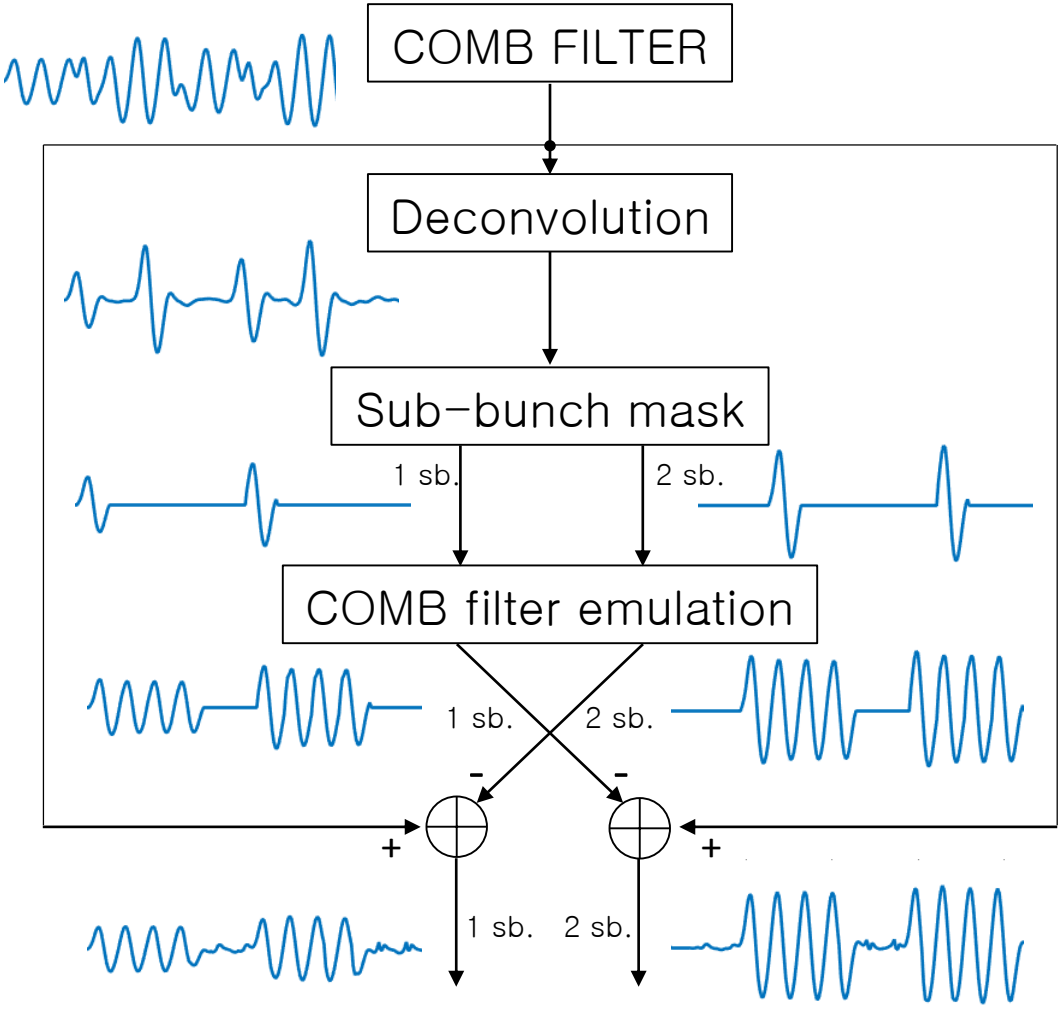
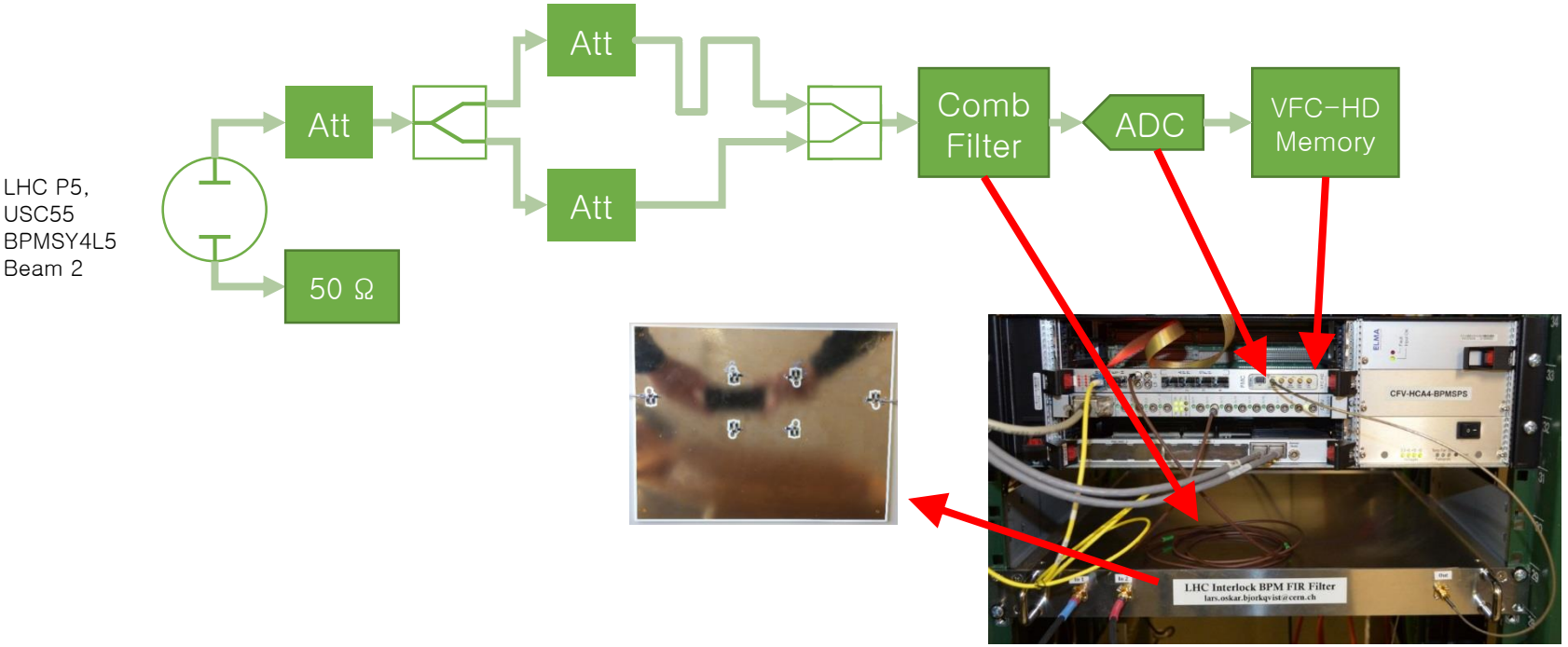


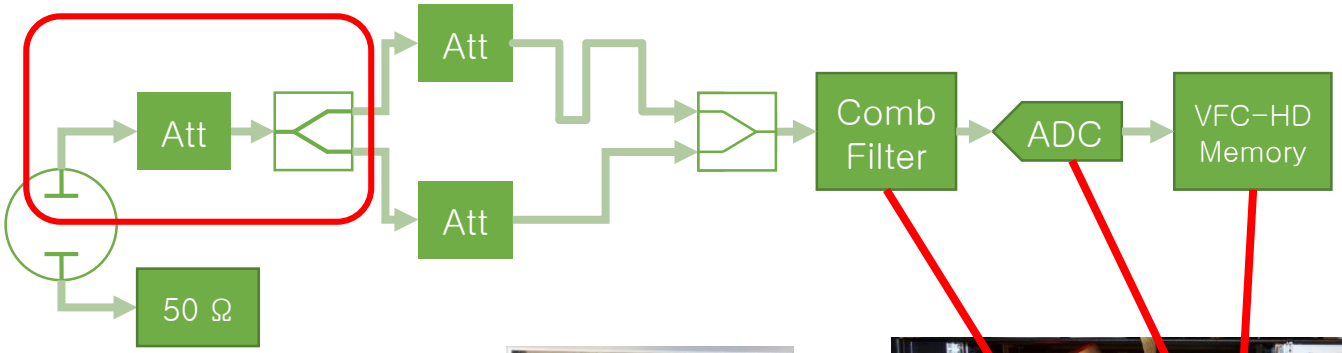
iBPM

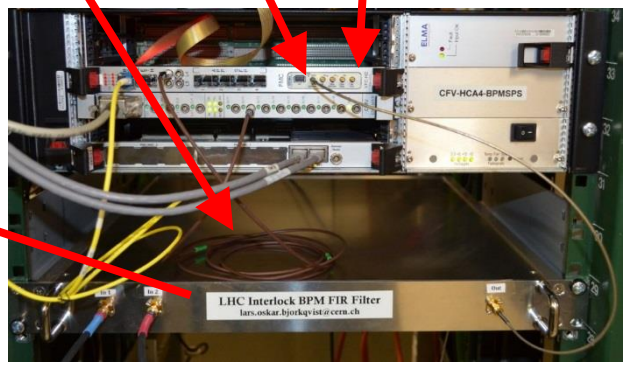
Preliminary Beam Results

Measurements set-up



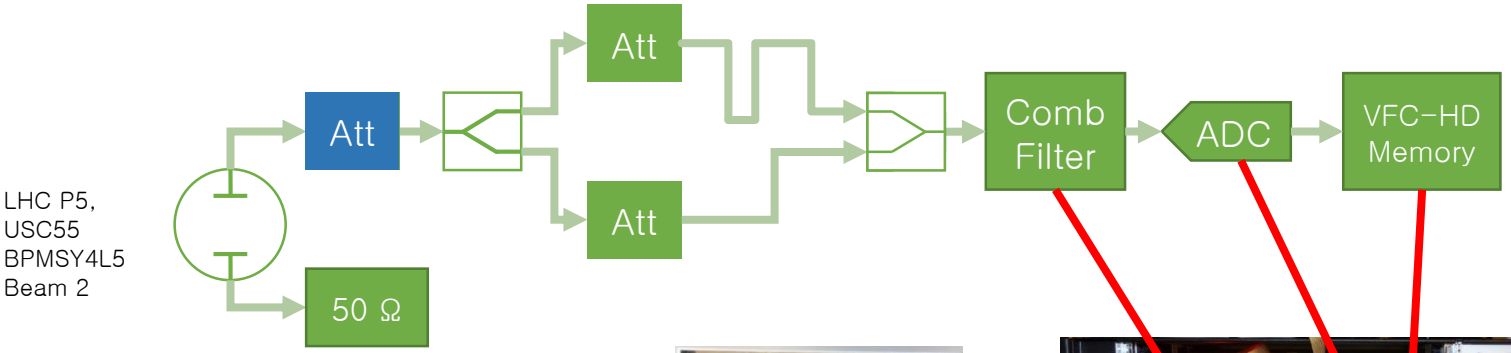
Measurements set-up

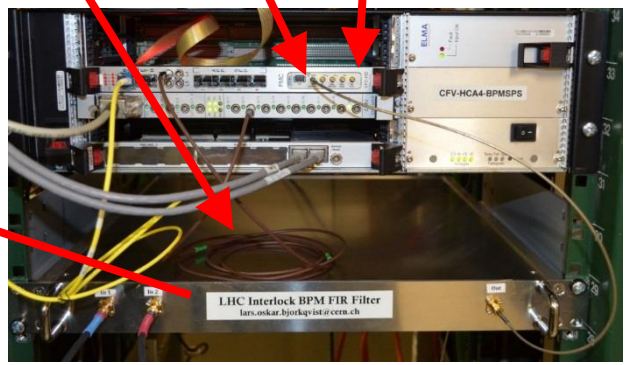




- Decoupled from beam motion

Measurements set-up





- Decoupled from beam motion
- Emulation of intensity

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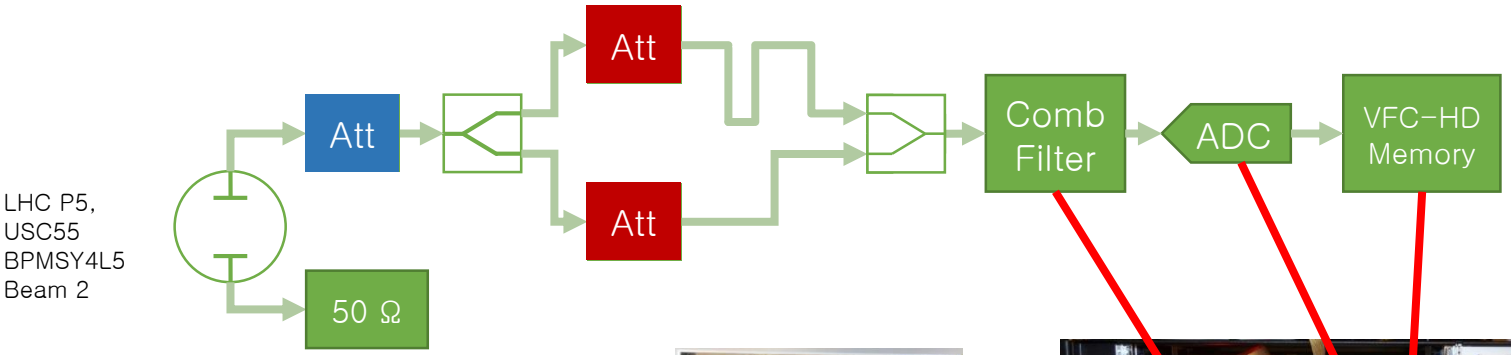

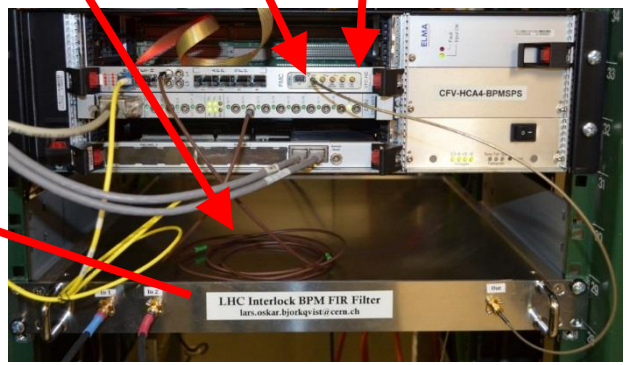

- Decoupled from beam motion
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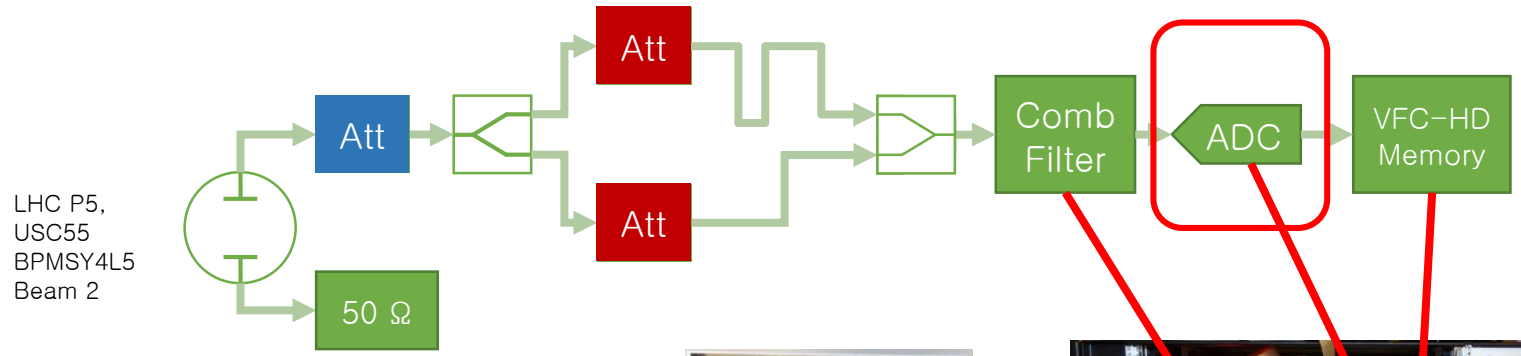
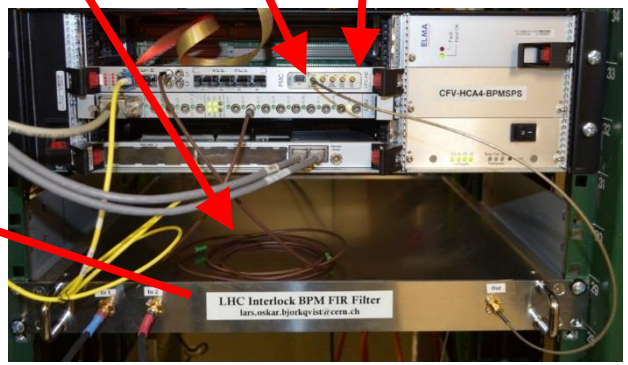
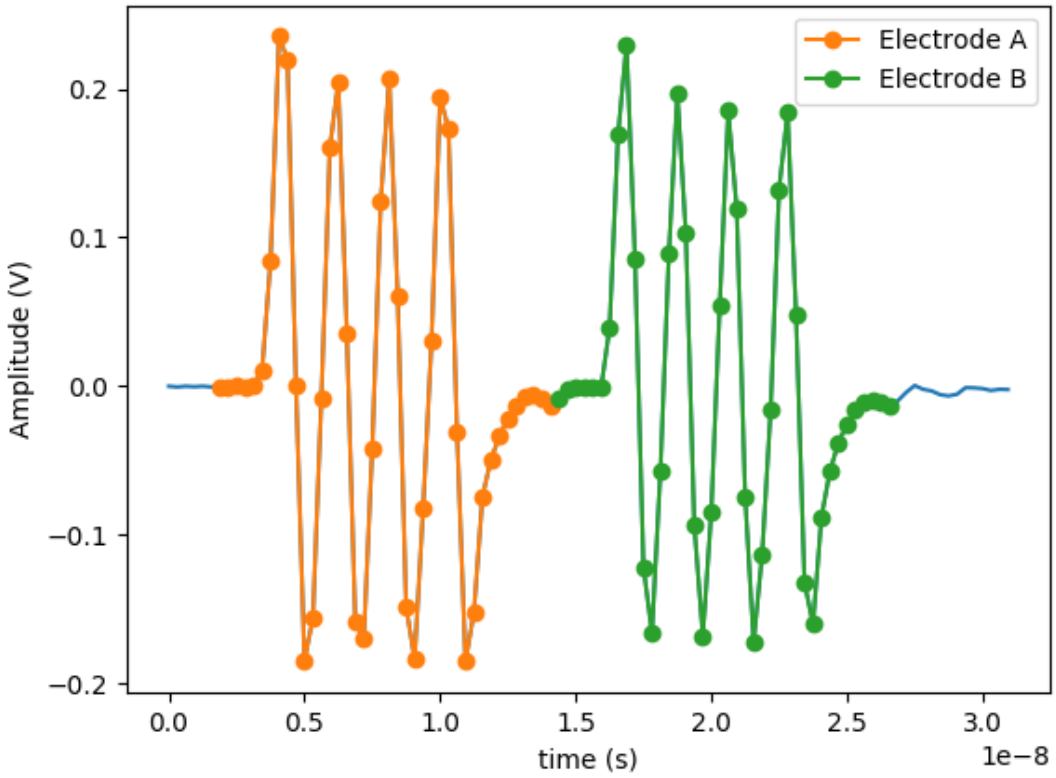




- Decoupled from beam motion
- Emulation of intensity
- Emulation of displacement
- ADC configurations:
  1. Vadatech 12bit @3.2 Gsps
  2. HTG 14bit @2.6 Gsps

Beam Acquisitions



- 40 – 12bit samples per electrode
- Beam Asynchronous
- Beam Synchronous

Acquisition: Vadatech 12bit (8.8 ENOBS) @ 3.2 Gsps

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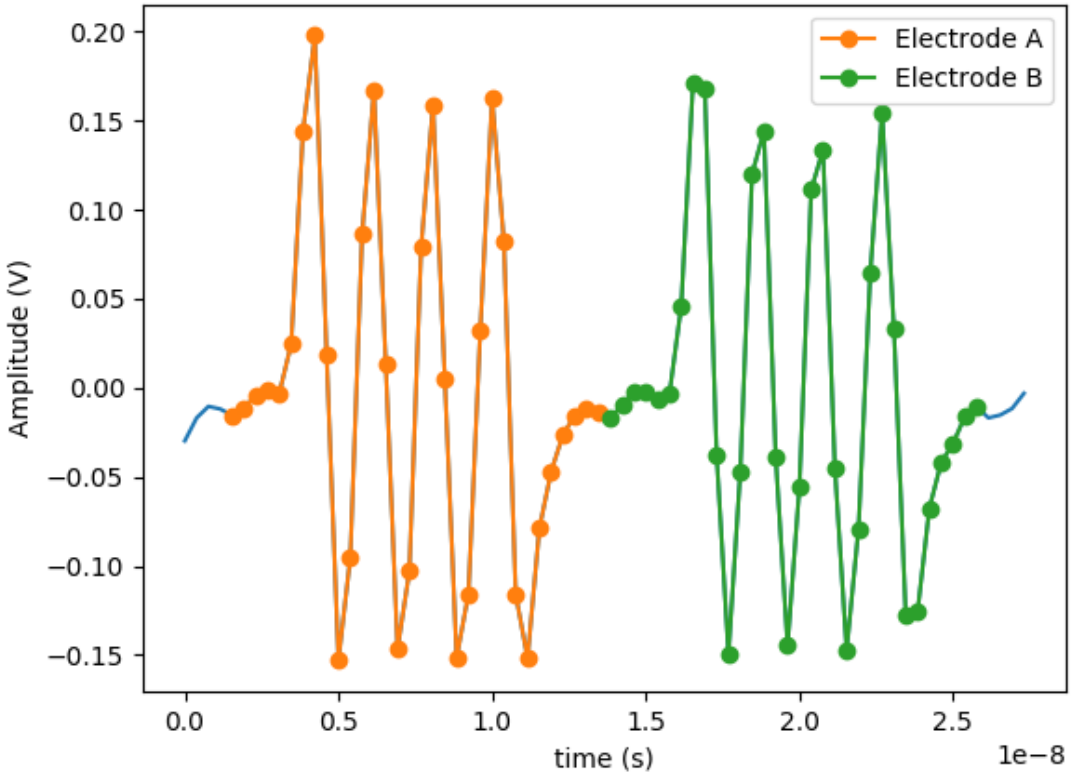
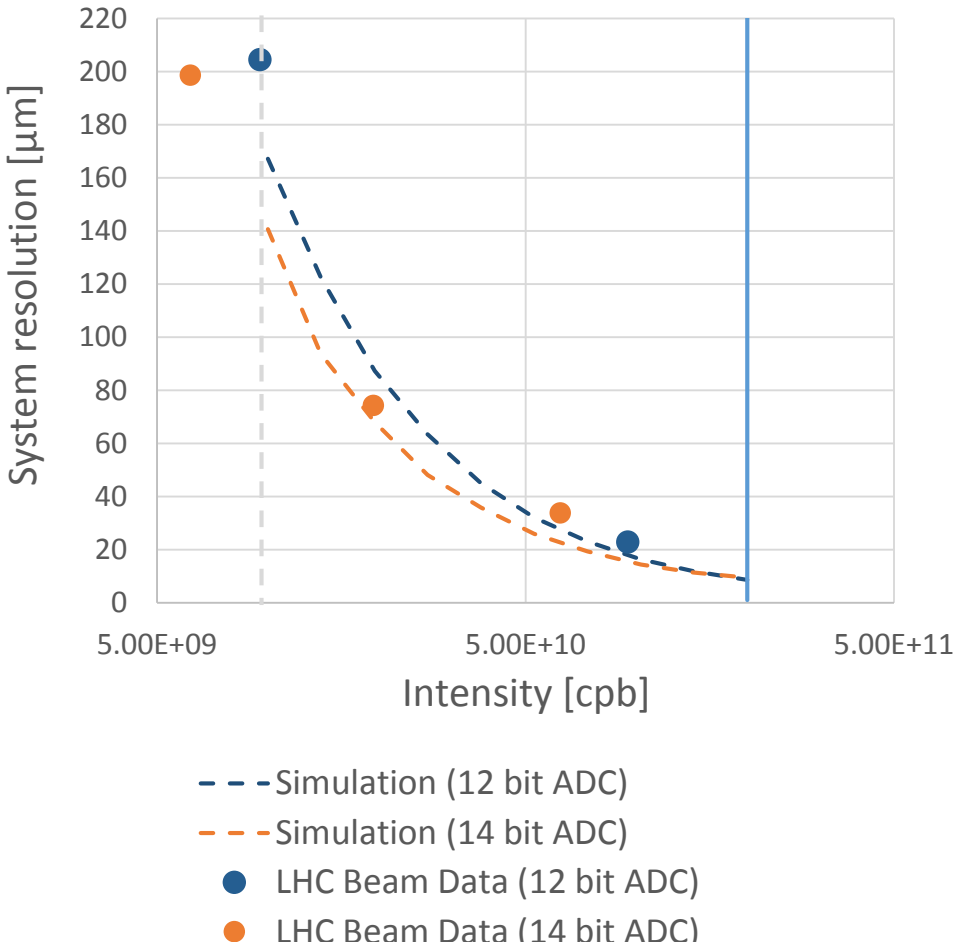


- 32.5 – 14bit samples per electrode
- Beam Asynchronous

Acquisition: HTG 14bit (9.6 ENOBS) @ 2.6 Gsps

Position Error Resolution

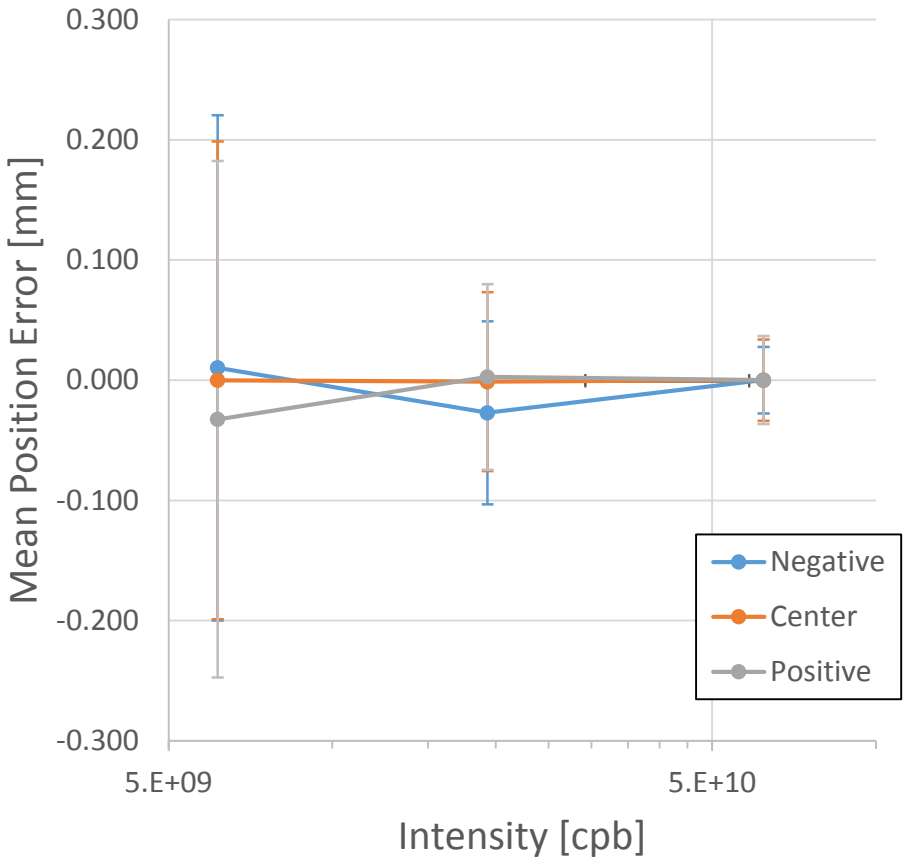


Intensity is scaled in order to cover the full ADC range with maximum intensity (2e11) and displacement (± 7.5 mm).

Resolution comparison for the two ADCs results with the simulation results.

- ✓ Resolution < 200 µm
- ✓ Low Intensity → gain with number of bits, despite lower f_s

Position Error Offset

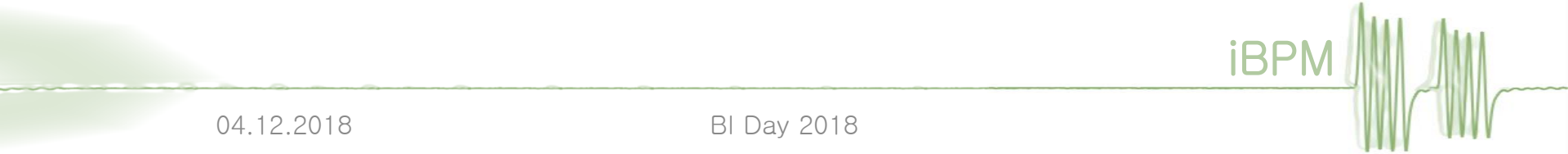


Intensity is scaled in order to cover the full ADC range with maximum intensity (2e11) and displacement (± 7.5 mm).

Mean value of Position Error for the ADC 14bit @2.6 Gsps

✓ Intensity independent

Summary



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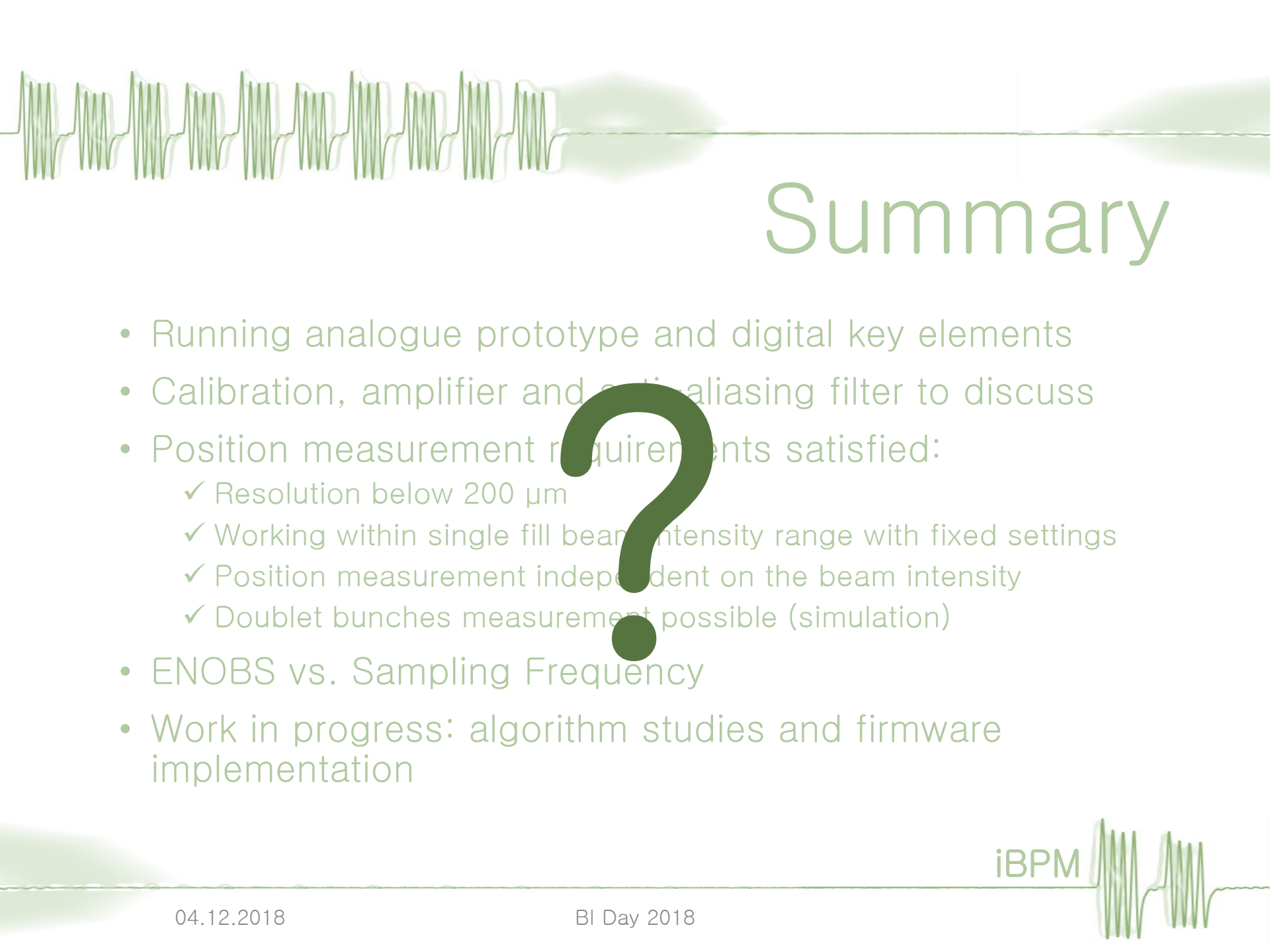


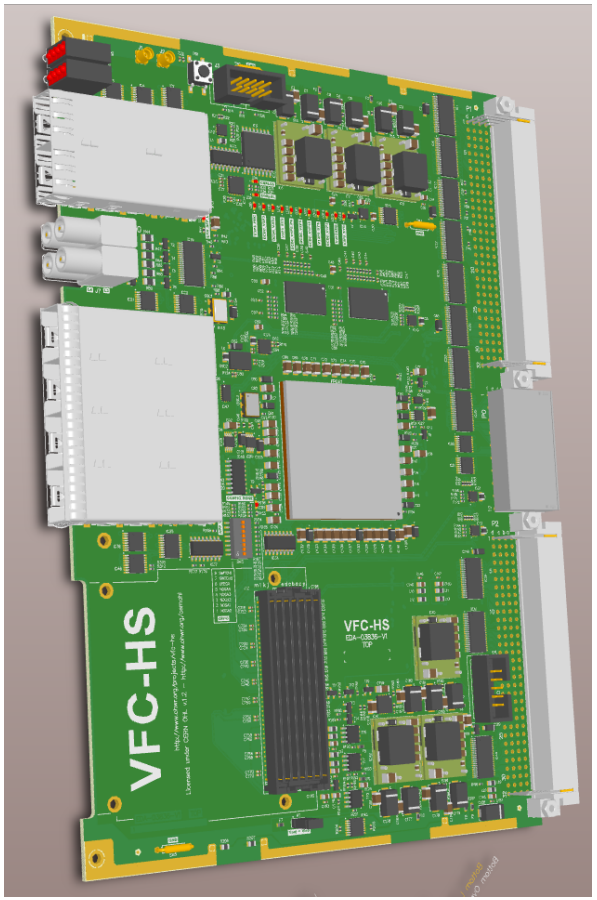
Carrier Upgrade: VFC-HS

Upgrade of VFC-HD:

- FMC+ connector
- Faster Xcvrs (10 Gbps)

- Schematics done, layout nearly done

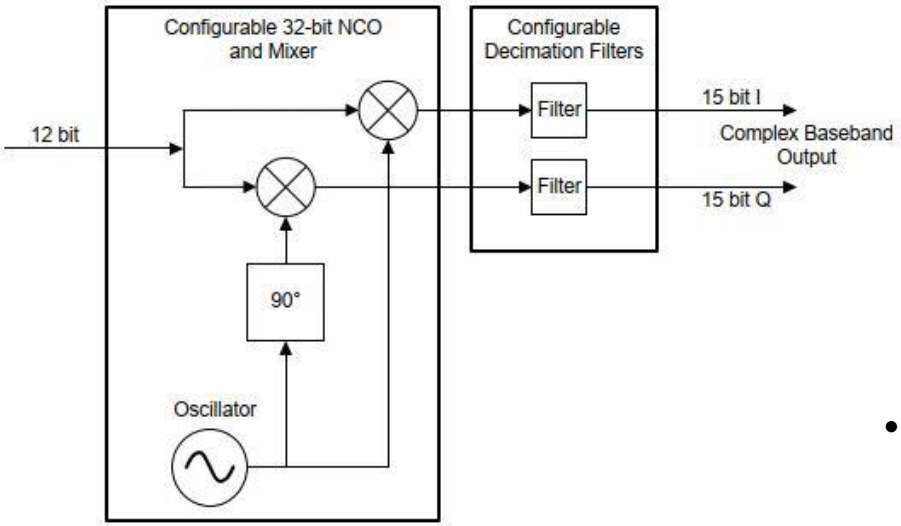
Ref: https://www.ohwr.org/projects/vfc-hs



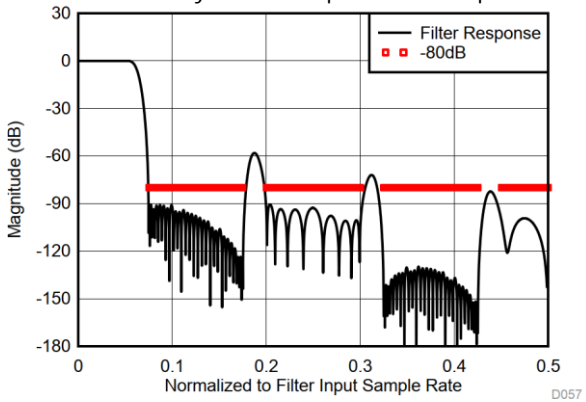
DDC and IQ measurements

Vadatech 15 bit IQ @4 Gsps 8-DDC

DDC Block Diagram



Decimate by 8 – Stopband response



- NCO (500 MHz) + Digital Down Converting Filter (factor 8) embedded in the chip:
  - NCO @ 500 MHz, decimation factor 8, IQ 15 bit
- DDC filter too narrow, time response bigger than comb filter response

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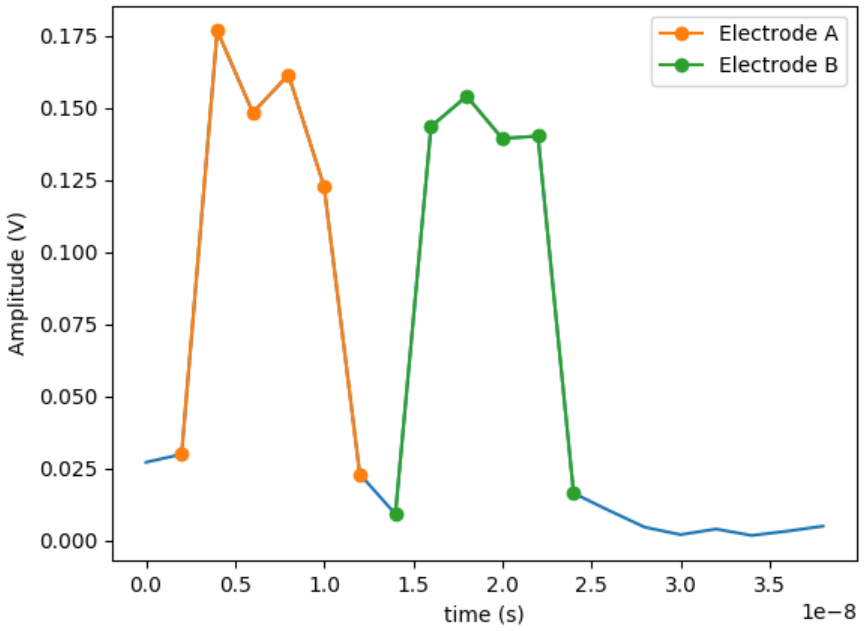

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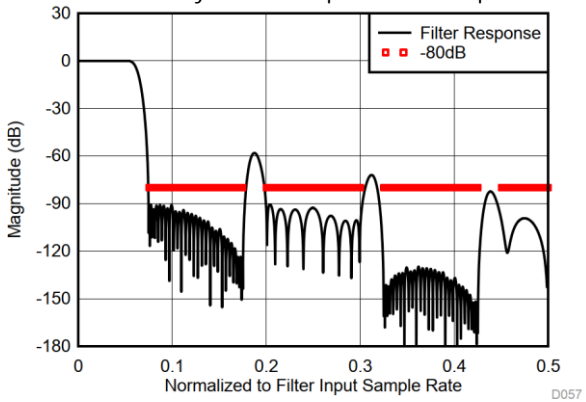

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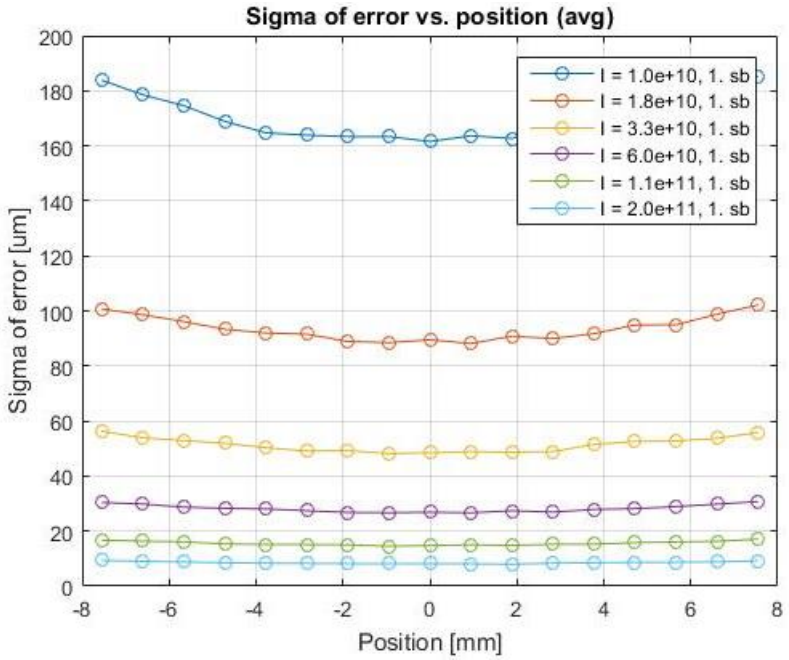
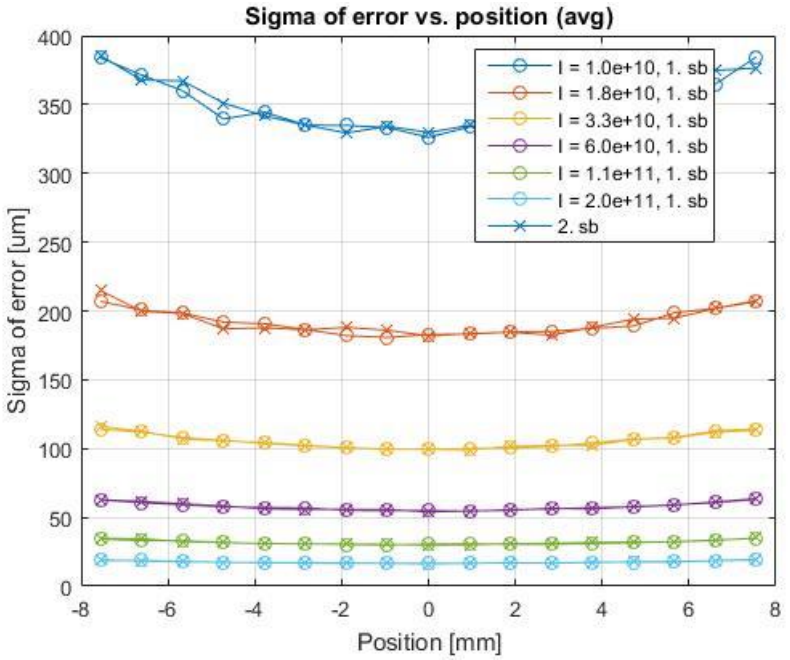
Doublets simulation



One Singlet Bunch

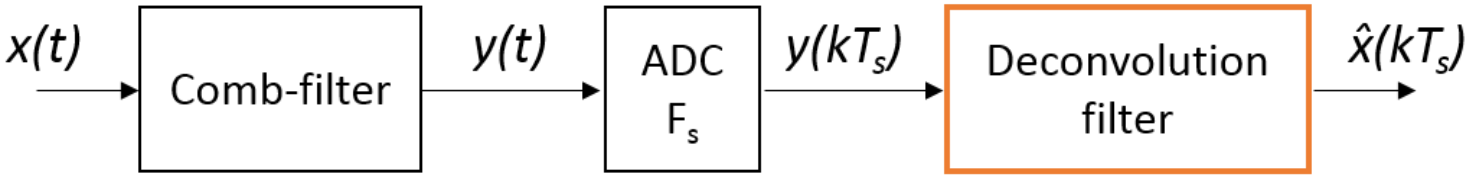


One Doublet Bunch (two sub-bunches)

RMS on one exact period

- 4 time less samples than in the singlet case
- Half the resolution

Deconvolution Methods



- Interpolation + IIR filter

$$\hat{x}(kT_s) = y(kT_s) - \boldsymbol{A_1}\hat{x}((k-\boldsymbol{K_1})T_s) - \boldsymbol{A_2}\hat{x}((k-\boldsymbol{K_2})T_s) - \boldsymbol{A_3}\hat{x}((k-\boldsymbol{K_3})T_s)$$

$$H(z) = \frac{1}{1 + A_1 z^{-K_1} + A_2 z^{-K_2} + A_3 z^{-K_3}}$$

- FIR filter: numerically computed as the inverse of the Comb-filter transfer function.