# Overview on camera sensor technology

**Walter Tutsch, PCO AG**

Krakow 2019, April 1st

# Overview

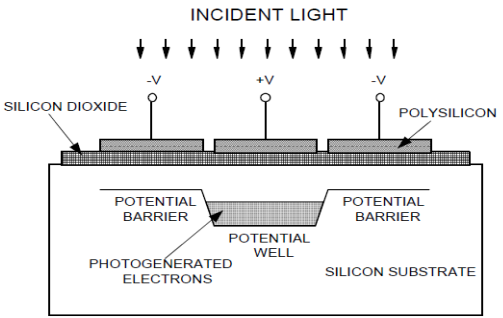
- CCD
- EMCCD
- scientific CMOS
- fast data interfaces: CameraLink HS
- sCMOS application in MCP based intensified cameras
- Summary

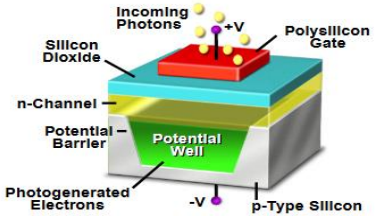
# CCD

## Charged-Coupled Device

# CCD

**Single Pixel Elements (Photodiodes) collect charges.**
**Parallel & serial charge shift to (single) A/D converter.**



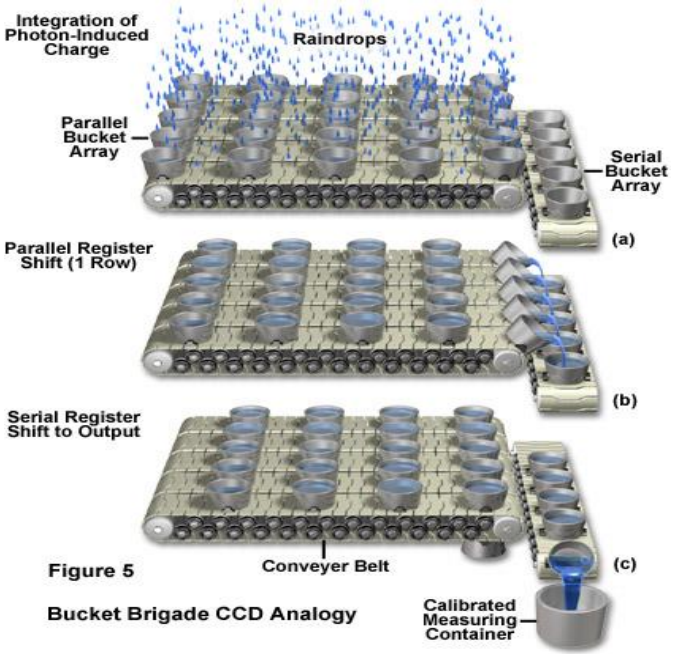




Figure 5

Bucket Brigade CCD Analogy

## Architecture of an interline transfer CCD Sensor

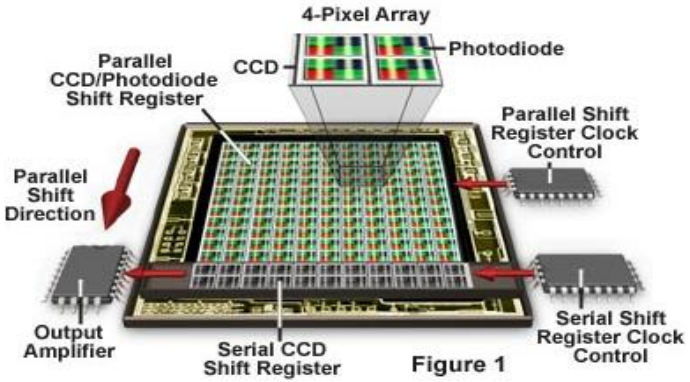
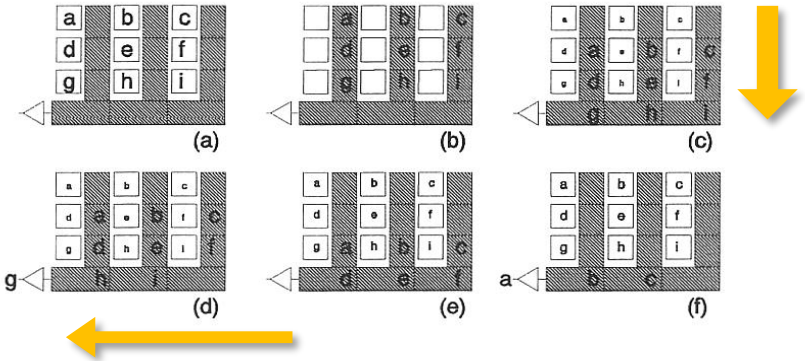



Figure 1



# CCD

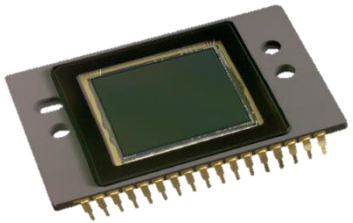
## PRO

- **low spatial noise**
  (homogeneous images due to single ADC)
- **low dark current**
  (thermally generated electrons)
- **high linearity** (signal intensitiy has a linear response to incident photons)
- **binning possible**
  (addition of charges before readout)
- **suitable for long exposure times**
  (> 10s)
- **short exposure times**
  (interline transfer CCD: ~500ns / 1 µs)

## CONTRA

- **slow readout (= slow frame rate)**
- **smear / blooming (low protection against oversaturation of pixels)**
- **manufacturing process is costly (compared to CMOS sensors)**

Sony ICX285



Kodak KAI-4022

# A letter from Sony…

**Notice of discontinuation of Sony Semiconductor Corporation's Kagoshima wafer production line ( CCD 200mm line )**

January 30, 2015

Dear Valued Customers:

Thank you for your all of effort as always. Let us begin by expressing our gratitude for the business we have established together thus far.

As noted below, recently we have reviewed the business situation in Device Solution Business Group under Sony Corporation.
We are afraid we will discontinue operations of the CCD 200mm wafer line at Kogoshima Technology Center in Sony Semiconductor. By the end of March 2017, we will cease production of devices currently being manufactured on this line.

We would kindly like to ask for your cooperation in working with us for the final production of each device on this line. Please contact the appropriate sales persons in Device Solution Business Group under Sony Corporation if needed. We really thank you again, and hope to keep working together for even future business.

Sincerely,

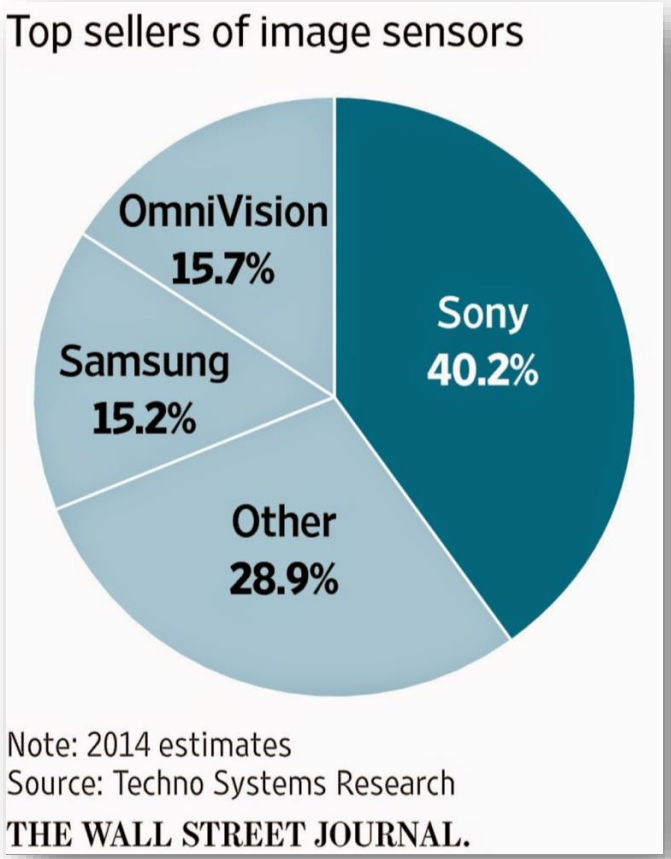
#Production Line: **Kagoshima Technology Center CCD 200mm wafer line**
( Related Devices : Please refer to the attached form. )

#Schedule: LTB Quantity to be due by **End of August 2015**
( The demand with the responsibility to buy )

Discontinue operations at wafer line by **End of March 2017**

Last shipment of the finished product by **End of March 2020**
( Acceptance day of the last order by **End of September 2019** )

Yasuhiro Ueda
SVP, Corporate Executive
Senior General Manager
Image Sensor Business Division
Device Solutions Business Group
Sony Corporation




**Sony annouces end of CCD production**

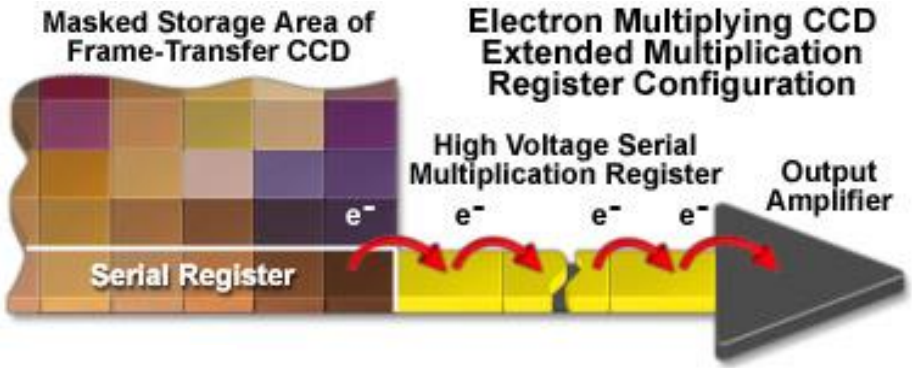
# EMCCD

## Electron-Multiplying Charged-Coupled Device

# EMCCD

Pixel design similar to standard CCD sensor

Before readout, the charges are multiplied (impact ionization) in the „high voltage multiplication register“.



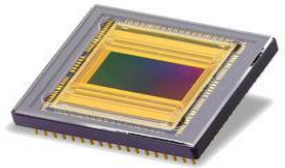
# EMCCD

## PRO

- **multiplication of signal electrons increases signal to noise ratio**
  (read noise is not multiplied)
- **user selectable gain**
  (multiplication can be adjusted based on the needs of the application)
- **extremely sensitive**
  QE up to ~95% with back illuminated emCCD
  (single photon detection possible)

## CONTRA

- **additional noise source due to multiplication process** (statistical variation of the overall number of electrons generated by multiplication register)
- **dark current**
  (thermally induced electrons are multiplied**)**
- **deep cooling necessary**
- **high gain = low dynamic range** (even small signal which is highly multiplied will saturate the pixel / ADC)



e2v L3Vision™

# sCMOS

**scientific complementary metal oxide semiconductor detectors**

# sCMOS: What makes a CMOS sensor a sCMOS ?

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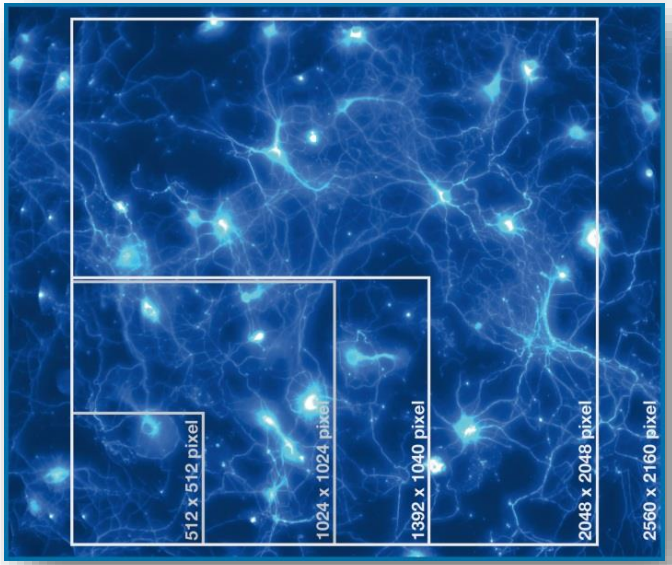
**high resolution**




**high dynamic range**



**high frame rate and high sensitivity**
– max. 150 photons & 200 fps

# HDR with sCMOS

## the technical implementation side

How to design a sensor with such a high **Intra-Scene Dynamic** ?

$$dyn_{image\ sensor} = \frac{full\ well\ capacity\ [e-]}{readout\ noise\ [e-rms]}$$

There are two „tuning knobs“:

1. Design pixel with high full well capacity
2. Reduce the readout noise to a minimum

# HDR with sCMOS

## the technical implementation side

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### 1. Pixel with high full well capacity

- from a simple geometric aspect, full well capacity is correlated to the pixel size:

➡ the higher the desired full well capacity is, the larger the pixel size has to be, **BUT**...

- large pixel show higher dark current
- large full well capacities require sufficiently large capacitors for intermediate storage and transfer of the photo electrons but ...
- large capacitors reduce the gain in µV/e-
- large capacitors increase ***kTC noise*** which is the main source of readout noise

➡ This is like a dead race !

# HDR with sCMOS
## the technical implementation side

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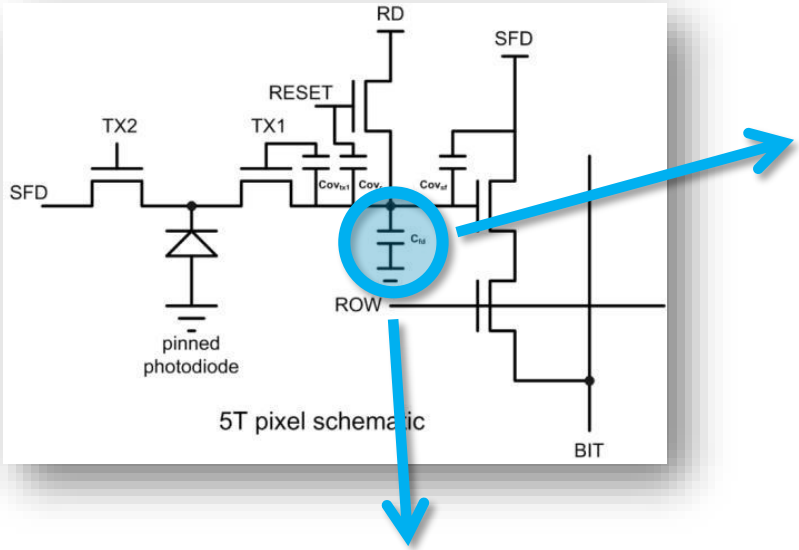
### 2. Reduce the readout noise to a minimum




**Check list for the Floating Diffusion capacity**

- must be large enough to hold full well
- small enough to avoid too high kTC noise
- small to allow for high gain (µV/e-)

quick calculation for CIS2521:

- total capacity C ~ 4fF, maximum voltage U ~ 1.2V

$Q_{FW} = C \times U$ => $Q_{FW}$ = 29.600 e- **o.k.**

- $Q_n = \sqrt{k_B T C}$ , $Q_n$ ($k_B$, 300K, 4fF) = 25e- rms **o.k.**
- 1.2V/29.600e- = 40µV/e- o.k.

**How do I get rid of the remaining 25e- rms kTC noise and reach the 1 – 2 e- rms level of sCMOS ?**

Reset (kTC) noise can be minimized by correlated double sampling (CDS)
= subtraction of signal level and previous reset level

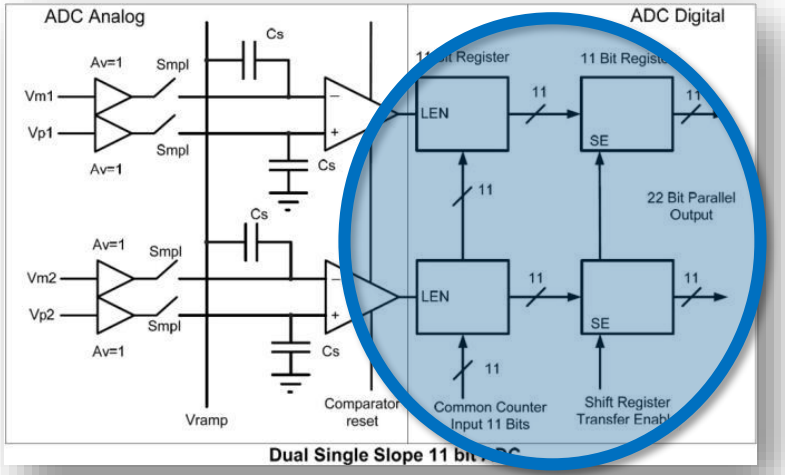
# HDR with sCMOS

## the technical implementation side

$$\mathrm{dyn}_{\text{sCMOS image sensor}} = \frac{\text{full well capacity [e−]}}{\text{readout noise [e−rms]}} = \frac{30.000\ \text{[e−]}}{1\ \text{[e−rms]}} = 30.000\ (89.5\text{dB})$$

**How to digitize the 16bit intra-scene dynamic range of the sensor ?**

**technical limit:** A/D converters implemented on a sCMOS sensor can not exceed 11bit dynamic because of power consumption, size, heat dissipation...




- The row output signal is fed into two 11bit A/D converters in parallel.
- One gets the original (low gain) signal,
- the other gets the original signal amplified x 30 (high gain).
- The outputs of both 11bit A/D converters can be matched together to cover the full 16bit dynamic range.

# HDR with sCMOS
## the technical implementation side

**Additional benefit of the parallel 11bit readout:**

Two 11bit A/D converters can be operated at a lower frequency than a single 16 bit A/D converter (at constant output frame rate)

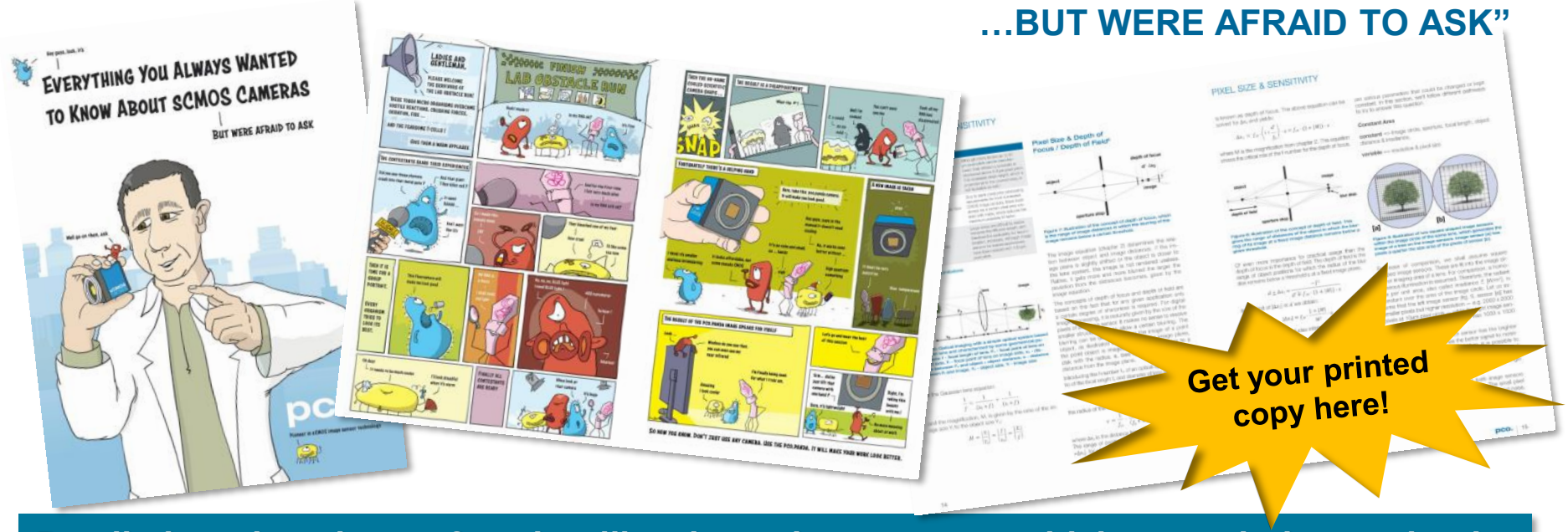
11bit conversion with „low“ frequency produces less noise as it allows for longer setting times in the comparator of the ADC

**What makes a conventional CMOS sensor a scientific CMOS ?**

It‘s mainly the adjustment and fine tuning of CMOS transistors to the needs of extreme sensitive and precise pixel readout in combination with dynamic enhancing ADC techniques and QE improvements (fill factor + micro lens).

# more knowledge in our sCMOS eBook…

## "EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT sCMOS CAMERAS …BUT WERE AFRAID TO ASK"




**Detailed explanations of topics like dynamic range, sensitivity, resolution and a lot more of sensor and imaging relevant content.**

# Scientific CMOS image sensors

## BAE Fairchild & GPixel

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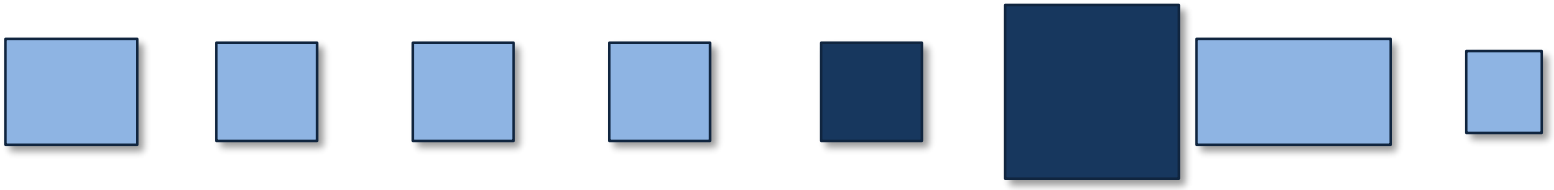
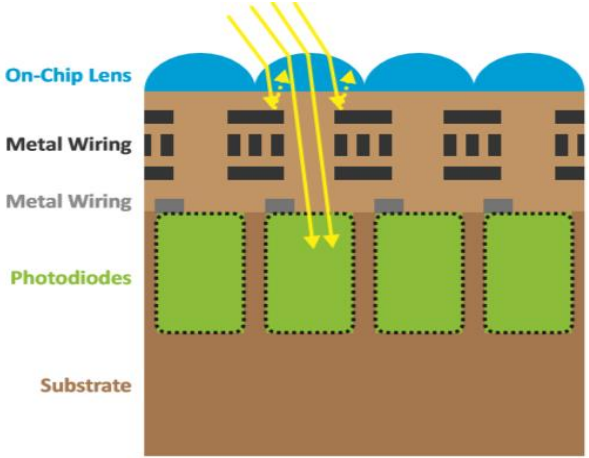
| image sensor | CIS2521 | CIS2020 | CIS2020A | GSENSE2020e | GSENSE2020BSI | GSENSE400BSI | LTN4625A | GMAX0505 |
|---|---|---|---|---|---|---|---|---|
| manufacturer | BAE Fairchild | BAE Fairchild | BAE Fairchild | GPixel Inc | GPixel Inc | GPixel Inc | BAE Fairchild | GPixel Inc |
| resolution [pixel] | 2560 x 2160 | 2048 x 2048 | 2048 x 2048 | 2048 x 2048 | 2048 x 2048 | 2048 x 2048 | 4608 x 2592 | 5120 x 5120 |
| pixel pitch [µm²] | 6.5 x 6.5 | 6.5 x 6.5 | 6.5 x 6.5 | 6.5 x 6.5 | 6.5 x 6.5 | 11.0 x 11.0 | 5.5 x 5.5 | 2.5 x 2.5 |
| active area [mm²] | 16.6 x 14.4 | 13.3 x 13.3 | 13.3 x 13.3 | 13.3 x 13.3 | 13.3 x 13.3 | 22.5 x 22.5 | 25.3 x 14.3 | 12.8 x 12.8 |
| diagonal | 21.98 mm | 18.83 mm | 18.83 mm | 18.83 mm | 18.83 mm | 31.86 mm | 29.06 mm | 18.10 mm |
| readout noise | < 2e- | 1e- | 1e- | < 2e- | < 1.6e- | 1.6e- | 2 | 1.6 |
| frame rate (full) | 100 fps | 100 fps | 100 fps | 94 fps | 47 fps @ HDR | 48 fps | 240 fps | 150 fps @ 10bit |
| rolling shutter | X | X | X | X | X | X | X | - |
| global reset | X | - | - | X | X | - | X | - |
| global shutter | X | - | - | X | - | - | X | X |
| QE (peak) | > 60% | > 70% | > 80% | 72% | 95% | 95% | > 50% | 71% |
| dynamic range | > 1 : 15000 | 1 : 30000 | 1 : 30000 | 1 : 22387 | 1 : 50119 | 1 : 44668 | 1 : 25119 | 1 : 10000 |
| fullwell capacity | 30000 e- | 30000 e- | 30000 e- | 45000 e- | 55000 e- | 89000 e- | 40000 e- | 16500 e- |
| power consumption | 2 W | 1.5 W | 1.5 W | 0.8 W (RS) | 0.85 W | 0.65 W | 2 W @ 60 fps | 1.9 W |
| monochrome | X | X | X | X | X | X | X | X |
| color | X | - | - | X | - | - | X | X |

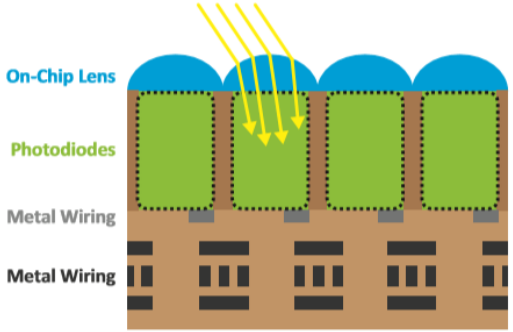
**image sensor size drawn to scale**



# back illuminated sCMOS

Why is a backside illuminated sensor more sensitive than a front side illuminated ?



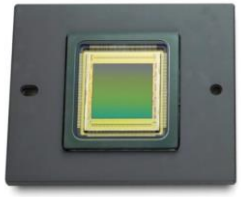





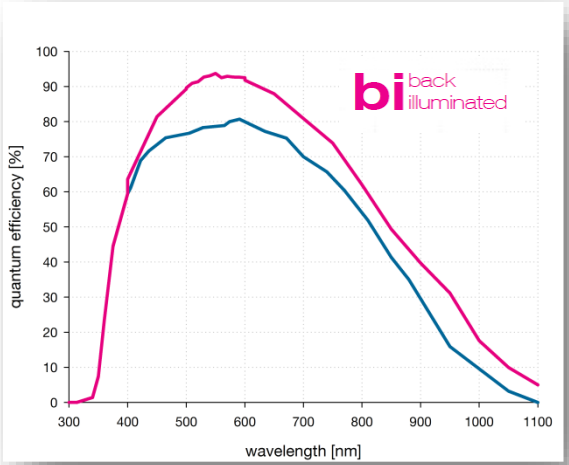
The wafer is processed with the image sensors reversed, and a large part of the substrate is physically and chemically etched away. The image sensors are then effectively illuminated from the back, and the light reaches the photodiodes more directly.

# sCMOS Cameras
## new front- and back illuminated image sensors

...allow for ultra compact non-cooled cameras with




- monochrome or color sensor
- ultra-compact size: 65 x 65 x 65 mm³
- latest 16 bit sCMOS sensor technology front & back illuminated
- high resolution 2048 x 2048 pixel
- pixel size: 6.5 x 6.5 µm²
- low readout noise 2.1 e- med
- dynamic range of 21 500 : 1
- quantum efficiency up to 95 % (bi)
- exposure times from 10 µs to 5 s
- maximum frame rate 40 fps @ full resolution
- USB 3.1 Gen1 interface
- power over USB



# sCMOS outlook

- **more resolution**
  - pixel not too small (optical resolution and dynamic range)
  - pixel not too large (dark current, „Lag“ and readout noise)
- **more sensitivity**
  - Backside Thinning, QE > 90%
- **higher dynamic**
  - elaborate collection technologies deploying e.g. additional „buckets“
- **more speed**
  - more parallel A/D converter and faster digital readout
- **reduced readout noise**

  - charge domain CDS
- **more additional functions**

  - Multi-Tap-Readout

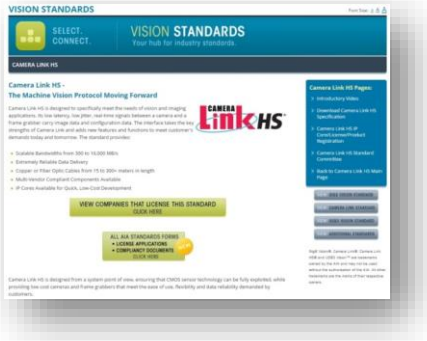
# fast optical interfaces: CameraLink HS standard

pco.

pco.edge 5.5 : a high performance cooled sCMOS camera
5.5 MPix with 16bit digitization and 100 fps generates 1.1 GByte/s data load

CAMERA Link HS®

aia VISION ONLINE
GLOBAL ASSOCIATION FOR VISION INFORMATION




| Parameter | Camera Link HS |
|---|---|
| Data Rate | 1.2 GByte/s per channel, number of channels scalable |
| Cable Length | nearly unlimited |
| Cable Type | MMF and SMF lightguide, insensitive towards electro-magnetic radiation, light weight, cost-effective |
| Hardware | standard network technology, Ethernet |
| IP Core | IP-Core in FPGAs, committee-IP-Core guarantees compatibility |
| Data Safety | X-Protocoll: Forward Error Correction (FEC) |
| Trigger Ability | Frame grabber can generate various trigger events at low jitter, various signal run times can be compensated by trigger-over-cable (from V2.0) |
| Sustainability | cost-effective hardware due to standard network technology |

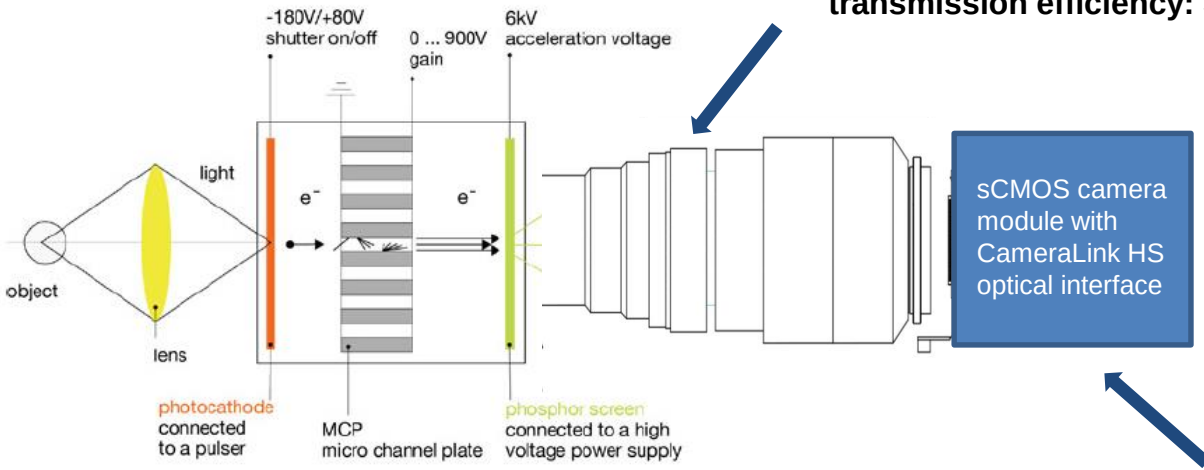
# fast optical interfaces: CameraLink HS standard


- per Camera Link HS channel appr. 1.2 GByte/s
- 4x pco.edge CLHS cameras directly on a single grabber
- 1x PCIe Gen3 (x8) slot required on PC side

# sCMOS application
## MCP based intensified cameras

- **Principle of image intensification**

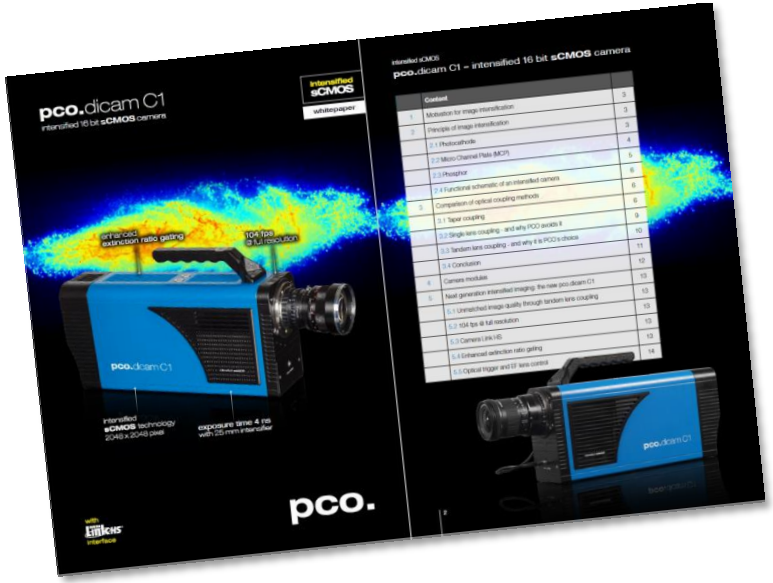
tandem relay lens
collimator lens 1, f =100mm F 1.5
imaging lens 2, f =53mm F 0.85
**transmission efficiency: 32%**

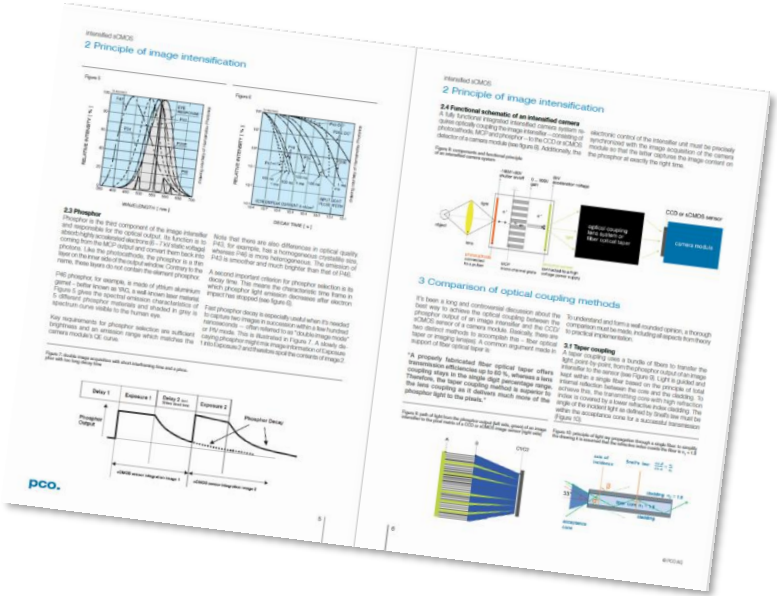



**4 MPixel, 16bit, 100fps**

# MCP based intensified cameras
## knowledge base

- **More about the principles of image intensification and optical coupling: pco.dicam C1 intensified 16bit sCMOS whitepaper available from our website**



# Summary on camera sensor technology

- There are still a few high end CCD and emCCD sensors available, some of them for very special applications like image acquisition in deep uv. But Sony‘s decision shows that we can‘t expect much further development in CCDs.

- sCMOS sensors show today (except for their dark current behaviour) much better performance data than good conventional CCD sensors, so that they have already replaced CCDs in many „low-light“ applications.

- CameraLink HS as a new data interface standard is now available to make full use of sCMOS speed.

- Even established technologies like MCP based intensified cameras benefit from sCMOS sensors.

# PCO AG Kelheim - Bavaria - Germany

Since 1987 PCO develops and manufactures high end CCD,CMOS & sCMOS camera systems for scientific and industrial research, measurement, quality control and OEM applications.

# Thank you!

# ...latest news !

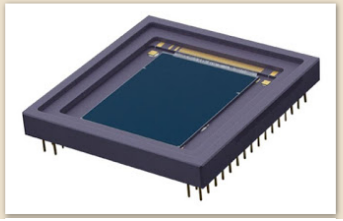
## Teledyne e2v Releases 4MP BSI Rad-Hard Sensor

Teledyne e2v has released a new image sensor, the CIS120, for harsh environments such as space applications. Samples have been available since February 2019 along with a full test and demonstration system.

Key specifications of the CIS120 include a resolution of 2048 x 2048 and BSI 10µm square pixels with a QE of 90% at 550 nm (typical). The sensor offers both a rolling shutter mode with a frame rate of 30 fps (8 bit) and a global shutter mode with a frame rate of 20 fps (12 bit).

**Key features include:**

- Good latch-up immunity and high SEU threshold by design and is resistant to ionising radiation by process choice
- Pixel read timing is set by an on-chip sequencer to simplify use and to reduce pin count
- A column parallel ADC is controlled by its own sequencer
- Resolution can be set anywhere from 8 to 14 bits
- Four LVDS channels output the image data and are controlled by the readout sequencer to scan along each row in turn.
- All configuration settings are programmed over an SPI. This includes shutter mode, ADC resolution and bias current values
- Package options include ceramic PGA and metal and ceramic three-side butting designs for use in mosaic focal planes
- CIS120 is stitched, so other sizes are possible from 2048 × 1024, up to 2048 × 8192 pixels, without the cost of new masks as well as other customer-specific requirements such as anti-reflective coatings
- An increased charge capacity of 100 ke– is possible by a metal pattern change



## TYPICAL PERFORMANCE

| | |
|---|---|
| Number of pixels | 2048 × 2048 |
| Pixel size | 10 µm × 10 µm |
| Image area | 20.48 × 20.48 mm |
| Linear charge capacity | 35 ke⁻/pixel |
| Conversion gain | 40 µV/e⁻ |
| Quantum efficiency @ 550 nm (BI) | 90 % |
| Dark current at 20 °C | 50 e⁻/pixel/s |
| Readout noise | 4 e⁻ rolling shutter<br>11 e⁻ global shutter |
| ADC resolution | 8, 10, 12 or 14 bit |
| Frame rate (rolling shutter and full frame) | 30 fps @ 8bit,<br>20 fps @ 12bit |
| Outputs, LVDS or sub-LVDS | 4 data + 2 sync |
| Output data rate | 260 Mbps/channel |
| Setup and control bus | SPI |
| Clocks | 4 MHz and 130 MHz |
| Power supplies | 3.3V and 1.8V |
| Power consumption | <280 mW (sub-LVDS)<br><350 mW (LVDS) |
| Die size (width × height) | 22.20 × 28.35 mm |

## SPECTRAL RESPONSE

A typical back illuminated spectral response (QE) with the 'Multilayer-2' AR coating is shown below: