
SSL for ATLAS

Scalable Systems Laboratory for Innovation & Integration

Rob Gardner
Enrico Fermi Institute
University of Chicago



US ATLAS Computing Facility Meeting @ Argonne
December 5, 2018



IRIS-HEP SSL Purpose

- Provide the Institute and the HL-LHC experiments with **scalable platforms** needed for development in context
- Provides **access** to **infrastructure and environments**
- Organizes software and resources for **scalability testing**
- Does foundational systems R&D on **accelerated services**
- Provides the **integration path** to the OSG-LHC production infrastructure

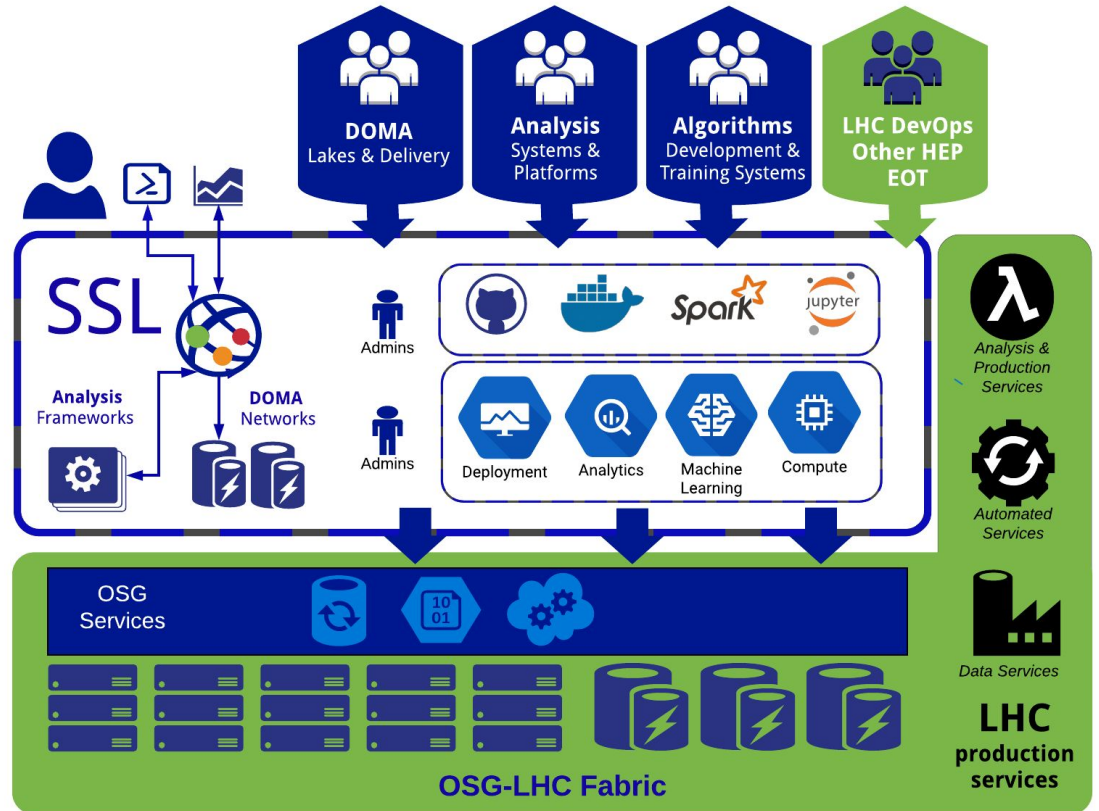


SSL: Path to Production

Provisioning of software **environments** and development tools.

Distributed platforms materialized with tools like containerized edge services.

Integration point with the OSG and LHC experiment services (data, analysis).



SSL Team & Resources

- Small core group to support base environment
- Dynamically **draws effort from R&D pillars**
- Interfaces to OSG-LHC and LHC Ops
- Organizes leveraged resources needed to scale

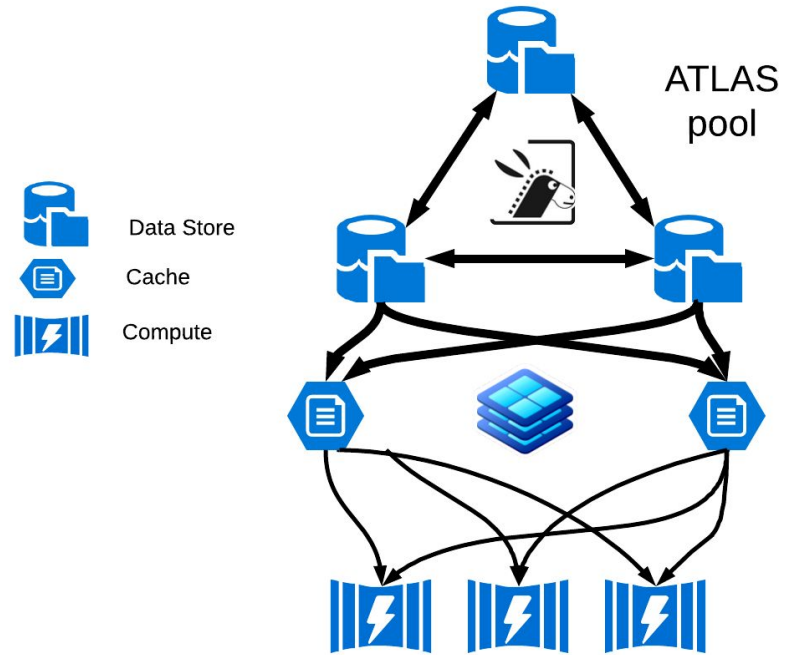


Components and Practice

- A number of core IRIS-HEP SSL services will be defined resulting from requirements gathering
 - Shared (cross-experiment, cross-pillar) dev environment
- The SSL can support the HL-LHC R&D activities of WBS 2.4

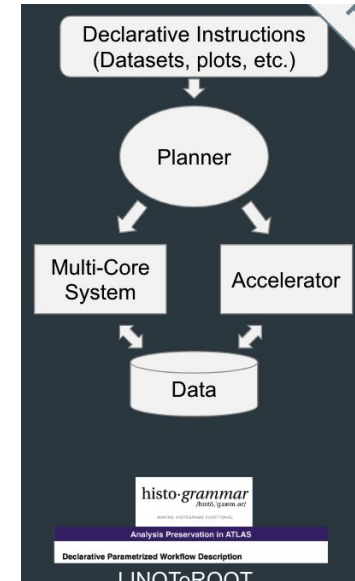
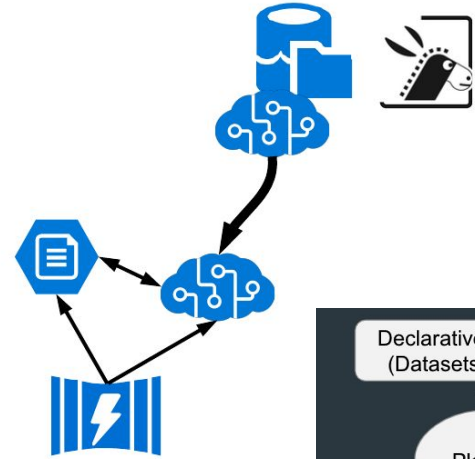
Example: DOMA simulators

- Major theme in WLCG-DOMA is R&D on new data architectures capable of HL-LHC scales
- SSL to facilitate prototyping

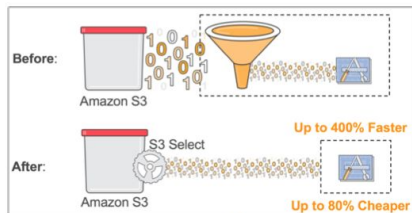


Example: systems R&D

- Another major theme is system scalability R&D
- In DOMA this might be a hardware accelerated intelligent data delivery service
- In AS this might be used in a declarative or “low-latency” analysis platform



A Cloud Example: Data Analysis



- Iterators over all objects in an S3 bucket
- S3 select
- Interesting: Pricing and business model (when you own the endpoints and network COST)

Hardware Acceleration: Big Wins

Xeon E5620 (8-thread, 340mm², 80W)



UDP (64-lane, 8.7mm², 0.86W)



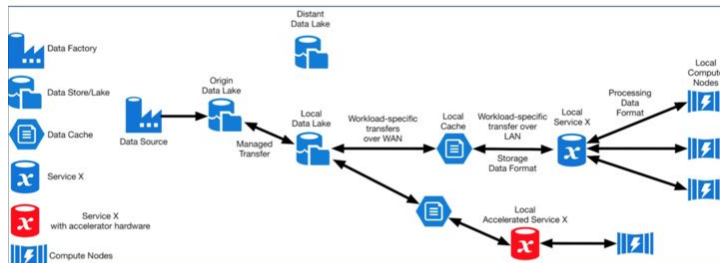
UDP Hardware Implementations

64-lane UDP	ASIC (28nm)	FPGA (Arria 10)
Frequency	1GHz	40MHz
Resource	8.7mm ² 2	109K ALM, 8Mbit BRAM

From A. Chien at impromptu IRIS-HEP discussion meeting at UChicago 9/7/18

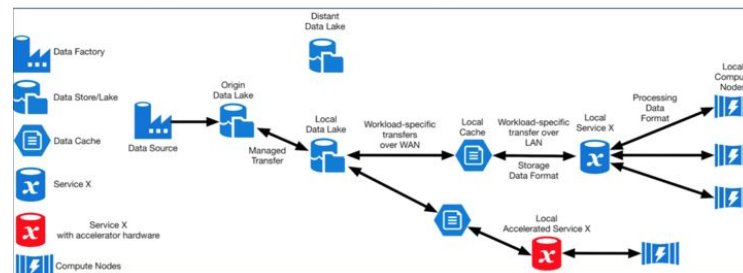
<https://indico.cern.ch/event/755728/>

What does this mean for IRIS-HEP?

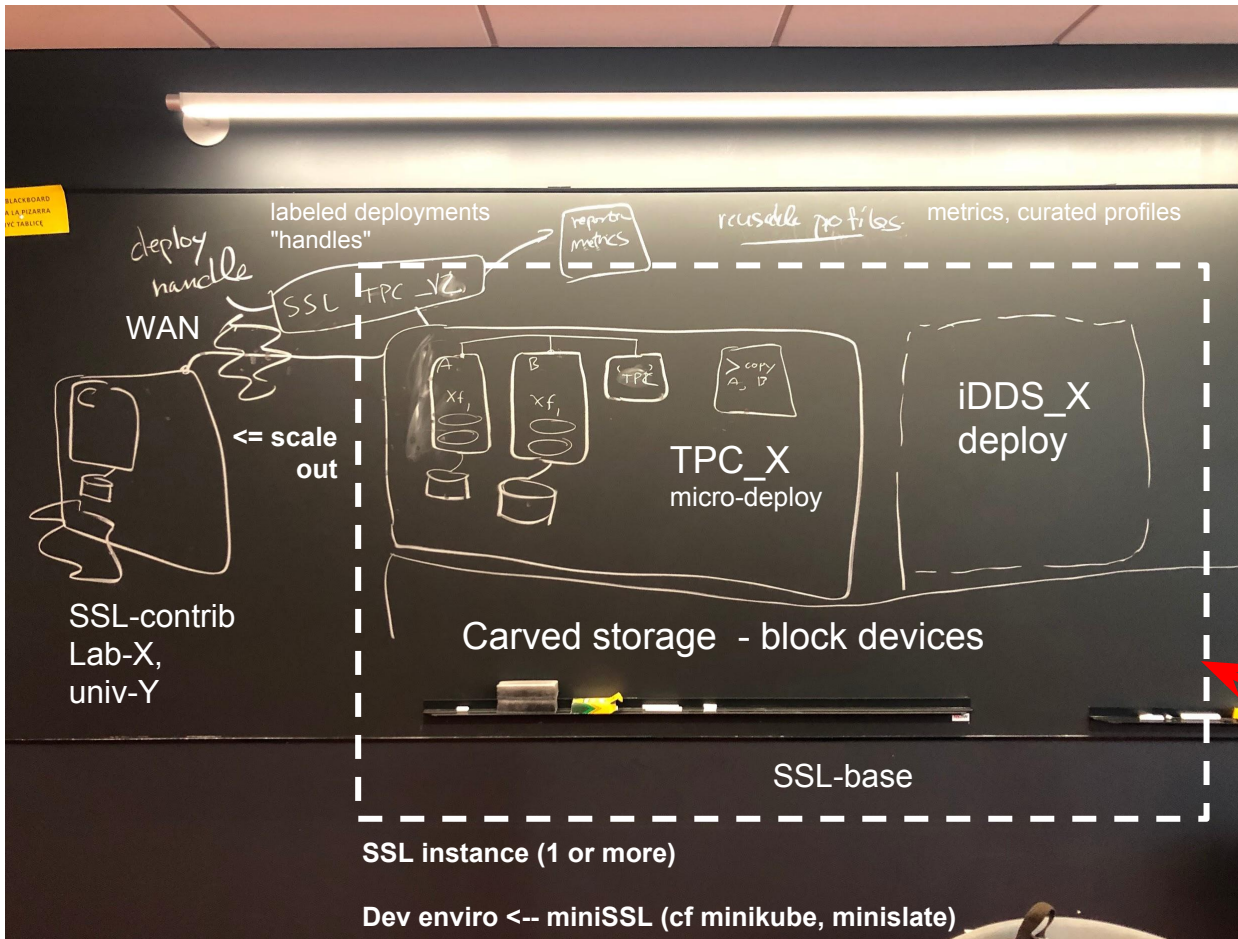


- Distributed Data Lake, Shared General Data format (across experiments)
 - Scalable analysis pulls data from Lake, and ships to computing resources [analysis]
 - Variety in analysis experiments and data use and availability of compute resources IMPLIES large data movement

Example Research Topics



- Programmable hardware acceleration [10-100x size reduction]
- => Can dramatically increase System scalability and HEP application science capability

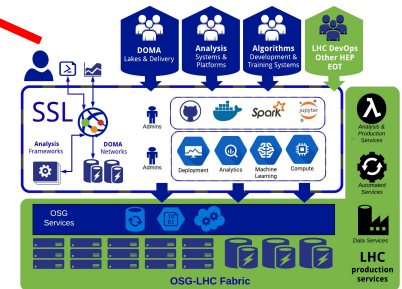


Scenario:

Develop new third-party copy software (TPC)

Requires three orchestrated
four orchestrated services plus
control host

Labeled, reproducible:
Micro deployment
WAN deployment
Scaled deployment



SSL and ADC development

- The SSL can provide a shared development and integration platform
- No dedicated hardware – must be able to dynamically assemble resources for testing, then return to production
- Next year will be figuring out how to do this smoothly