Contribution ID: **26** Type: **Exercise**

Hardware Acceleration Through FPGAs - First Experiments in VHDL (exercise 1)

Tuesday, 5 March 2019 16:00 (1 hour)

FPGAs are a more and more ubiquitous technology. They offer the benefits of fast, application-tailored hardware, typically associated with ASICs, while enabling fast prototyping, upgradability and low costs. This makes them an ideal ally in HEP computing, specifically in areas where high performance is needed and/or specifications and needs may vary.

The lectures will focus on the intrinsic parallel processing characteristics of FPGAs, emphasizing how they can be exploited to implement data-intensive algorithms. Focus will also be put on concepts like hardware/software partitioning (very important to help the most performing parts of the systems in collaborating with the legacy CPU oriented codebase).

A simple hands on exercises session will be added to let the students get acquainted with the main tools and the VHDL language.

Presenter: Mr LOPEZ, Giorgio (CERN)

Track Classification: Lectures and exercises