Trigger Primitives In Endcap

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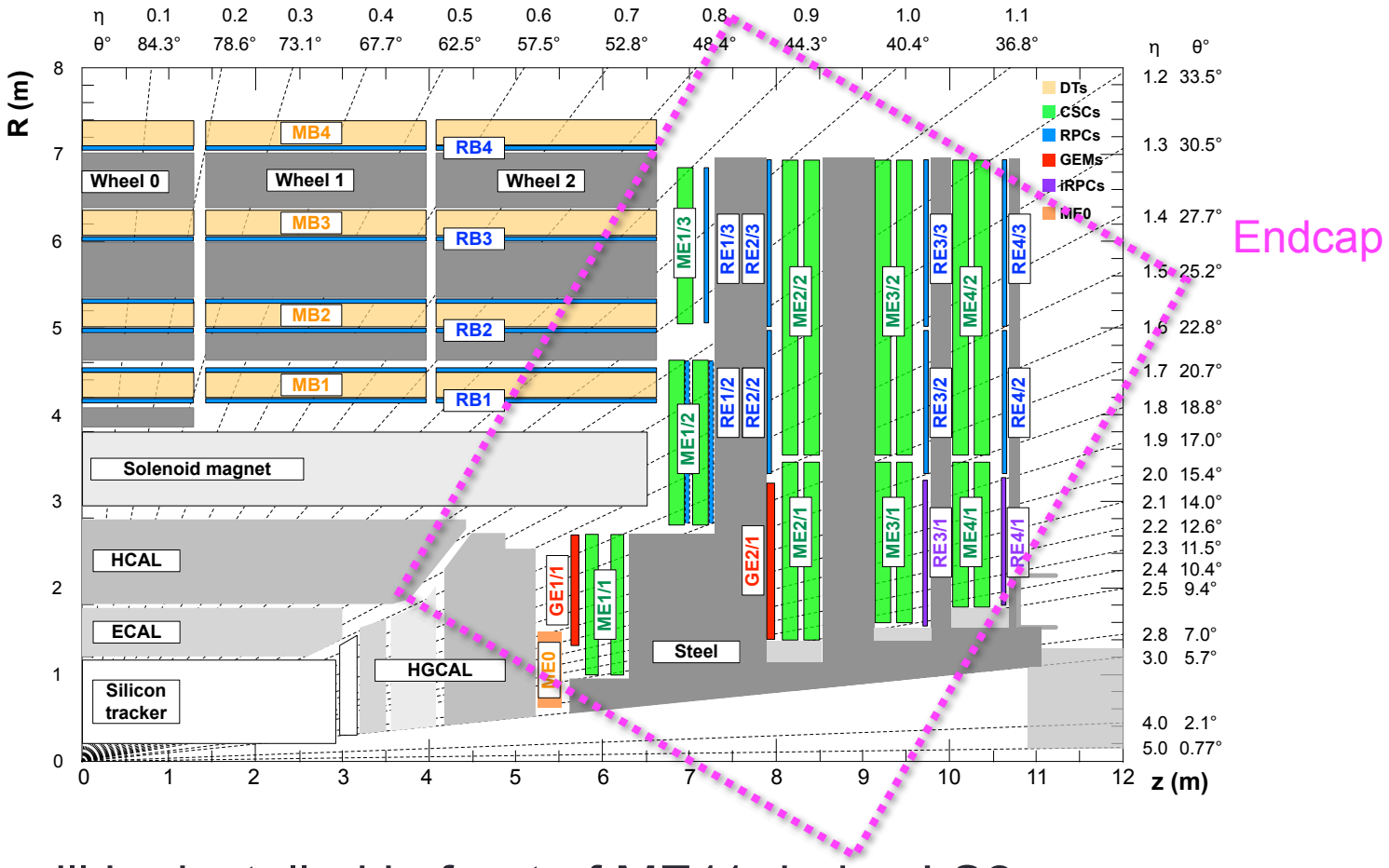
https://indico.cern.ch/event/768856/timetable/?view=standard

Outline

- GEM-based endcap upgrade overview
- Current CSC local trigger and upgrade
- GEM local trigger
- GE11-ME11 integrated local trigger
- Phase-2 upgrade

GEM-Based Endcap Upgrade Overview

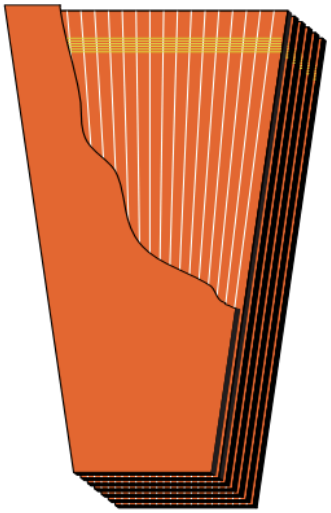


- GE11 will be installed in front of ME11 during LS2
- Phase-2 upgrade: GE21 and ME0 will be installed during YETS (GE2/1) and LS3 (ME0)

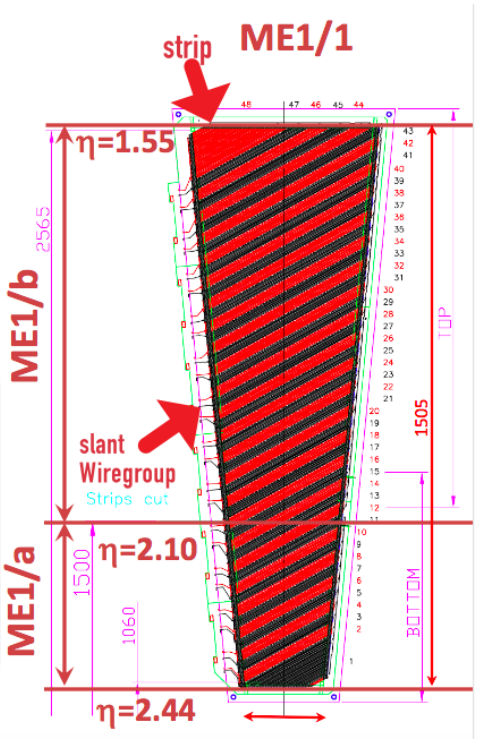
CSC Local Trigger

- Introduction
- Trigger primitive efficiency from Tag&Probe
- Local trigger upgrade (CSC-only)
- CSC position resolution improvement
- Cathode trigger threshold reduction
- CSC local trigger emulation

Cathode Strip Chamber (CSC)



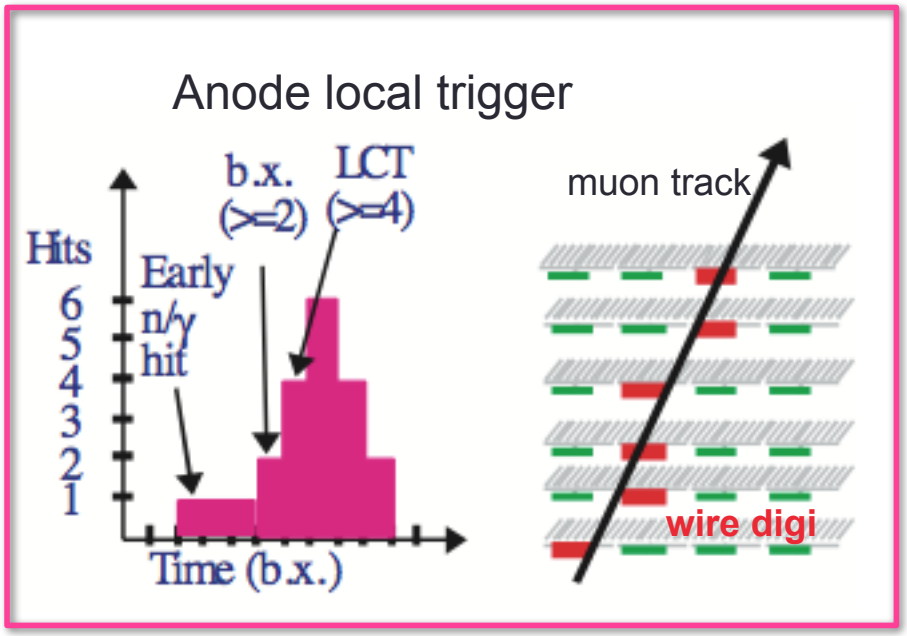
- Cathode strip chamber consists of 6 CSC layers
- Anode wires cross with cathode strips
- muons register hits on wires and strips when passing through the chamber

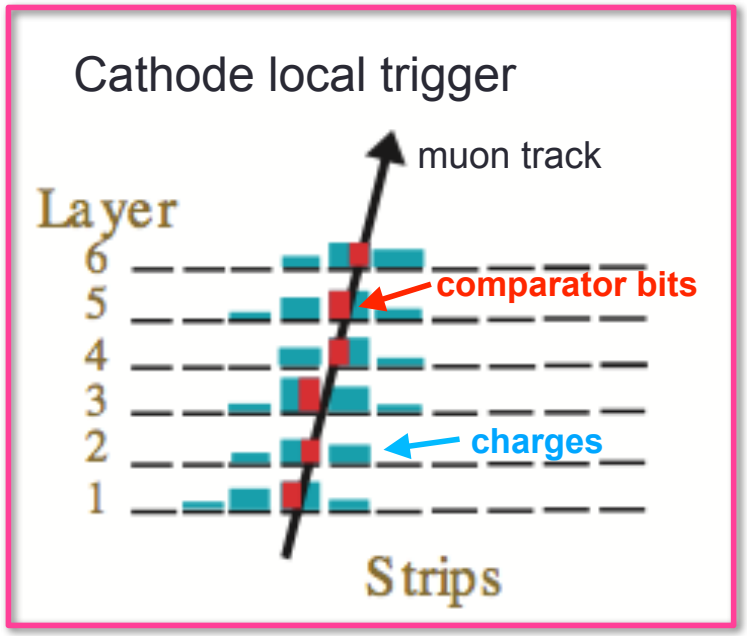


Special ME1/1

- ME11 is physically partitioned into ME1a and ME1b
- Wiregroup in ME11 is slant

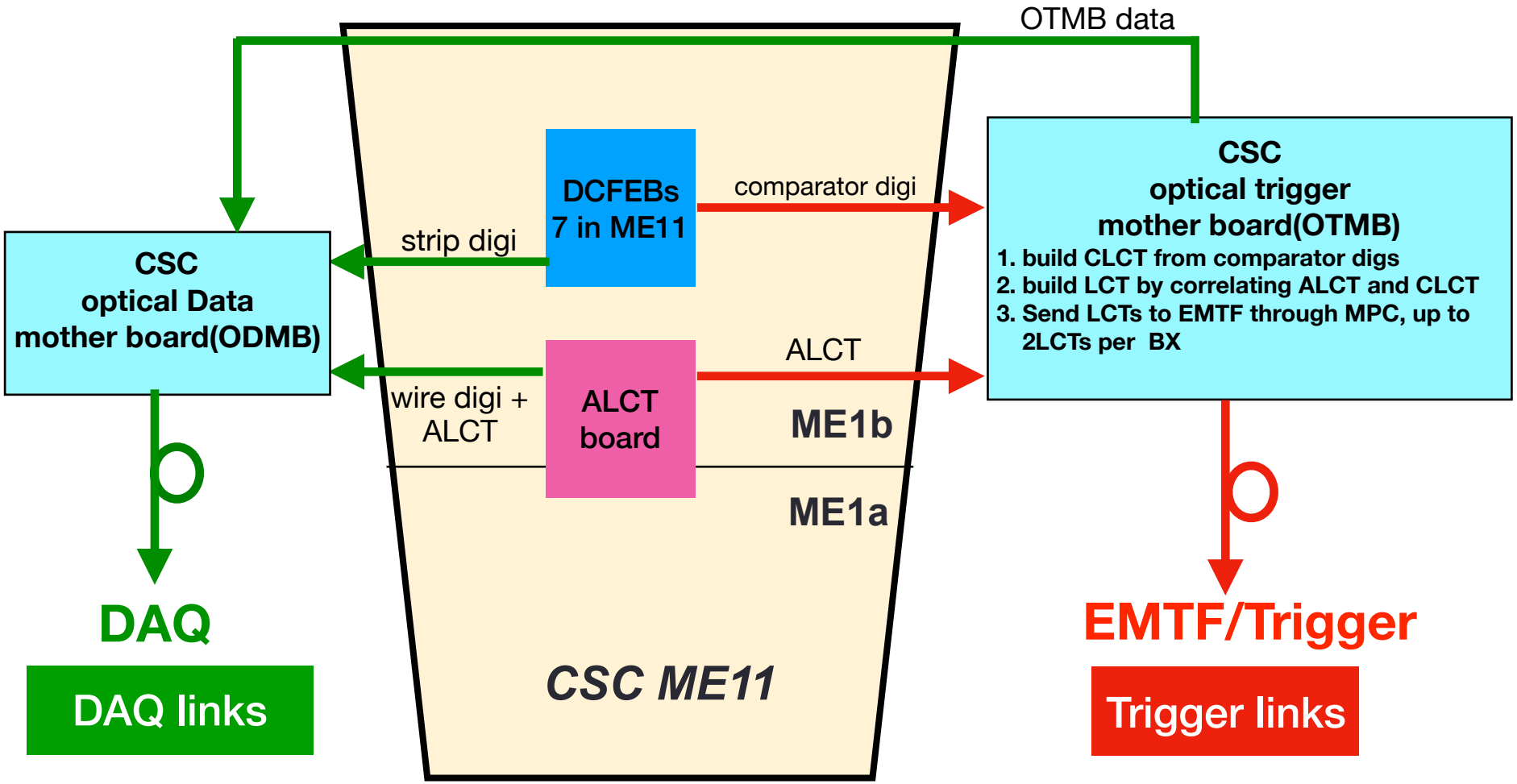
CSC Local Trigger Algorithm





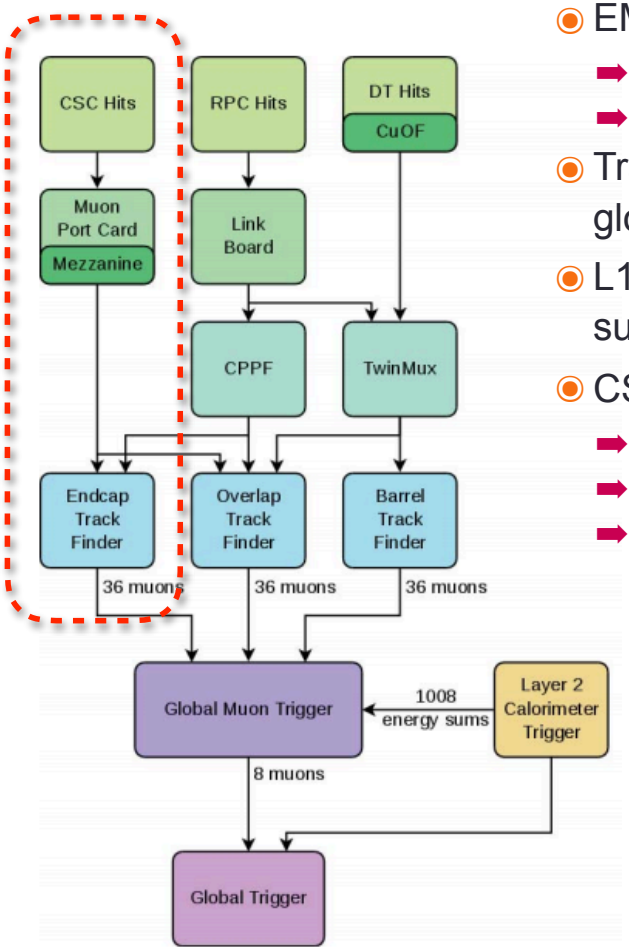
- Both ALCT and CLCT are built from pattern recognition
  - ALCT: valid anode pattern with >= 4hits out of 6 layers
  - CLCT: valid cathode pattern with >= 4hits out of 6 layers
- LCT: correlation of ALCT and CLCT within matching window in timing
- (O)TMB sends out up to 2LCTs per BX and finally LCTs are transmitted to EMTF
  - In Run-2 only ME11 uses OTMB (with optical links) and all non-ME11 uses TMB
- LCT Dataformat, 32 bits
  - Anode wiregroup number, cathode halfstrip number, CLCT pattern id, LCT quality etc

ME1/1 Electronics

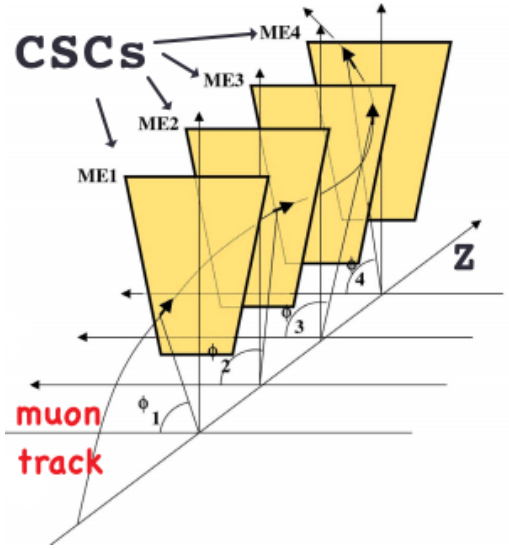


- Anode Local Charged Trigger (ALCT) built from wire digi
- Cathode Local Charged Trigger(CLCT) built from comparator digi
- Local Charged Trigger(LCT) built from ALCT+CLCT matching and finally sent to EMTF to form tracks

Endcap Muon Track Finder(EMTF) and LCTs

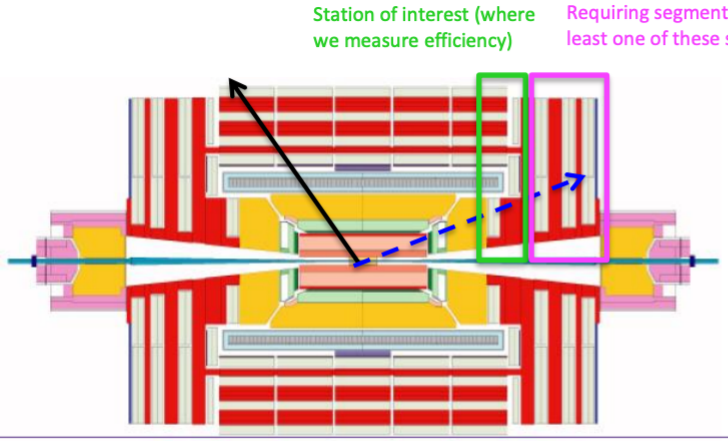


- EMTF builds muon tracks by combining LCTs from all 4 stations
  - EMTF receives LCTs through muon port card (MPC)
  - RPC hits could be optionally used
- Tracks from ETMF are sent to global muon trigger and finally to global trigger
- L1 accept(L1A) is made by global trigger and sent back to subsystem for readout
- CSC data readout, setup in P5 by default:
  - ALCT board: ALCT+L1A to read out wire digi, Anode trigger
  - (O)TMB: CLCT+L1A to read out comparator digi, cathode trigger, LCT
  - (D)CFEB: preCLCT+L1A to read out strip digi



Tag and Probe Method For LCT Efficiency

Isa, Stephen etc. UW



Probe (= Tracker track extrapolated to CSC system)

- p>8GeV, |η|<2.4, dxy<2cm, dz<24cm,
- Track fit normalized chi2<4
- number of strip tracker hits>7, number of strip tracker and pixel tracker hits>9
- $\Delta\eta<0.003$, $\Delta\phi<0.003$, $\Delta p_T/p_T<0.05$
- charge opposite to tag muon charge
- 0.2<ΔR(tag, probe)<10.
- Z: 75GeV<M(tag+probe)
- Extrapolated track in CSC active region -> definition in backup
- For LCT efficiency: no other track is closer to LCT
- At least one other station (other then station of interest) has segment matched to "probe"
- TrRelsoR(ΔR<0.3)<0.4

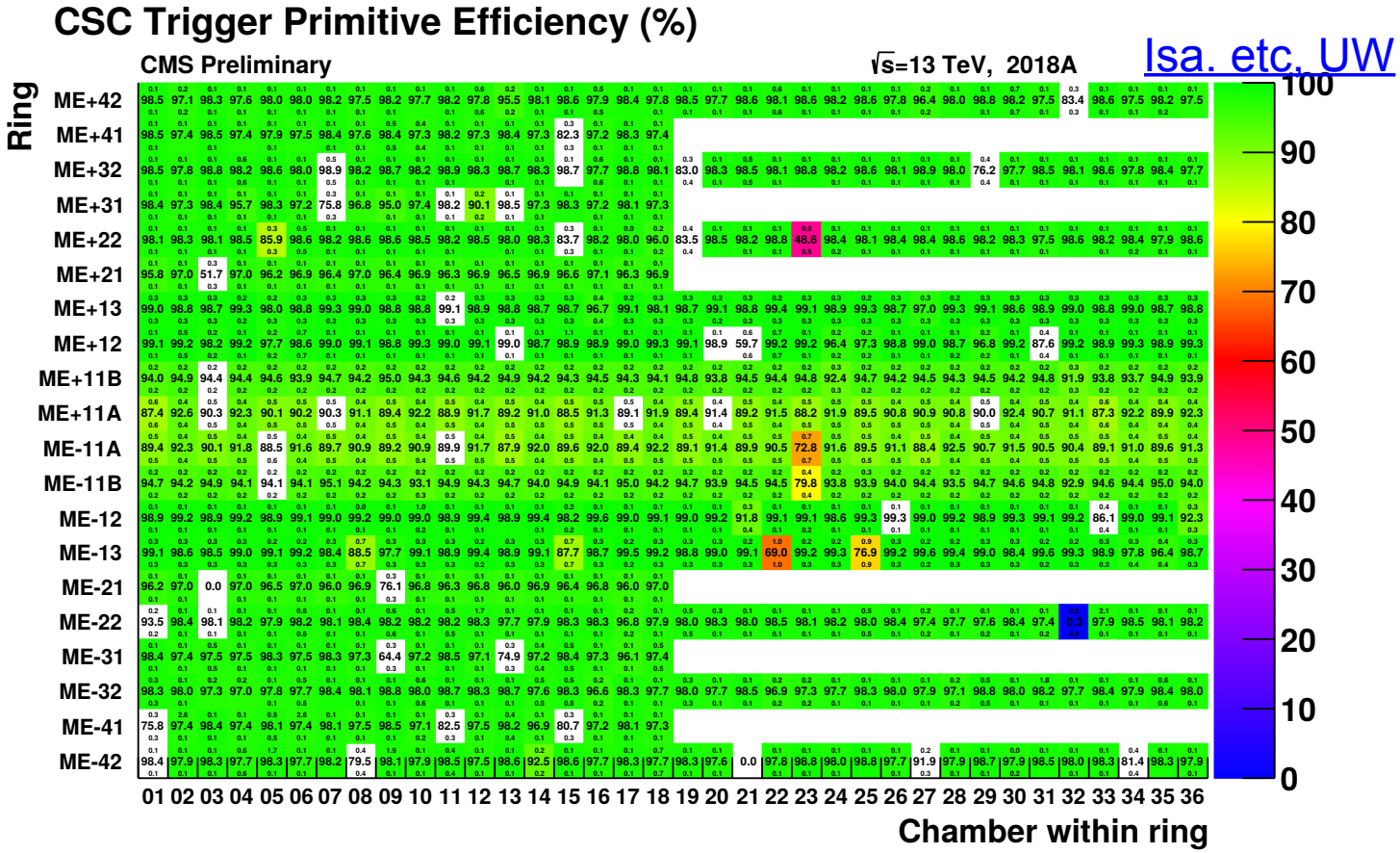
Passing probe:

- Distance(segment/LCT, track)<Max(5cm, 5sigma)

Tag muon (= Tracker muon)

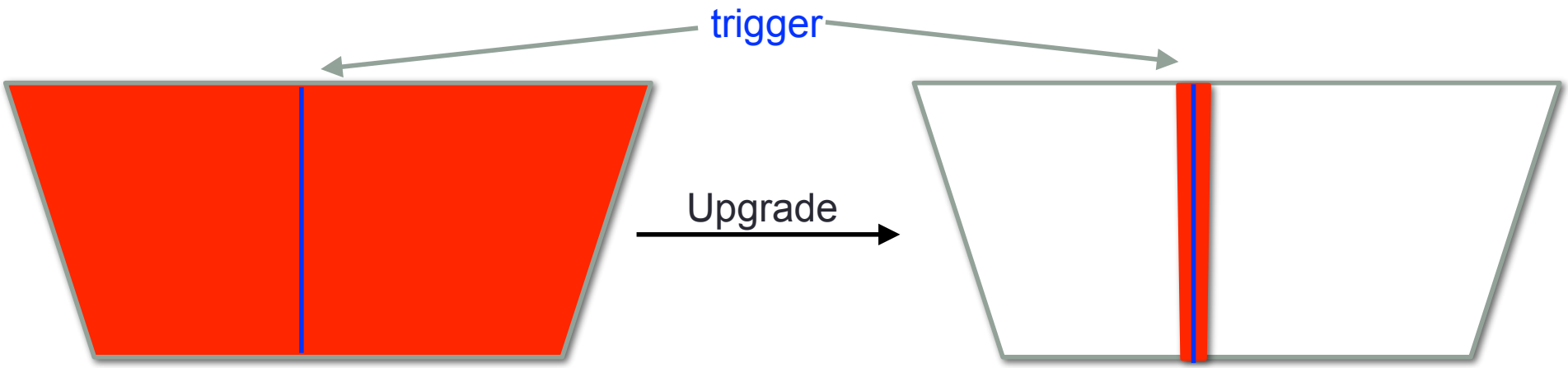
- Tracker muon
- pT>5GeV, dxy<2cm, dz<24cm
- fit normalized chi2<4
- number of strip tracker hits>7
- number of matched muon segments>2
- ΔR(to any single muon trigger objects)<0.01
- PFIsoR(ΔR<0.4)<0.15
- TrRelsoR(ΔR<0.3)<0.4

LCT Efficiency from Tag&Probe: 2018RunA



- Non-ME11 efficiency : ~98%
- LCT efficiency in ME1a region is only ~90%, quite low! in ME1b: ~95%
  - ➡ Big concern as LHC is moving to high luminosity regime
- In usual 2018 runs ME11 LCT rate @ Instant Lumi ~1.5e34 $cm^{-2}s^{-1}$(<PU>~36) is ~300kHz per chamber

Local Trigger Algorithm Upgrade: Regional Dead Time

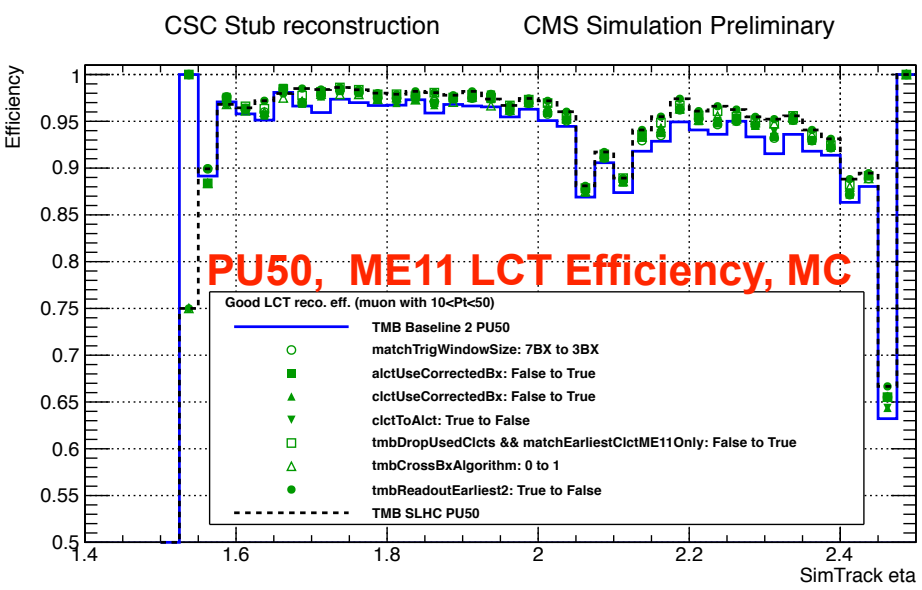


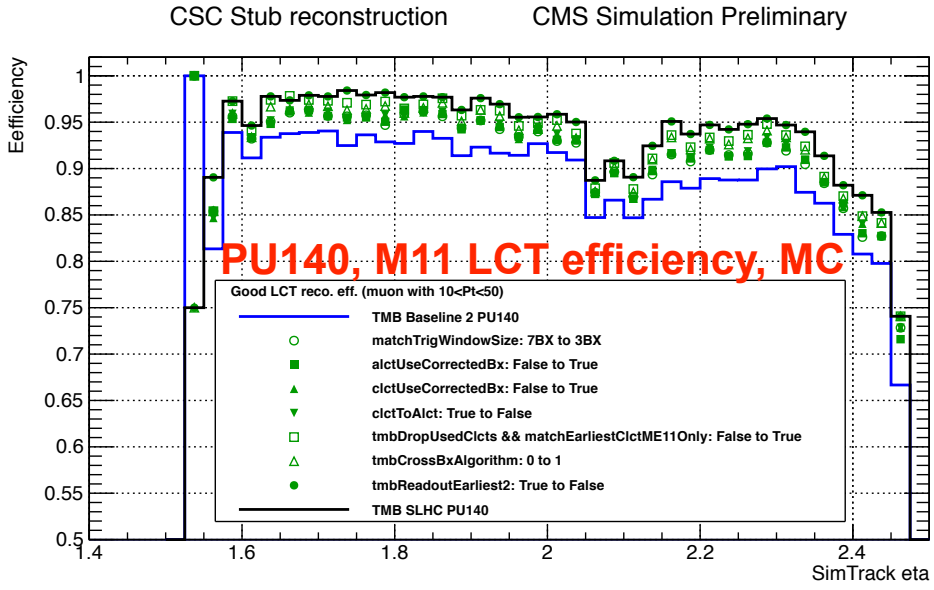
Current algorithm:
whole chamber is **busy** after one trigger

New algorithm:
only region around trigger is **busy**

- Current algorithm: freeze the whole chamber for a few BX after one trigger=> a few BX dead time after one trigger
  - ➡ Dead time caused by pileup muons would result in efficiency loss for high pT muons
  - ➡ Impact of dead time on efficiency could be more significant in high PU
- New algorithm: freeze the region around trigger and other region is active for next trigger immediately => only regional dead time
  - ➡ New algorithm could largely recover the efficiency loss due to dead time in principle

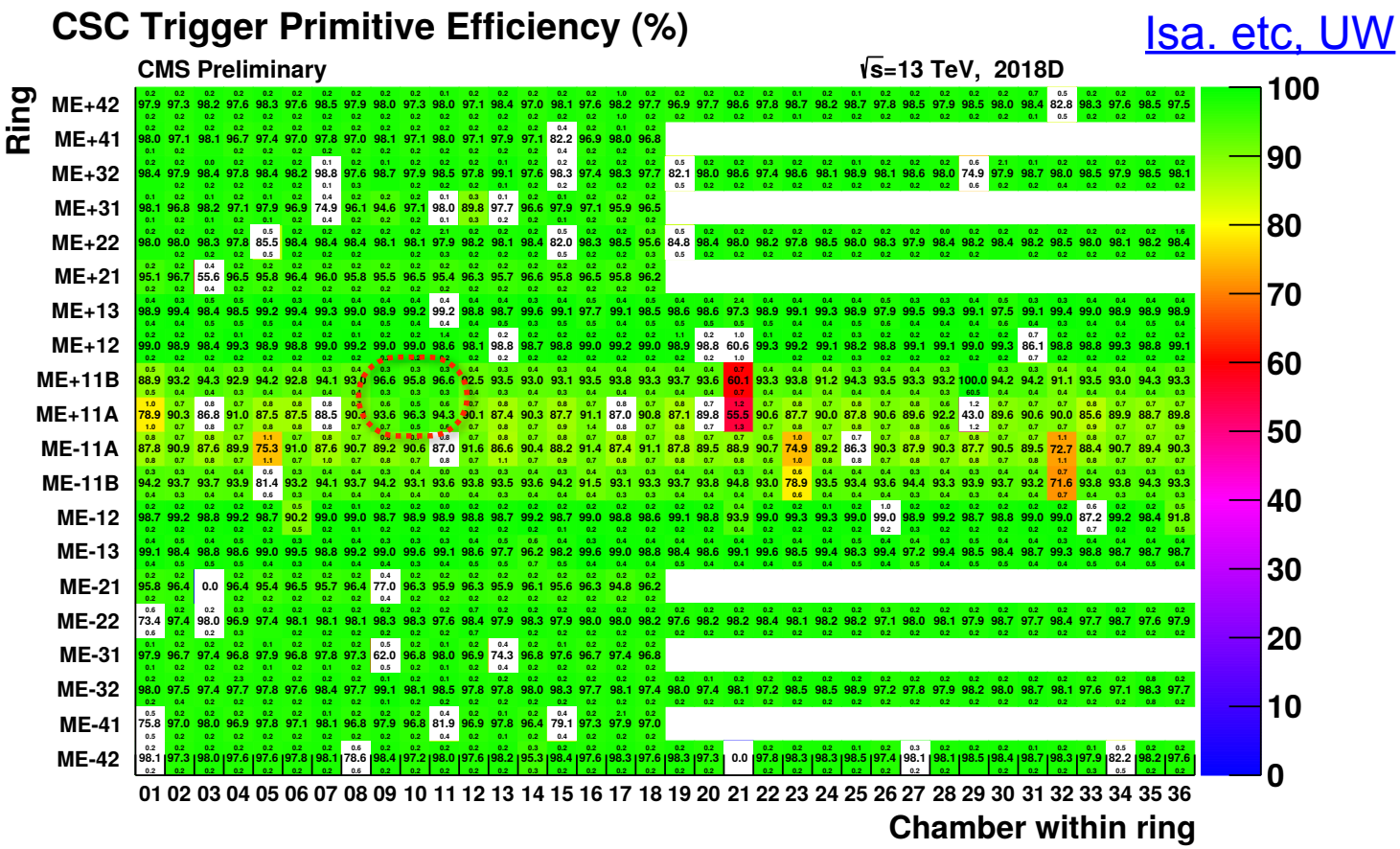
Simulation Predictions





- Considering the harsh environment in high luminosity run, CSC local trigger upgrade was firstly proposed back to 2013, with simulation study
  - ➡ New algorithm was already implemented in cmssw and could be optionally switched on
- Based on simulation, new algorithm could improve the LCT efficiency significantly at PU140
- 2018OTMB is built by implementing new algorithm in firmware and is tested at b904, GIF++ and P5
  - ➡ 2018OTMB only modified local trigger algorithm and used the same FPGA as current one did
  - ➡ No changes in data formats, both trigger path and DAQ path
  - ➡ 2018OTMB firmware was loaded to ME+1/1/09, 10, 11 since 2018 Sept.

LCT Efficiency From Tag&Probe: 2018RunD



Isa. etc, UW

- Above LCT efficiency was measured after 2018OTMB firmware was loaded to ME+1/1/09, 10, 11 in P5
- LCT efficiency of ME+1/1/09, 10, 11 is higher with 2018OTMB firmware, especially in ME1a region
  - ➡ No sizable LCT rate increase due to 2018OTMB firmware in usual 2018 runs, from CSC operation observation

LCT Efficiency Improvement of 2018OTMB From Tag&Probe Method

ME+1/1/09 was loaded with new firmware since July 25th

Chamber	2018A	2018D (25/07 - 23/08) run 320673 - 321461
ME+1/1A/09	89.4%	94.3%
ME+1/1B/09	95.0%	96.3%

Isa. etc, UW

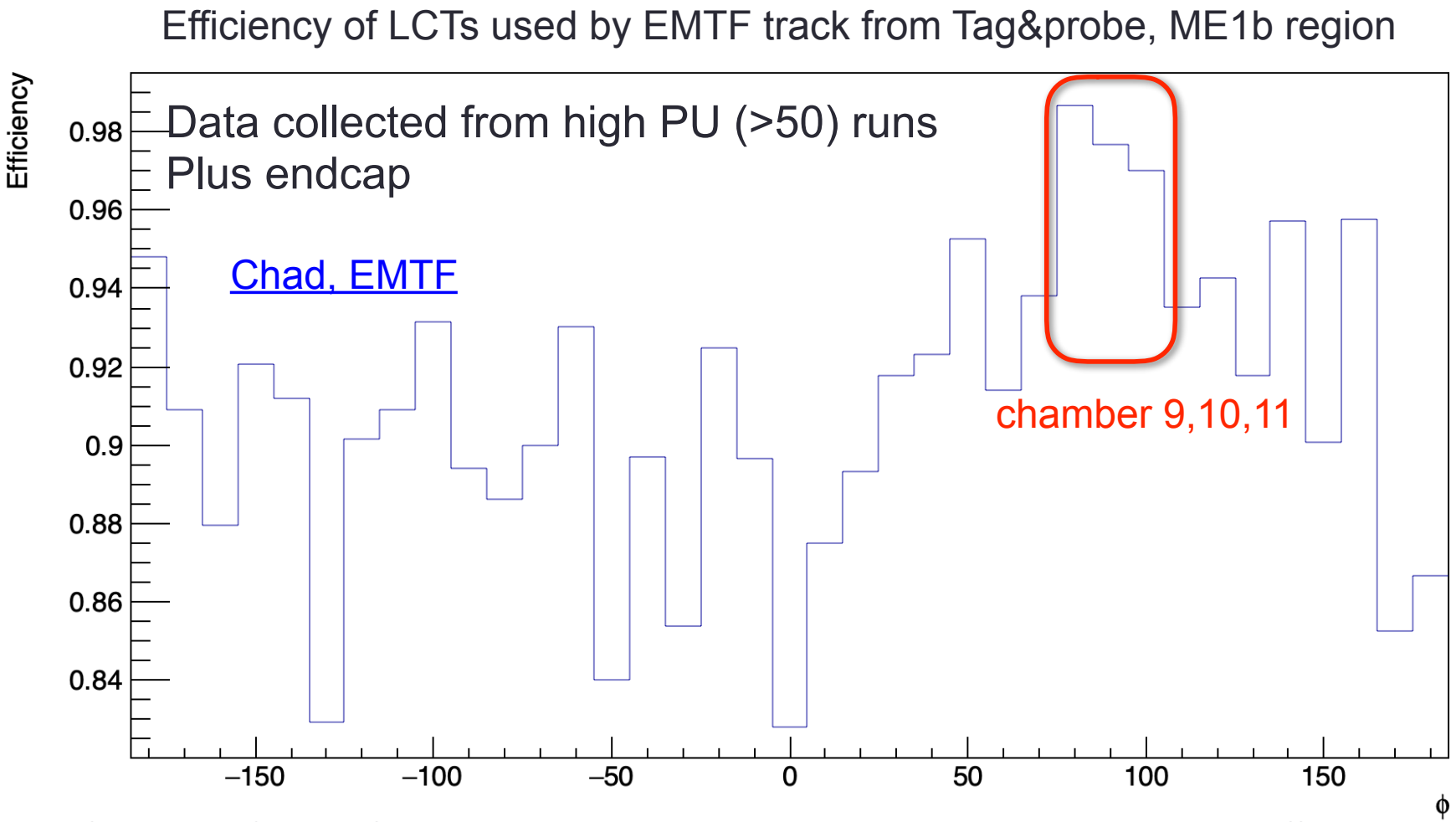
Chamber	2018D before TS2 run 321710 - 322057	2018D after TS2 run 323470 - 323983
ME+1/1A/09	$94.1\ ^{+0.4}_{-0.4}$ %	$93.6\ ^{+0.6}_{-0.7}$ %
ME+1/1B/09	$96.4\ ^{+0.3}_{-0.4}$ %	$96.6\ ^{+0.3}_{-0.3}$ %
ME+1/1A/10	$89.9\ ^{+0.9}_{-0.9}$ %	$96.3\ ^{+0.5}_{-0.5}$ %
ME+1/1B/10	$94.4\ ^{+0.4}_{-0.4}$ %	$95.8\ ^{+0.3}_{-0.3}$ %
ME+1/1A/11	$88.9\ ^{+0.8}_{-0.9}$ %	$94.3\ ^{+0.6}_{-0.6}$ %
ME+1/1B/11	$93.9\ ^{+0.4}_{-0.4}$ %	$96.6\ ^{+0.3}_{-0.3}$ %

LCT efficiency increase summary

	LCT Eff improvement
ME+1/1A/09	4.9%
ME+1/1B/09	1.3%
ME+1/1A/10	6.4%
ME+1/1B/10	1.4%
ME+1/1A/11	5.4%
ME+1/1B/11	2.7%

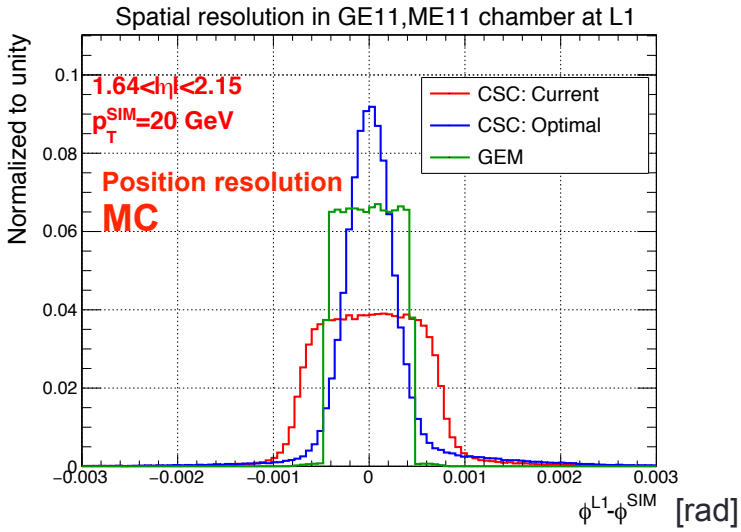
- Encouraging efficiency improvement showed by Tag&probe method
  - ➡ ~1.5% in ME1b and ~5% in ME1a
- Another analysis also showed that 2018OTMB firmware could recovered ~5% more events which are expected to be missing in current OTMB firmware. (Tao, emulation)
- 2018OTMB firmware is our new baseline for future upgrade and will be used Run3 for all OTMB

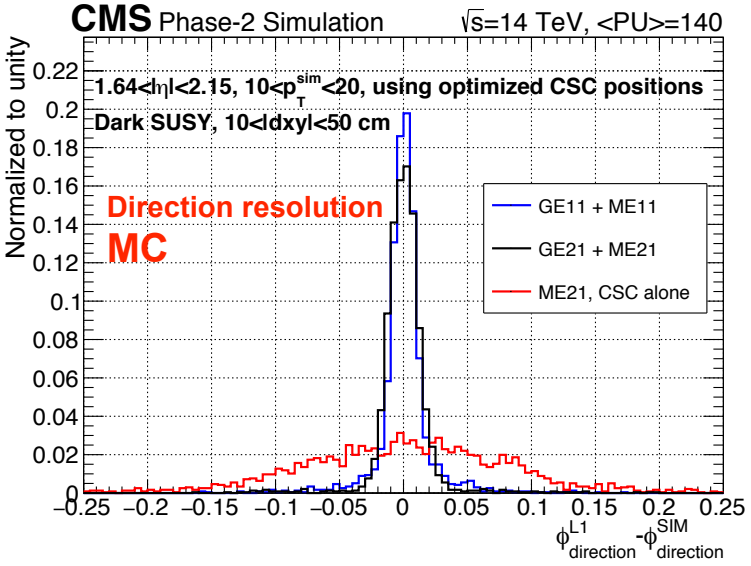
Track-Finder Level Improvement



- After 2018OTMB firmware was loaded to ME+1/1/09, 10 and11, the efficiency of LCT used by EMTF track is ~5% higher in these 3 chambers in high PU fill

CSC Position Resolution for Trigger

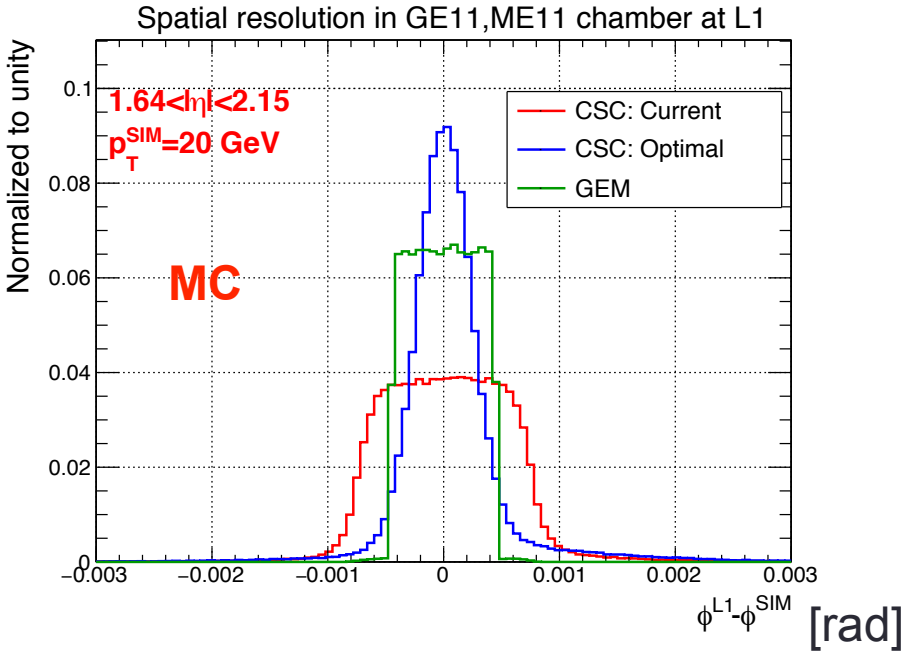


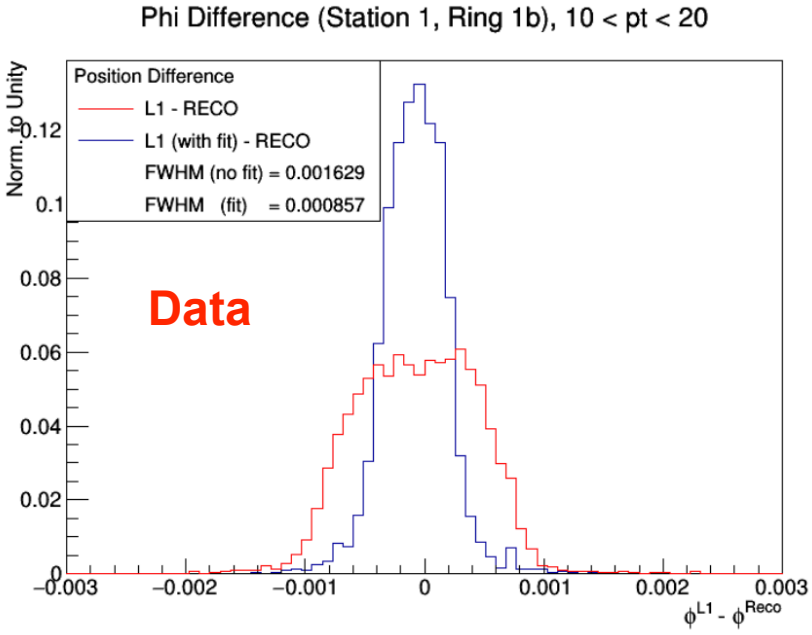


- ME11 trigger granularity: ~1.4 mrad/halfstrip
  - M11 geometry: 10 degree chamber, 128 half strips in ME1b (96 in ME1a)
- Current ME11 position resolution: ~1.5 mrad (left plot)
  - GE11 has better precision: ~1 mrad
- Local direction measurement relies on optimized CSC position resolution (right plot) in very forward region
  - Local direction measurement using CSC and GEM position benefits from comparable good position resolution
    - No materials between ME11 and GE11, almost no scattering
    - Similar for GE21-ME21
- Local direction measurements are critical in L1 trigger rate control (prompt muon trigger)
- Displaced muon trigger design in low eta region in endcap (Ring2 and Ring3) requires similar improvements in ME12, ME13 and ME22 (seen backup)
  - Ring2 and Ring 3 region, no new detector in future, but local direction is measured with CSC alone
- So could we improve CSC local measurement ? and How ? => next two slides !

Comparator Digi Fit

- Optimizing CSC precision is doable — [Malachi, fitting comparator digis]
  - Cathode local charged trigger (CLCT) is built by comparator digi in 6 CSC layers
  - Fitting comparator digis that formed CLCT could gives a better local position
  - Similar results from simulation (left) and real data (right)
- Realistic implementation in firmware is investigated by UCLA (next slide)
  - Fitting in firmware = complexity+large latency

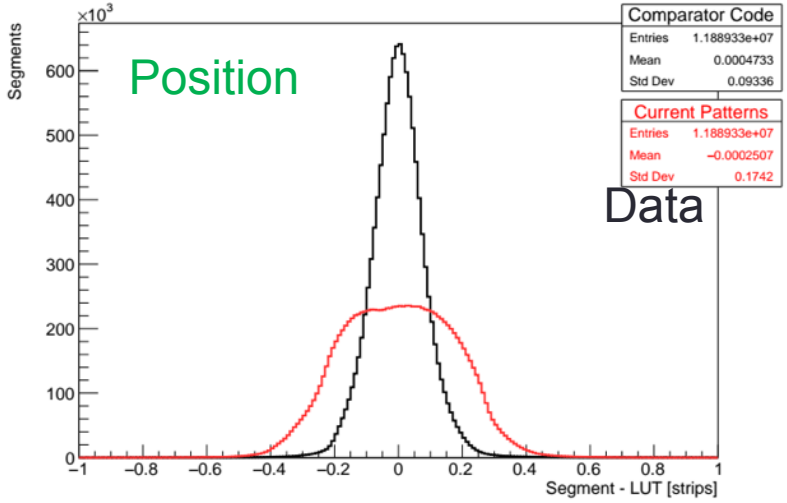




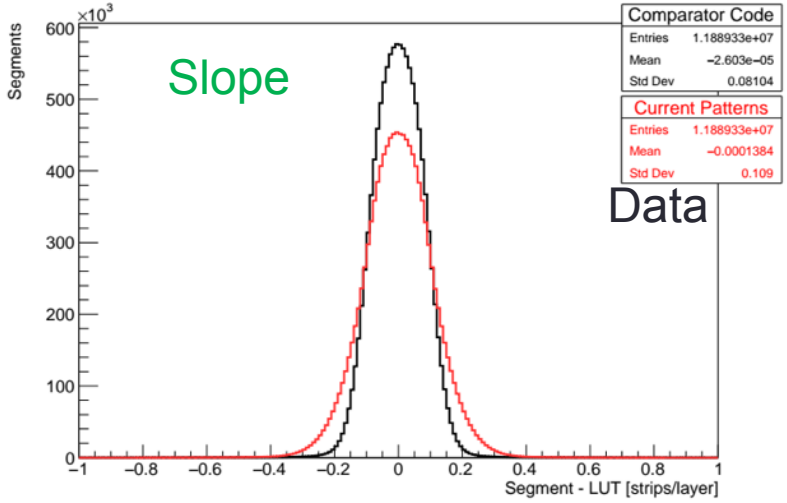
Comparator Code Look-Up Table(CCLUT)

- Current CLCT patterns have not been updated since 2007: in total 9 patterns
- News look-up tables proposed for CLCT construction: comparator code look-up table, ~4k patterns
- Current OTMB memory could adopt CCLUT without additional latency
  - ➡ Feasible for firmware implementation
  - ➡ Challenging for TMB (non-ring 1 CSCs after LS2) as FPGA on TMB is almost full now: Cool project for LS3 :)
    - We might be able to free up sizable space in TMB firmware!
- Processing real data with CCLUT already showed the improvements in position and slope (equivalent to local bending/pT measurement)
  - ➡ Position resolution is improved by ~2
  - ➡ Slope improvement is expected larger in Ring2 and Ring3 where magnetic field is stronger than Ring1
    - Slope information is used in displaced muon trigger design in low eta region in endcap (namely ME12, ME13, ME22 etc, no GEMs)
- To send out new position and slope information, the dataformat in trigger and DAQ path requires some changes. Discussed at end of the talk

Will, improvement on CLCT



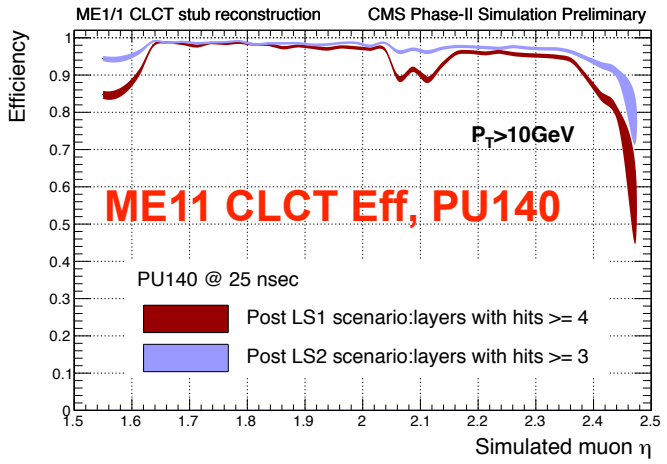
Andrew, firmware study

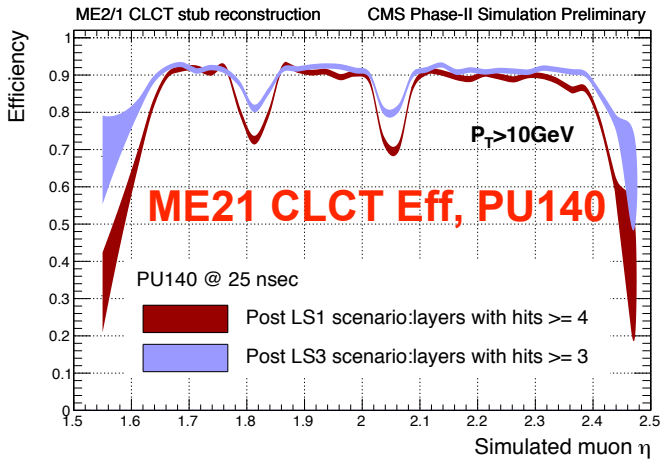


CLCT Threshold Reduction

- In Run2 setup, Cathode local charged trigger(CLCT) construction requires >= 4hits by default
- Reducing CLCT threshold from 4 to 3 could improve CLCT efficiency and finally improve LCT efficiency based on simulation
  - ME11: boundary of ME1a and M1b
  - Non-ME11: HV spacer
- CLCT threshold of ME+1/1/11 was lowered to 3 since this summer and analysis using real data showed efficiency improvement
  - With current OTMB firmware, 0.4% in ME1/1B, and 1.0% in ME1/1A
  - With new OTMB firmware, 1.2% in ME1/1B, and 2.7% in ME1/1A
  - CLCT rates increased by about 30%, matched LCT rates by about 15%
  - If we afford to rate increase, we always try to increase efficiency as much as we can

Will, 3-layer CLCT





Redefined LCT Quality Plan

- LCT quality is derived from Anode LCT (ALCT) quality, Cathode LCT(CLCT) quality, CLCT pattern
- LCT built from normal ALCT (>=4hits)+ low quality CLCT(=3hits) has low quality (=6)
  - Does EMTF use LCTs with quality below 10? **YES!**
  - Only up to two LCTs per BX per chamber are sent out and prioritizing is up to LCT quality
- In simulation, a simple modification of LCT quality definition was used to promote the quality of this type LCT
- In future we may apply similar changes in firmware level. NOT decided yet
- Another concern is from GEM+CSC integrated local trigger, seen following slides

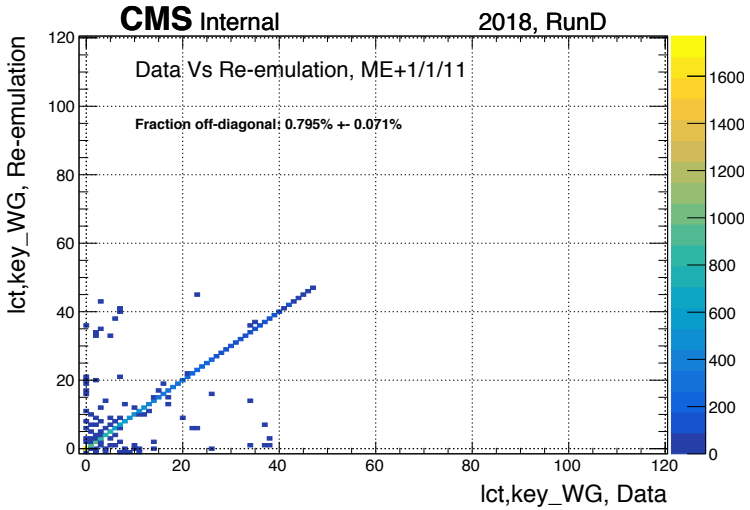
```
module lct_quality (ACC,A,C,A4,C4,P,CPAT,Q);
// Ports
  input ACC;     // ALCT accelerator muon bit
  input A;       // bit: ALCT was found
  input C;       // bit: CLCT was found
  input A4;      // bit (N_A>=4), where N_A=number of ALCT layers
  input C4;      // bit (N_C>=4), where N_C=number of CLCT layers
  input [3:0] P; // 4-bit CLCT pattern number that is presently 1 for n-layer triggers,
                 // 2-10 for current patterns, 11-15 "for future expansion".
  input  CPAT;   // bit for cathode .pattern trigger., i.e. (P>=2 && P<=10) at present
  output [3:0] Q; // 4-bit TMB quality output

// Quality-by-quality definition
  reg [3:0] Q;

  always @* begin

  if      ( !ACC && A4 && C4 && P==10 )          Q=15; // HQ muon, straight
  else if ( !ACC && A4 && C4 && (P==9 || P==8) ) Q=14; // HQ muon, slight bend
  else if ( !ACC && A4 && C4 && (P==7 || P==6) ) Q=13; // HQ muon, more
  else if ( !ACC && A4 && C4 && (P==5 || P==4) ) Q=12; // HQ muon, more
  else if ( !ACC && A4 && C4 && (P==3 || P==2) ) Q=11; // HQ muon, more
  //                                             Q=10; // reserved for HQ muons with future patterns
  //                                             Q=9;  // reserved for HQ muons with future patterns
  else if (  ACC       &&  A4       &&  C4 && CPAT ) Q=8; // HQ muon, but accel ALCT
  else if (          A && !A4       &&  C4 && CPAT ) Q=7; // HQ cathode, but marginal anode
  else if (          A &&  A4 &&  C && !C4 && CPAT ) Q=6; // HQ anode, but marginal cathode
  else if (          A && !A4 &&  C && !C4 && CPAT ) Q=5; // marginal anode and cathode
  //                                             Q=4; // reserved for LQ muons with 2D information in
the future
  else if (          A        &&  C        && P==1 ) Q=3; // any match but layer CLCT
  else if (         !A        &&  C                ) Q=2; // some CLCT, no ALCT (unmatched)
  else if (          A        && !C                ) Q=1; // some ALCT, no CLCT (unmatched)
  else                                             Q=0; // should never be assigned
  end
```

Others Ideas for Improvements

- Comparator threshold reduction to increase comparator hit efficiency
  - Comparator threshold for ME11 is 50 mV, higher than rest of CSCs (30 mV) Cameron and Siyuan Liu in 2016
  - ME11 configuration at P5 already changed the threshold into 30 mV since 2016
  - Further reduction is possible and could increase comparator hit efficiency
    - Noisy rate would also increase. to be studied
- Cathode local trigger setting: overall small effect
  - Extending comparator hit persistence to improve CLCT construction
    - Comparator hit persistence may expire before CLCT construction. Found in event displays, small effect
  - TMB-L1A matching window reduction to recover TMB data loss (~0.25%) in read out
    - TMB-L1A matching window is to initialize the TMB data readout
    - ~0.25% TMB data loss due to large TMB-L1A matching window (7BX)
  - Extend adjacent zone for (D)CFEB readout to recover hit efficiency, especially for low momentum muons
- Anode local trigger setting: similar improvement on LUT for ALCT construction, to be studied
- CSC configuration for Run3 is not finalized yet (still two years to work out!)
  - Some proposals are being tested at P5 and Let data tell us what to do next!
    - Twiki for recent changes: https://twiki.cern.ch/twiki/bin/view/CMS/CSCOTMB2018
  - Proposed changes will be further validated and tested during LS2, by b904 cosmic ray test and simulation
  - We also suggest that at beginning of 2021 run, start with current configurations, and test the proposed changes step by step and then finalize the configuration based on data analysis

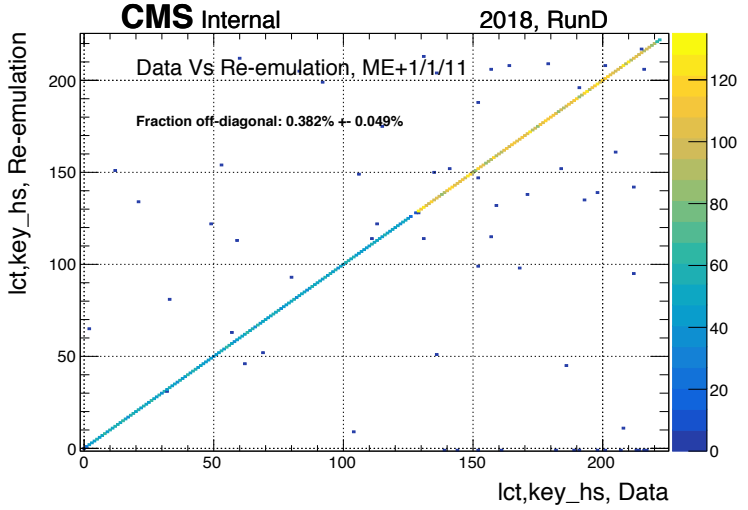
CSC Local Trigger Emulation

- Trigger emulator in CMSSW: emulating the CSC trigger primitives with wire digi and comparator digi as inputs
- Good agreement between data and emulation for 2018OTMB firmware
  - Data is taken after 2018OTMB firmware was loaded to ME+1/1/11
  - Bottom two plots are comparing the data (x-axis) and emulation (y-axis): anode wiregroup and cathode halfstrip in LCTs
  - Fraction of mismatches (off-diagonal) is <1%
  - Similar results for current OTMB algorithm (backup)



Anode location of LCT

Mismatch <1%



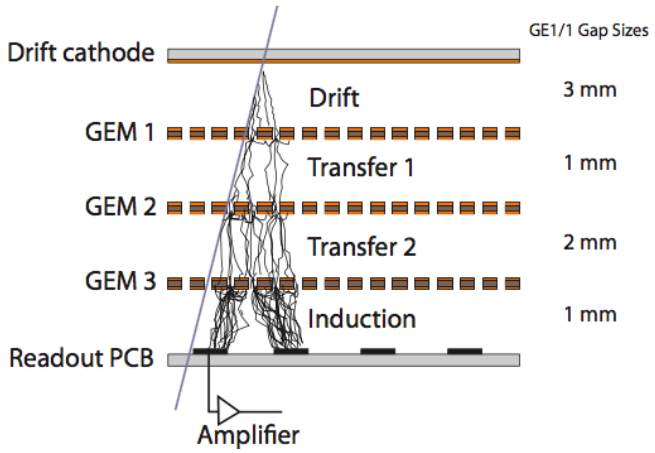
Cathode location of LCT

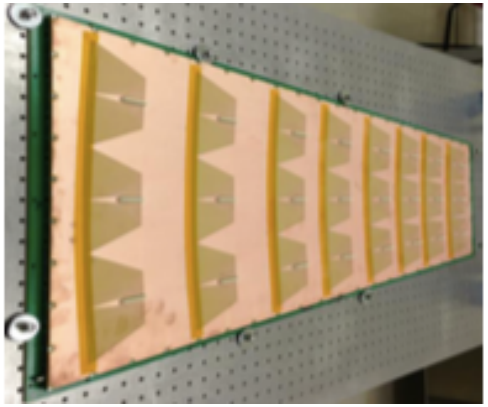
GEM Local Trigger

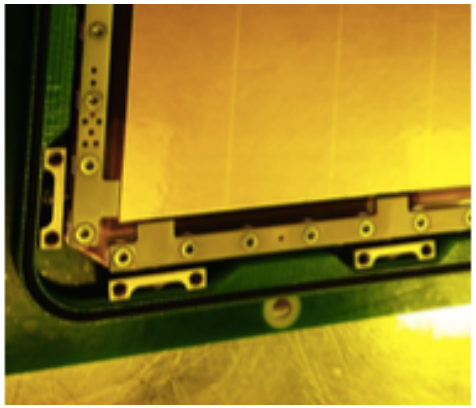
- Introduction
- Motivation of GE11 upgrade
- GE11 Electronics
- GEM trigger granularity
- GEM trigger dataformat

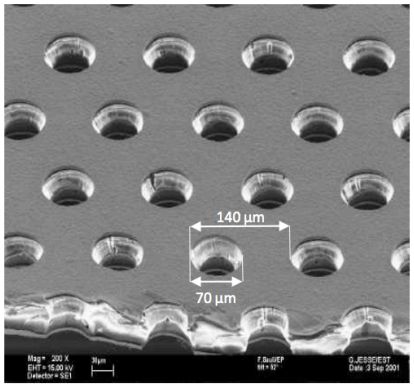
Gas Electron Multiplier (GEM)

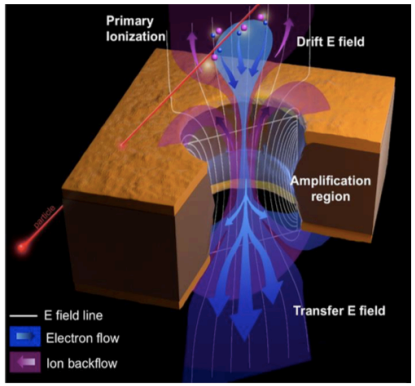
- Muon register hits on strips when passing through GEM
- Benefits of GEM technology
  - High efficiency: ~98%
  - High rate capability: 100MHz/cm^2
  - Good position and time resolution
- GE11, GE21 and ME0 all uses GEM technology





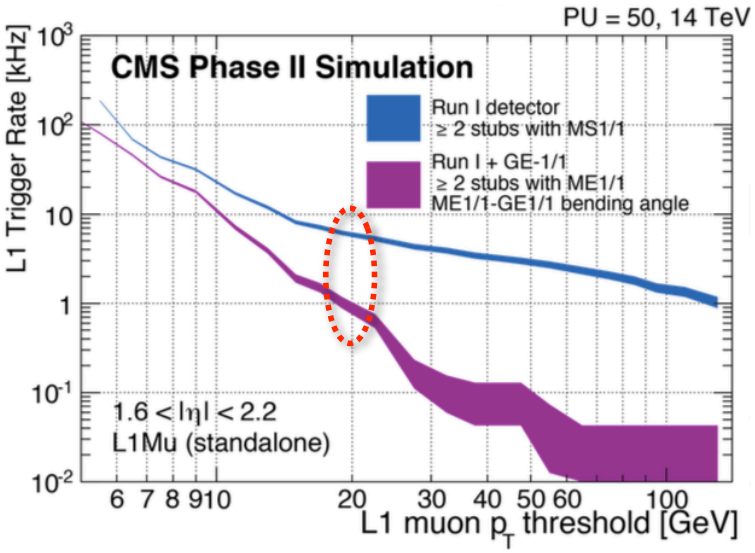


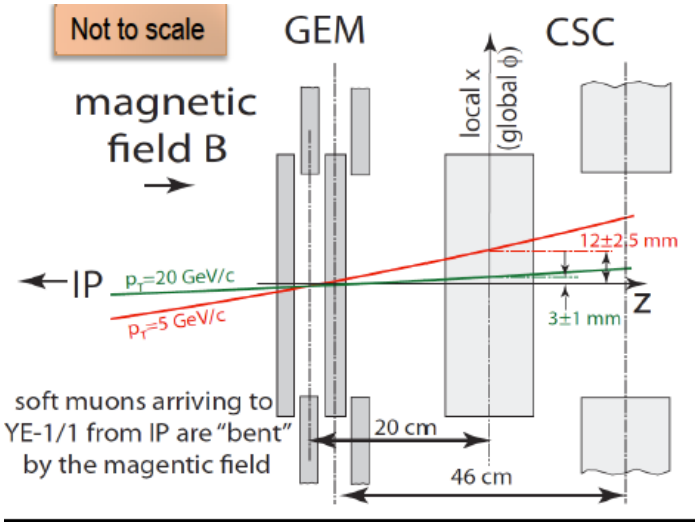




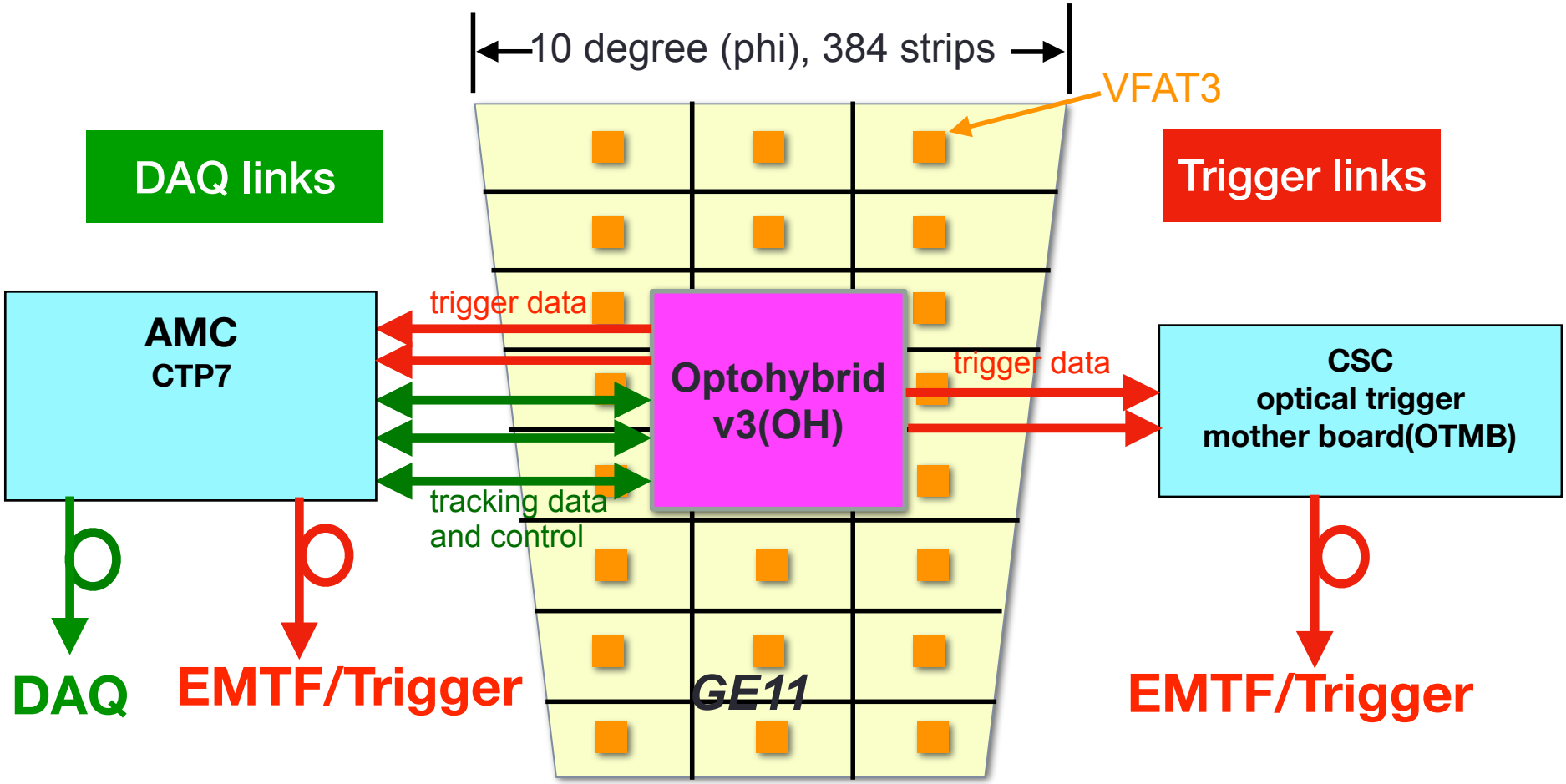
Motivations of GE11 Upgrade

- Need to maintain excellent muon trigger performance in the forward region in high luminosity LHC era
  - ➡ Very high rate of soft muons and some soft muons occasionally have stubs aligned like high pT muon
  - ➡ The bending angle between GEM and CSC is less effected by scattering as no material is between them
  - ➡ Large lever arm + magnetic field + good positions resolutions from GEM and CSC results in excellent discriminating power against soft muons from GEM-CSC bending angle



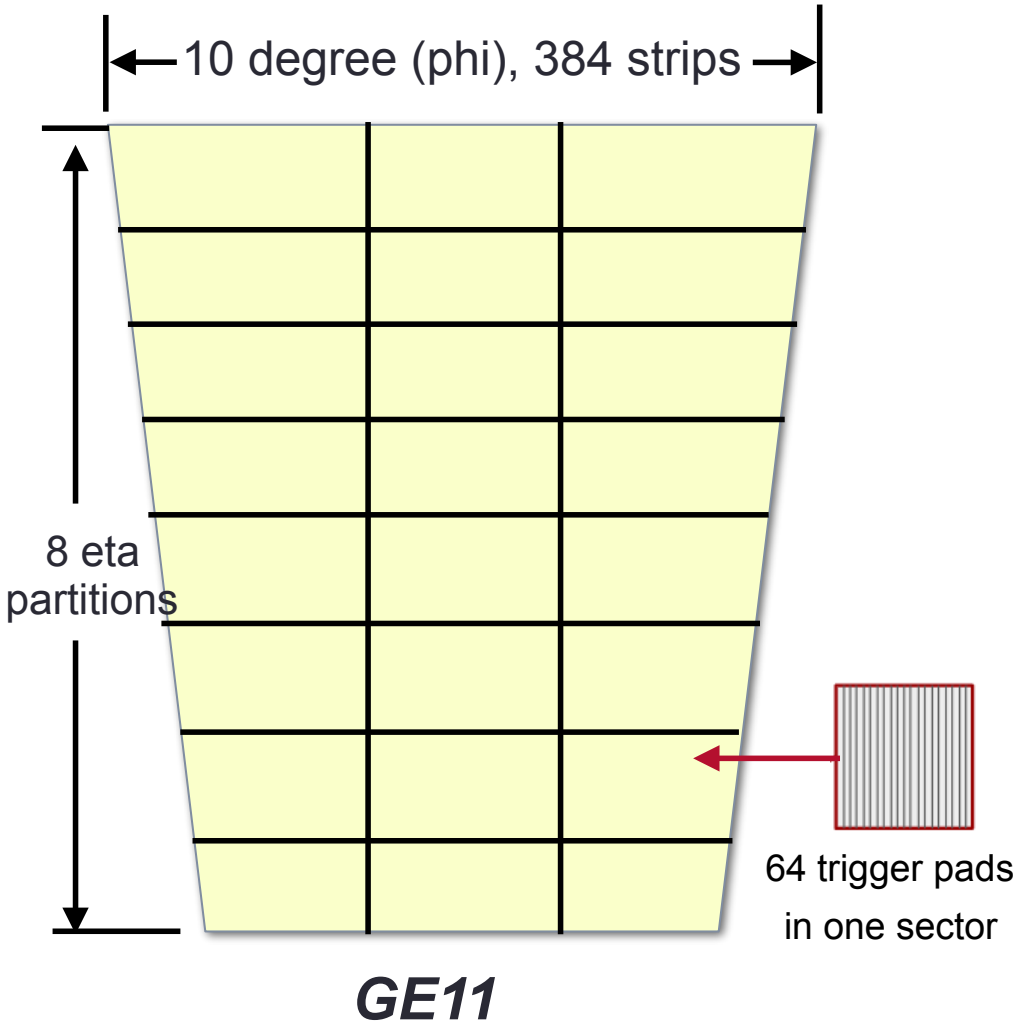


GE11 Electronics



- OptoHybrid board: concentrate 24 VFATs data and send out for triggering and DAQ
- GE11 electronics design is finalized
  - ➡ 24 VFATS and 2 OHs per chamber. 12 CTP7s in total
- Identical GEM trigger data is sent to CSC OTMB and EMTF

GEM Trigger Granularity



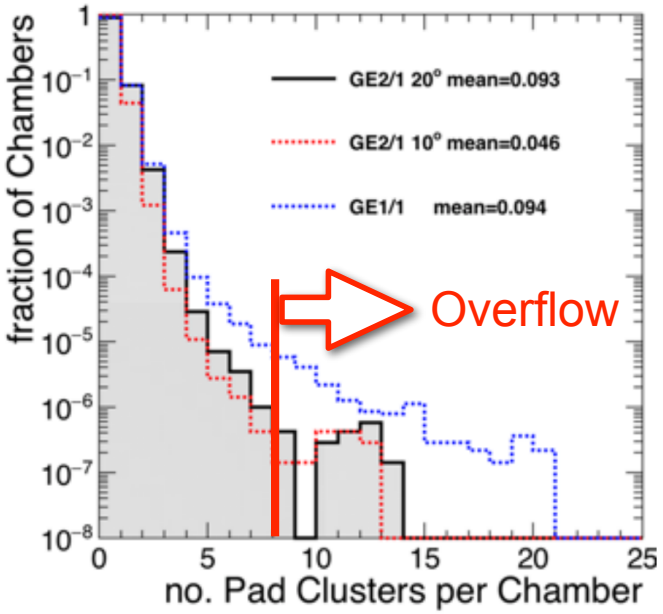
- Both GE11 and GE21 detector types have same trigger granularity
  - One trigger pad = 2 strips
  - Phi granularity = 0.9mrad/pad
  - 8 eta partitions
- Eta coverage
  - GE11: 1.5(1.6)-2.18 for short (long)
  - GE21: 1.65-2.4
- GEM layers
  - GE11 = 2 layers of GEM
  - GE21 = 2 layers of GEM
- GEM cluster finder
  - On-chamber electronic finds up to 8 clusters in the whole chamber
  - Cluster size is up to 8 pads
  - Latency ~3BX

GEM Trigger Data Format

- Each chambers sends up to 8 clusters (local position+size) per BX
  - Trigger data also includes frame marker, special marker for BC0, cluster overflow flag
- Overflow rate = 1.18E-05 @ PU140
  - To be reevaluated by new simulation with better background model
- Identical trigger data is sent to CSC OTMB and EMTF(through CTP7)
  - EMTF have enough spare links to receive GEM trigger data from CTP7s
  - Latency of GEM trigger data transmission to EMTF: comparable to CSC

GEM trigger cluster dataformat

	N bits
Phi sector	2
Eta partition	3
Pad number	6
Cluster size	3
Total	14

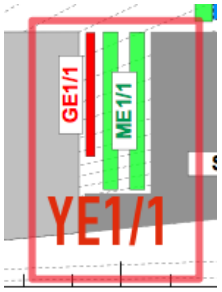


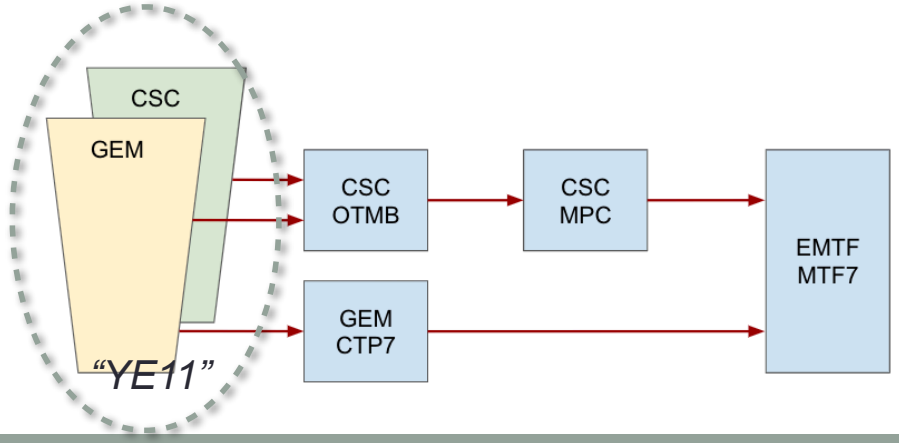
GE11+ME11 Local Trigger

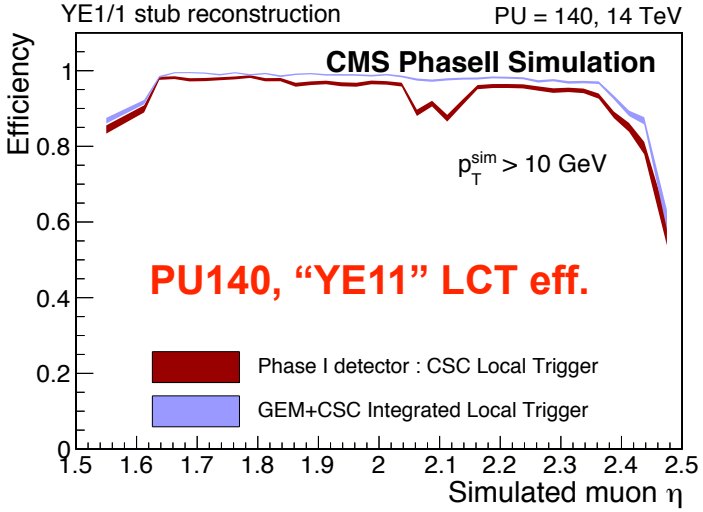
- GE11+ME11 local trigger
- Performance at track finder level
- GEM+CSC local trigger: simulation , firmware and data format

GE11+ME11 Integrated Local Trigger

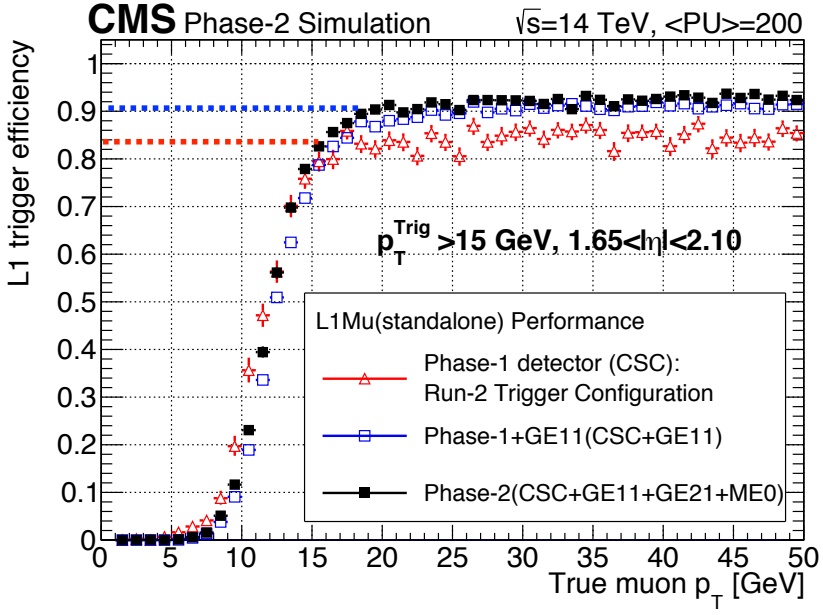
- CSC-only local trigger algorithm
  - Anode trigger (ALCT): coincidence of wire hits, >=4 out of 6 layer
  - Cathode trigger(CLCT): coincidence of comparator hits, >=4 out of 6 layer
  - Correlated trigger (LCT): ALCT-CLCT match in timing
- GE11 installation makes GEM+CSC algorithm possible in “YE1”1 region(=GE11+ME11)
  - GE11 only covers up to eta~2.1 while ME11 covers up to eta~2.4
- GEM+CSC trigger algorithm: coincidence of anode trigger, cathode trigger, GEM trigger
  - Anode trigger: unchanged, already very efficient
  - Cathode trigger: >=3 out of 6 layer coincidence of comparator hits
  - GEM trigger: GEM hits
  - Correlated trigger: all combinations we studied
    - ALCT+CLCT(>=4 hits), ALCT+CLCT+GEM, ALCT+CLCT+2GEM, ALCT+2GEM, ALCT+low quality CLCT(3layer hits, ME1a region only)
  - GEM trigger Matching is based on timing and position
- Local trigger efficiency is improved by GEM+CSC algorithm

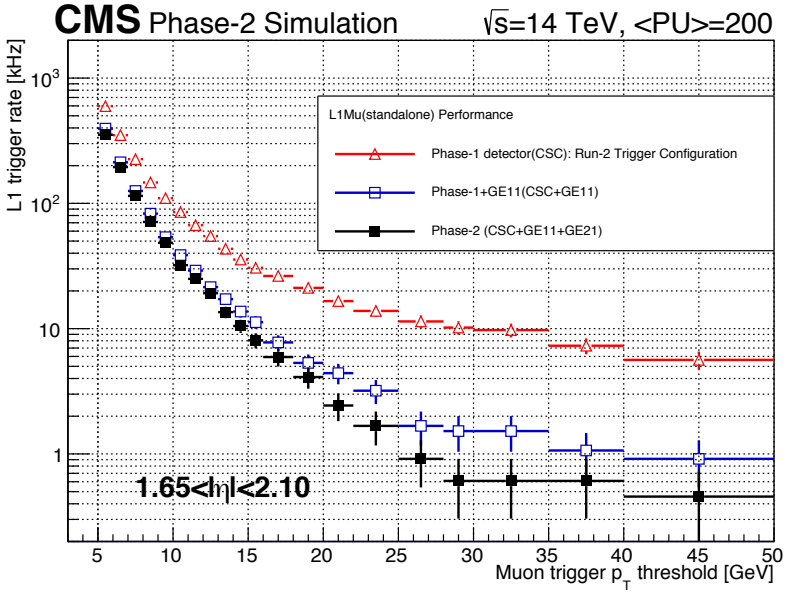






Performance at Track-Finder Level





- Improvement in local trigger could be propagated to track-finder level and could increase L1 muon trigger efficiency
  - Phase-1 detector: CSC-only
  - Phase-2 detector: CSC+GE11+GE21(+ME0). GEM+CSC algorithm is ON by default
- Meanwhile GEM installation also helps control L1 muon trigger rate by GEM-CSC bending angle cut
- Overall track-finder has a better performance with trigger primitives from GEM+CSC algorithm

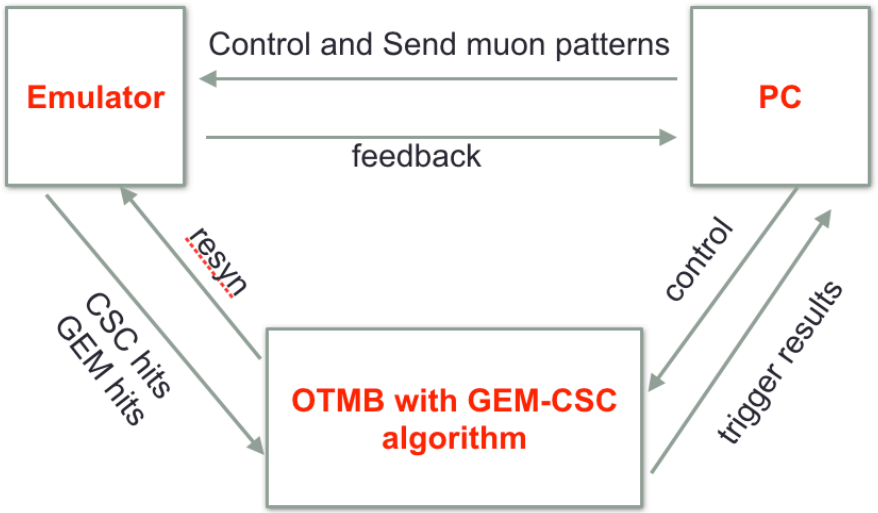
GEM+CSC Local Trigger: Simulation

- GE11 and GE21 both use realistic GEM digitizer to simulate GEM digis
- GEM+CSC algorithm for GE11-ME11 and GE21-ME21 was implemented in emulator in CMSSW back to 2014
  - LUTs to map GEM trigger and CSC trigger were generated by extrapolations and would be also used in firmware
  - Coincidence pad is built by matching GEM hits on two layers before running GEM+CSC algorithm
  - ALCT and CLCT construction part is unchanged
  - Matching between GEM trigger and CSC trigger requires both position and timing coincidence, and LCT quality is effected by matching
  - Up to two LCTs per BX per chamber are sent out and selection on LCT candidates is based on quality and GEM-CSC bending angle
    - No extra bandwidth for output transmission
- Future changes:
  - New LUTs for CLCT constructions for all CSCs
  - Modification due to real firmware implementation

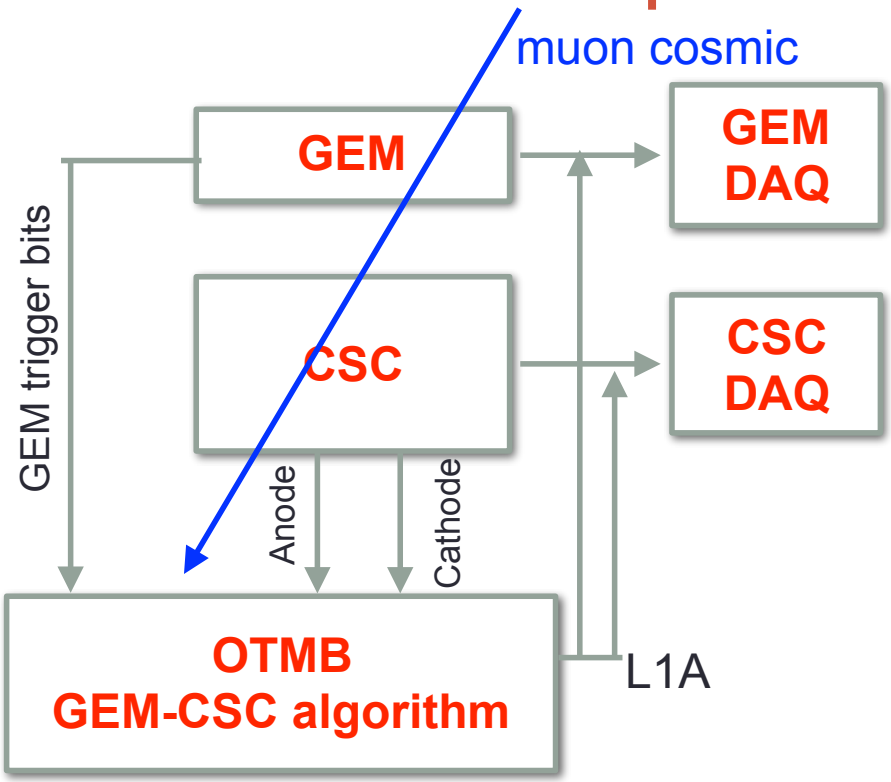
GEM+CSC Local Trigger: Firmware

- GE11 has two trigger fibers which connects to spare inputs on CSC OTMB
- OTMB firmware with GEM+CSC algorithm will be built on top of 2018OTMB
- CSC OTMB firmware has been demonstrated to receive and buffer GEM trigger data. work done by UCLA
  - ➡ Basic GEM-CSC trigger communication has been proven to performance as required OTMB to implement future combined GEM+CSC trigger primitives
  - ➡ Took combine runs at b904 in 2016 and read out GEM+CSC trigger data through the OTMB
- The firmware development is a joint effort of UCLA+TAMU and the schedule is controlled by managers
  - ➡ Probably first demon will be built roughly on July 2020 (very informally)

Teststand For GEM+CSC Firmware Development



Teststand using emulator board in lab



Teststand in future at b904

- Left: teststand setup using emulator board, at TAMU and UCLA
  - Emulator board emulates GEM and CSC trigger data based on muon patterns from PC
  - Test procedure: send muon patterns from PC and then receive trigger results after short latency, compare triggers results with muon patterns
- Right: teststand with muon cosmic, to be set up at b904

GEM+CSC Local Trigger: Trigger Bits

- GEM-CSC bending angle will be recalculated at track finder level
- To send out LCT with better position resolution, 1/4 strip rather than 1/2 strip, and better bending resolution(slope), More space is needed!!
  - Better position resolution is also expected in displaced muon trigger study
- LCT quality is effected by GEM trigger matching in GEM+CSC algorithm
- ME11 OTMB with GEM+CSC algorithm keeps 32 bits data format
- Redundant bits can be reallocated to additional position and slope information
  - current lct_quality and clct_pat is partially overlapped
  - LCT quality might be redefined and CLCT pattern might be replaced by local bending(CSC-only)
  - clct_bend is already covered by clct_pat
  - EMTF will be notified once proposal is fixed
- In DAQ path, the data format also will be changed but the bandwidth stays the same
  - Changes in packer and unpacker in cmssw
- New idea: add one more transmitter in new OTMB for ME21, 31, 41 to send out more trigger data. Not seriously discussed before
  - Report more LCTs when multiples muons hit one chamber

current data format of trigger primitives CSC-only algorithm

Table 4: LCT data fields and size.

Data Field	Size (bits)	Description
alct_key	7	ALCT key layer wiregroup
clct_pat	4	CLCT bend pattern
lct_quality	4	LCT quality
lct_vpf	1	LCT valid pattern flag
clct_cfeb	3	CLCT (D)CFEB
clct_key	5	CLCT key layer half-strip
clct_bend	1	Direction of CLCT bend
clct_sync_err & tmb_sync_err_en	1	Combined sync. err. flag
alct_bxn[0]	1	ALCT BX flag
clct_bx0	1	CLCT BX flag
csc_id	4	Trigger ID of a chamber

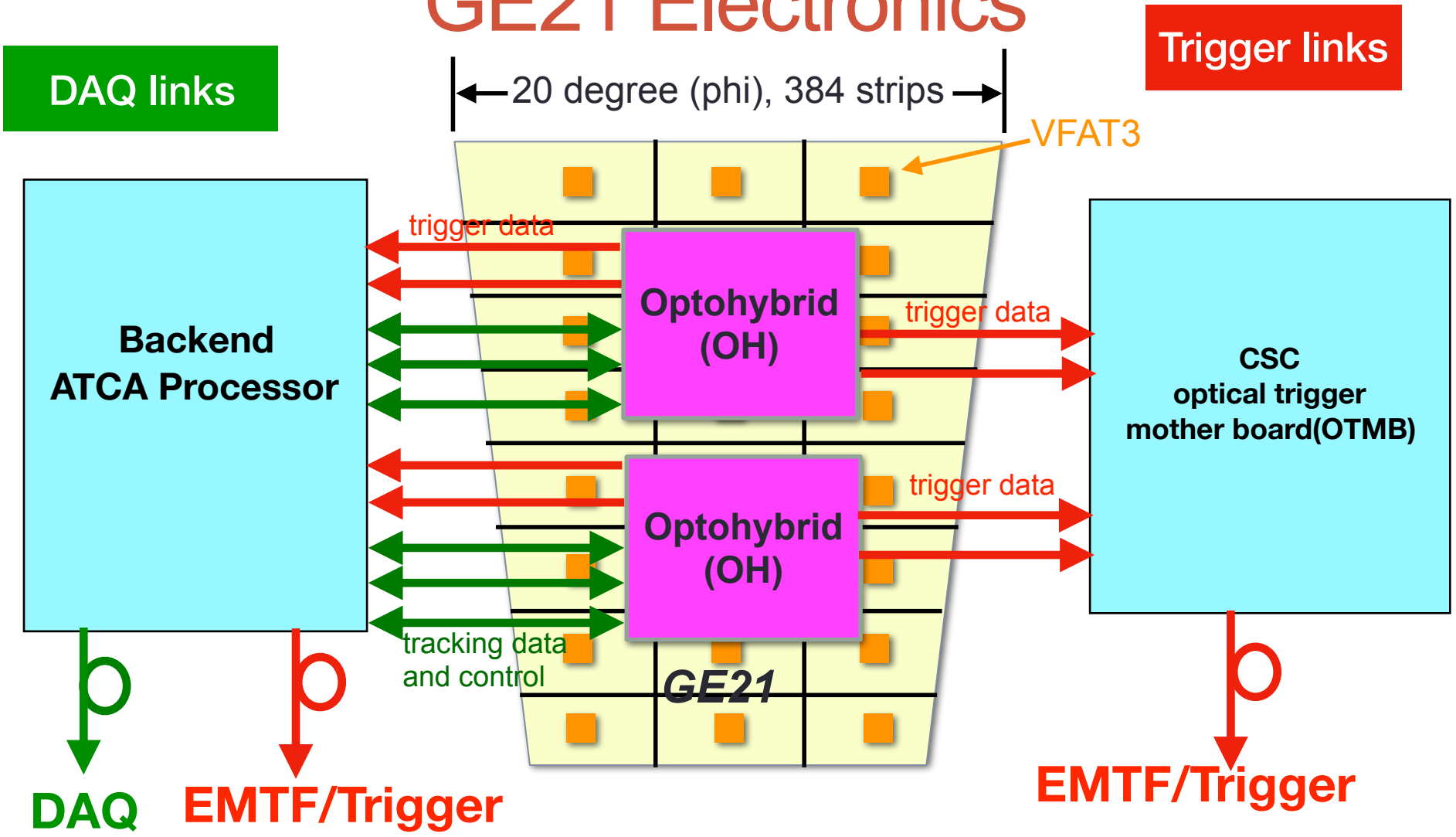
Phase-2 Upgrade

- Overview
- GE21 electronics
- GE21+ME21 local trigger
- Performance at track finder level

Phase-2 Upgrade Overview

- During LS3, ME0 and GE21 will be installed
- ME0, similar to standalone CSC, sends the CSC-like local trigger primitives to EMTF
- GE21+ME21, similar to GE11+ME11, uses GEM+CSC algorithm to build integrated local trigger and sends trigger primitives to EMTF
  - ➡ Could help improve efficiency and control trigger rate
- GE11+ME11, GE21+ME21 and ME0 make the directional measurements possible, which together allows pT assignment without beamspot constrain
  - ➡ Critical for highly displaced muon trigger (see the talk from Alexei)

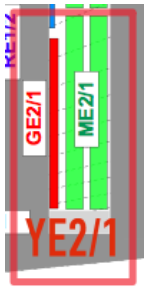
GE21 Electronics

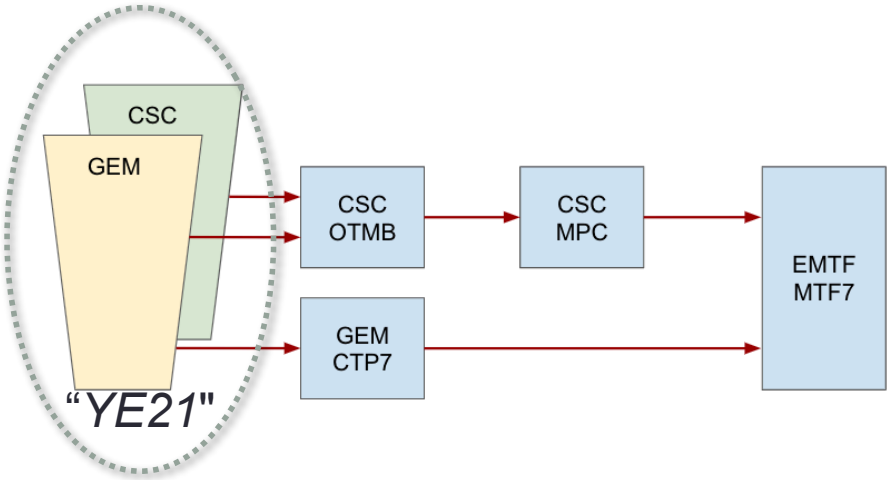


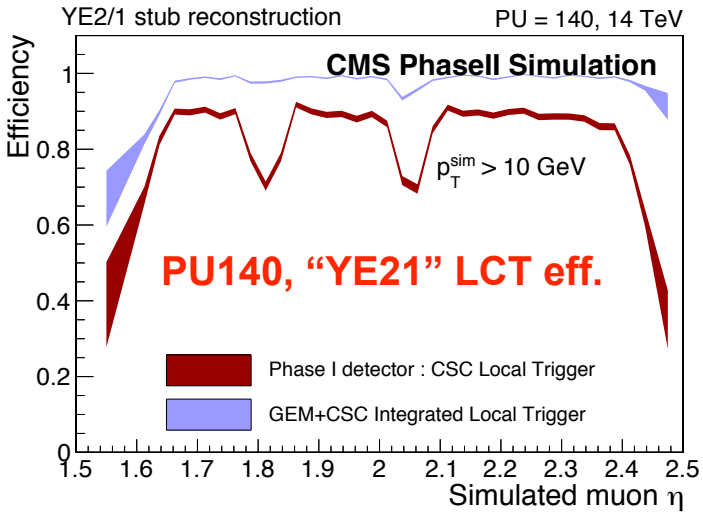
- 48VFATs and 4 optohybrid per chamber
  - ➡ GE21 electronics designed is not finalized yet
- ME21 uses TMB now but during LS2, all ring 1 CSCs will be commissioned with OTMB

GE21+ME21 Integrated Local Trigger

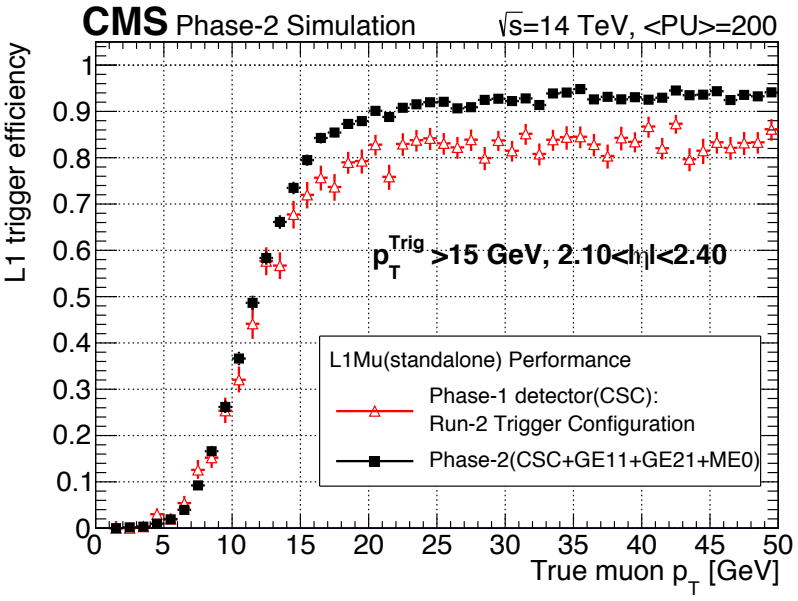
- GE21+ME21 local trigger: coincidence of anode trigger, cathode trigger, GEM trigger
  - Anode trigger: >=3 out of 6 layer coincidence of wire hits, to reduce inefficiency due to HV spacer
  - Cathode trigger: >=3 out of 6 layer coincidence of comparator hits
  - GEM trigger: GEM hits
  - Correlated trigger: combination we studied
    - ALCT+CLCT(both >=4layer hits), ALCT+CLCT+GEM, ALCT+CLCT+2GEM, CLCT+2GEM
  - GEM trigger and CSC trigger matching is based on timing and position
- Local trigger efficiency in "YE21"(GE21+ME21) could be improved by ~10% in PU140

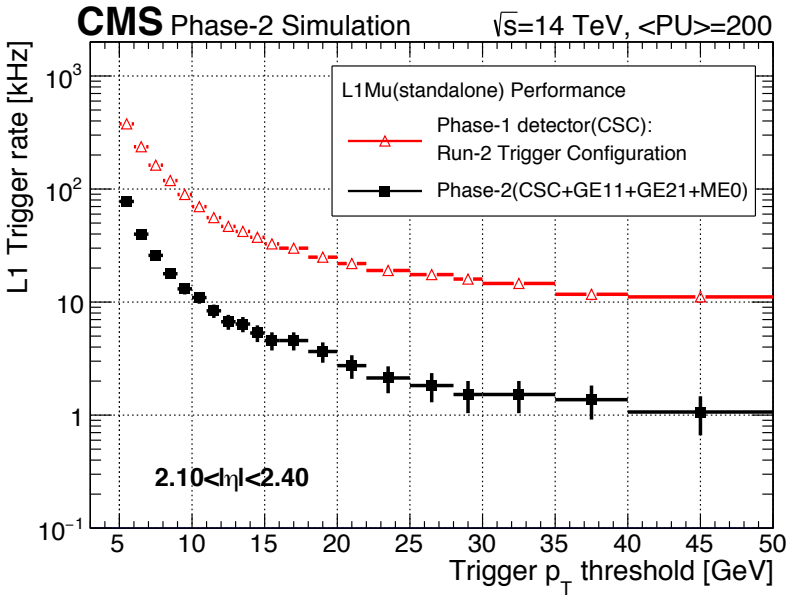






Performance at Track-Finder level: Eta2.1-2.4





- With GE21 and ME0 installation, standalone muon trigger performance is greatly improved in high PU
  - ➡ Simulation switched on GE21+ME21 algorithm in phase-2 configuration
  - ➡ ME0 stub is required in phase-2 configuration by default

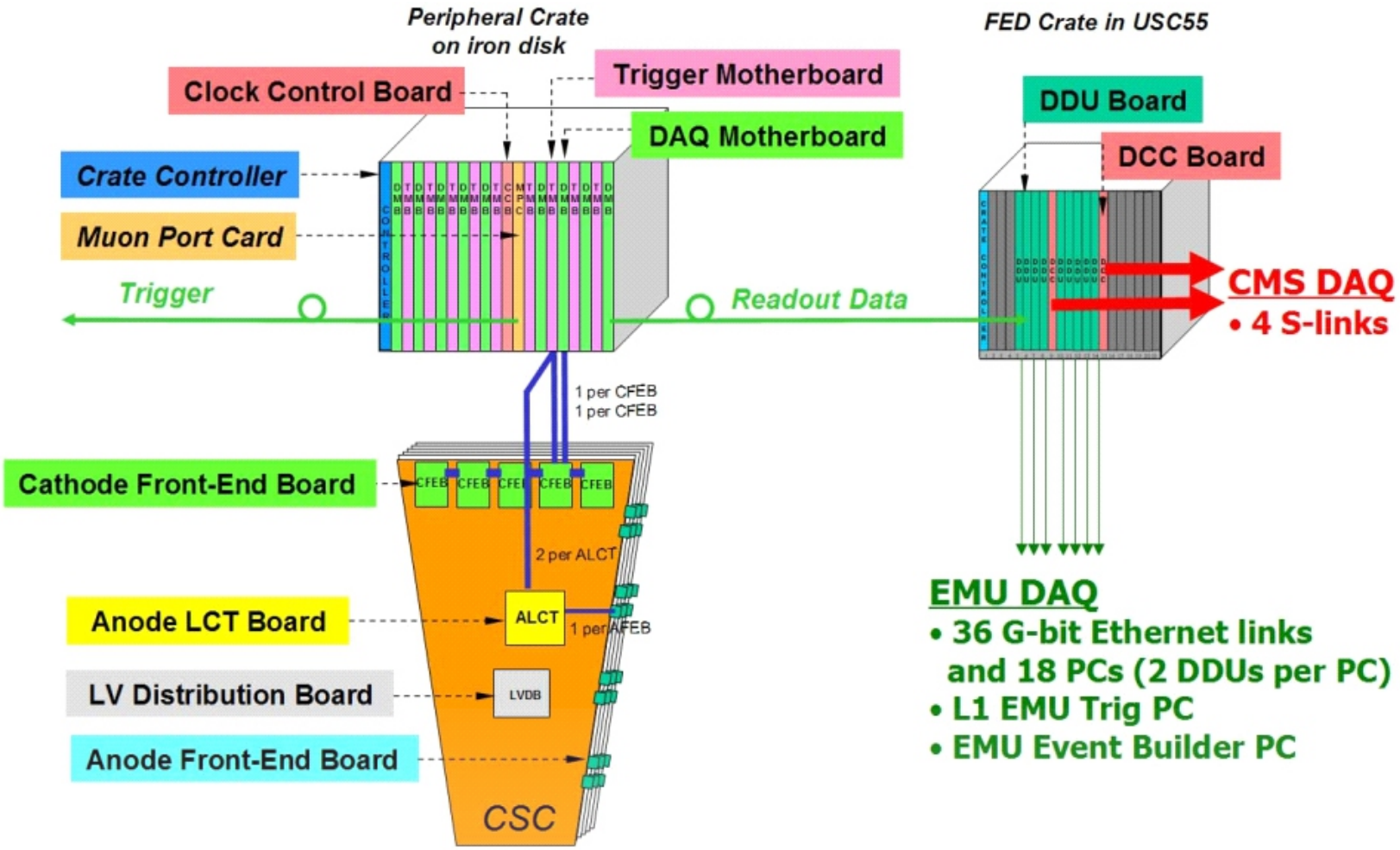
Summary

- In Run2, CSC trigger primitive is very efficient: ME1b: ~95%, ME1a: 90%, non-ME11 ~98%
- 2018OTMB firmware showed encouraging improvement and will work as our new baseline for future upgrade in forward region
  - ➡ After LS2, OTMB will be commissioned for all ring 1 CSC and rest of CSC will still use TMB
  - ➡ Some key new features in 2018OTMB algorithm might be also ported to TMB firmware
- Improving CSC position measurement with new LUTs is important for local directional measurements and is also very challenging
  - ➡ Requires extra bits to send out better position and slope(~local bending/pT)
  - ➡ FPGA in TMB is almost full but it will be a project in LS3 (more years to dig out solution)
- GE11 electronics design is finalized and local trigger is well defined
- GEM+CSC integrated local trigger was fully simulated and added in CMSSW back to 2014
- Firmware development of GEM+CSC algorithm is planned during LS2 and will be finished before Run3
  - ➡ The trigger bits sent to EMTF will remain 32 bits but will be re-interpreted
- Final CSC configuration for Run3 is not finalized yet (still 2 years away from Run3)
  - ➡ Some tests are being done at P5 and data could give important indications
- Phase-2 upgrade including GE21 and ME0 could maintain a good standalone muon trigger in forward region in high luminosity regime
  - ➡ Phase-2 upgrade also makes displaced muon trigger possible in forward region

Lots discussions and help from CSC group and GEM group, Thanks!

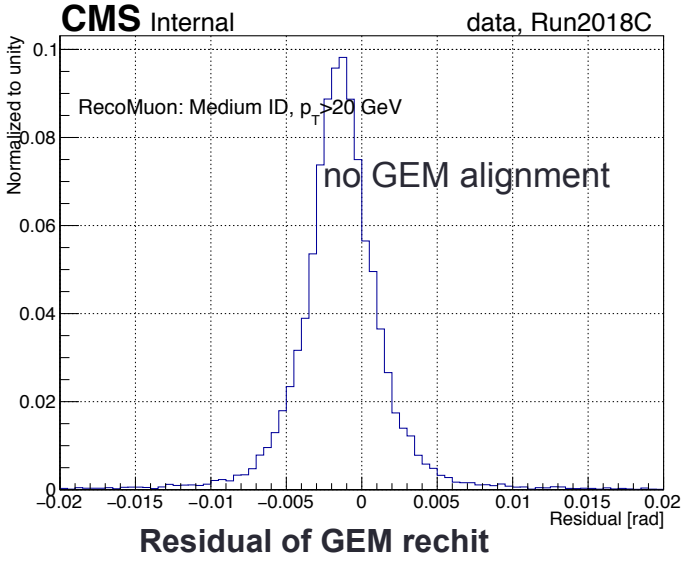
Backup

CSC Electronics Overview: Non-ME11

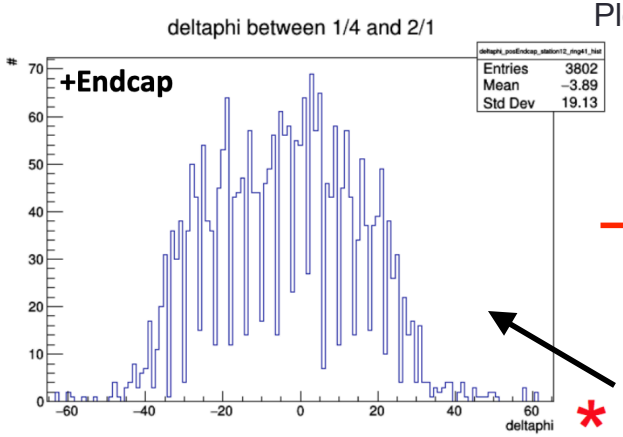


GEM-CSC Bending Angle and Alignment

- Residual of GEM rechit is quite large! Will kill GEM-CSC bending angle calculation!
  - Halfwidth is ~5mrad and distribution is asymmetric
  - GEM has good position resolution (strip pidtch ~0.5 mrad)
- Some misalignment patterns are found with GEM
  - Shift in local X, even from left plot!
  - Rotation along local Z
  - Other minor issues
- EMTF experience with CSC alignment: LUTs with alignment correction give better results in pT assignment
  - Very impressive considering the multiple scattering
- Lesson learned: LUTs of mapping GEM trigger and CSC trigger should be derived from geometry with alignment correction
  - No materials between GEM and CSC

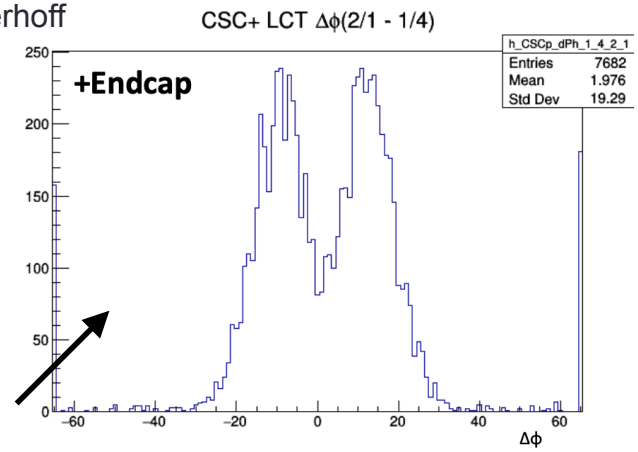


Plots form Kun Shi and Andrew Brinkerhoff

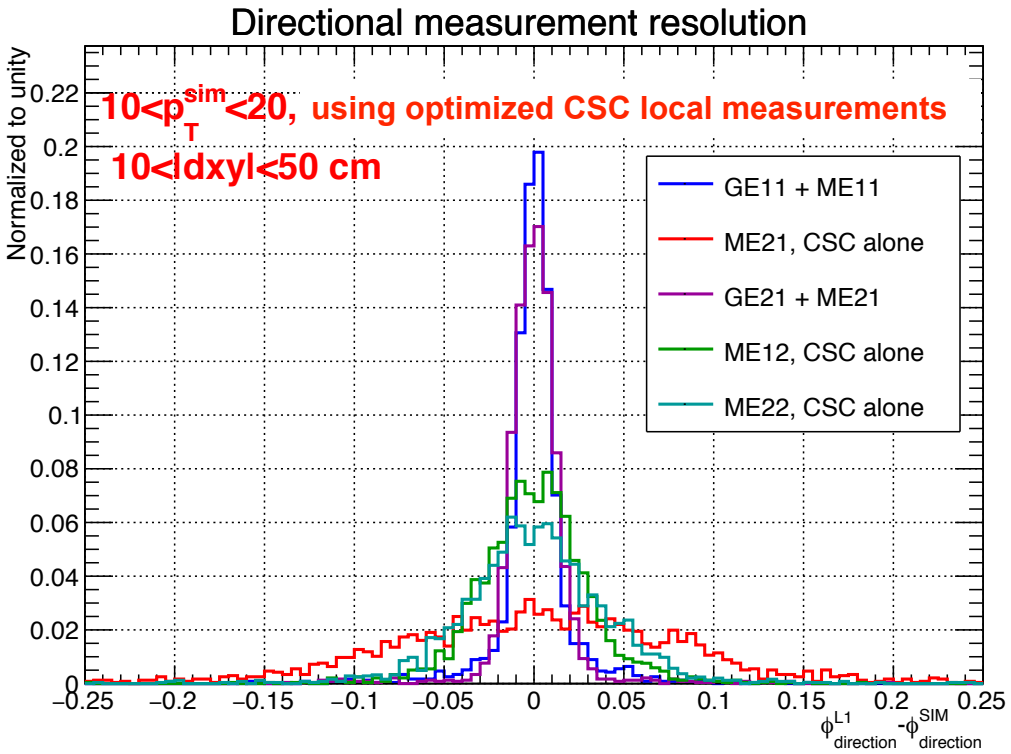


alignment correction

delta phi between station 1 and station 2 in EMTF
double peak due to +/- charge
Chad. EMTF

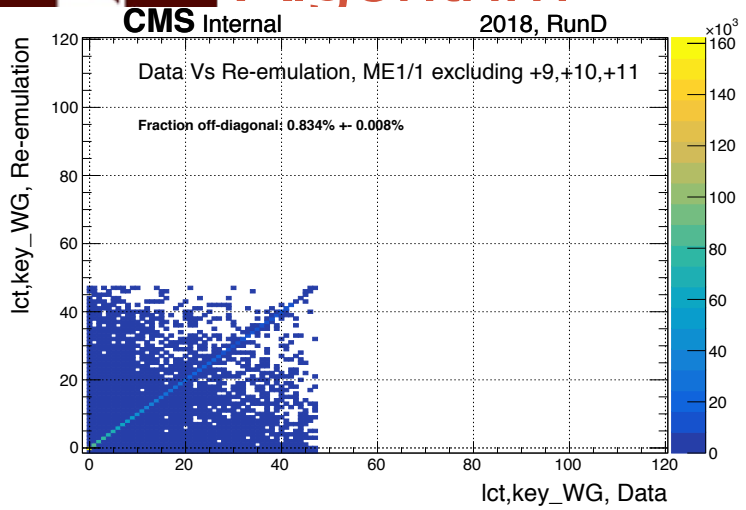


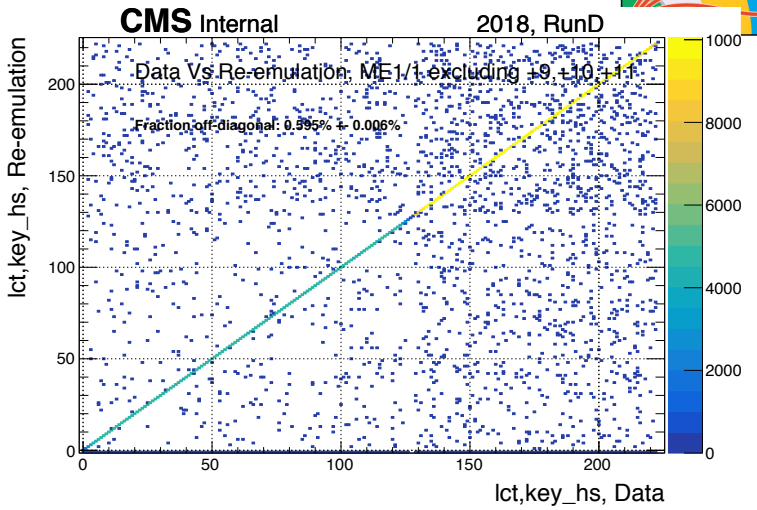
Local Direction Measurements with GEM and CSC



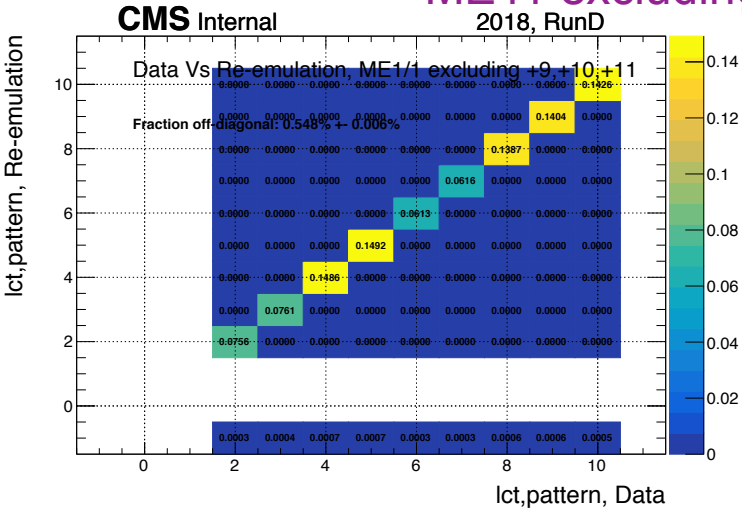
- In low eta region (eta1.2-1.6), ME12 alone and ME22 alone could form two good local direction measurements and together make displaced muon trigger possible
- In high eta region (eta 1.6-2.1), GE11-ME11 and GE21-ME21 also forms two good local direction measurements for displaced muon trigger design

Data vs Emulation: LCT for Current Algorithm

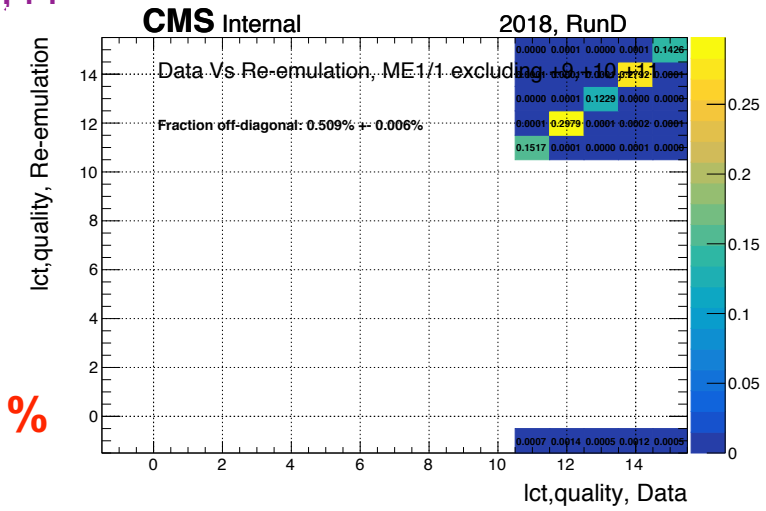




Run 323524, Single muon, 2018 Sep. 25th
ME11 excluding ME+1/1/09,10,11



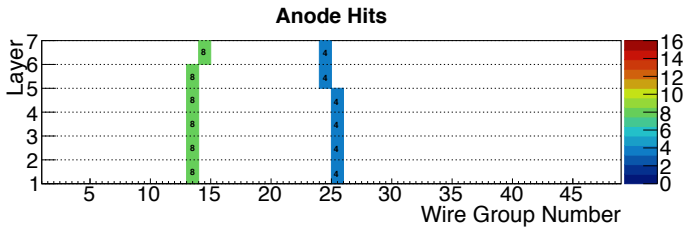
Mismatch <1%

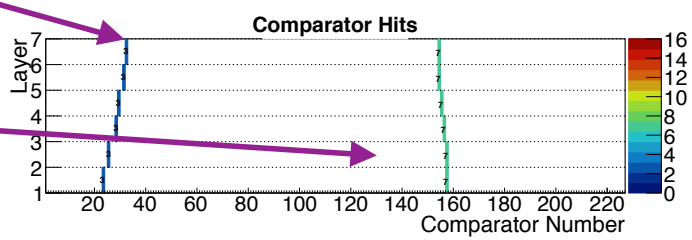


Event Display From Collision Data: Again!

muon1 arrives at BX4,
not in time with L1A, not read out by DAQ

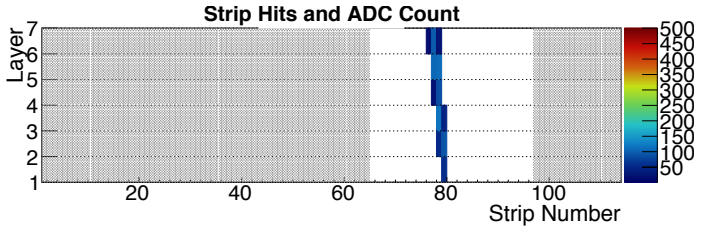
muon2 arrives at BX7,
in time with L1A





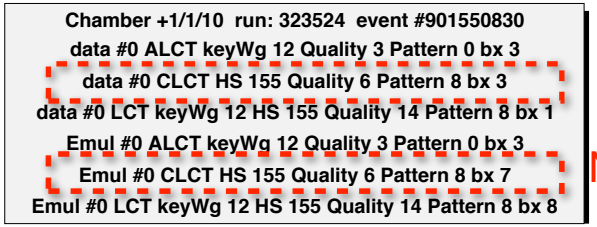
note: comparator digi is read out in 12 BX

current lgorithm fails to trigger on muon2 because of dead time caused by muon1 from a preceding collision



note: DCFEB readout is triggered by pretrigger

New algorithm with localized dead time zone is able to locally trigger on muon1 and muon2 and muon2 is read out by DAQ!



New algo

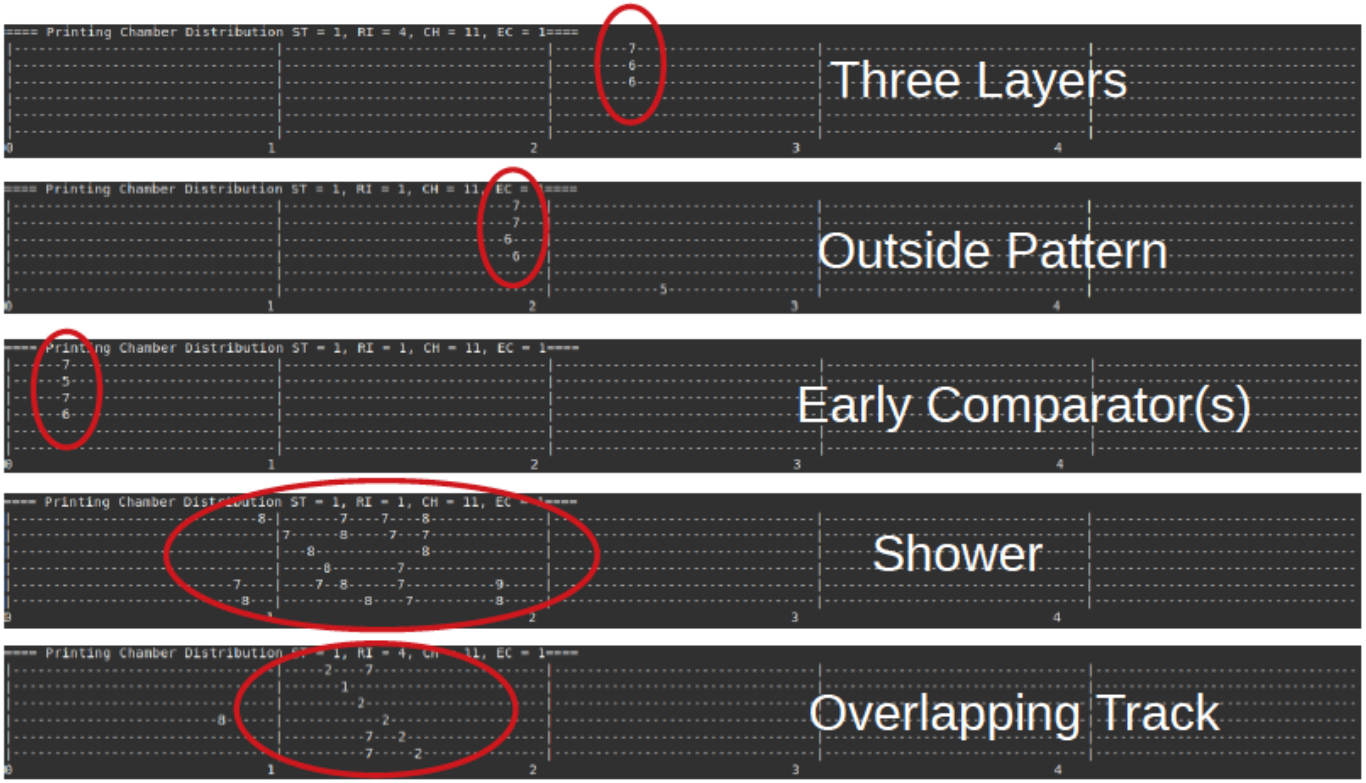
- Events that current algorithm failed to trigger on: ~5% (<PU>~40)
  - ➡ No preselection on events unpacked from RAW data
- New algorithm saves strip digis of muons matched with L1A while current algorithm would totally miss the muons in triggering and DAQ
  - ➡ New OTMB firmware also increase CSC segment efficiency

note: CLCT and LCT only at the one bx matched with L1A are read out

3-layers CLCTs in ME11

CLCT Results (cont)

- CLCTs categorized into five types after scanning events



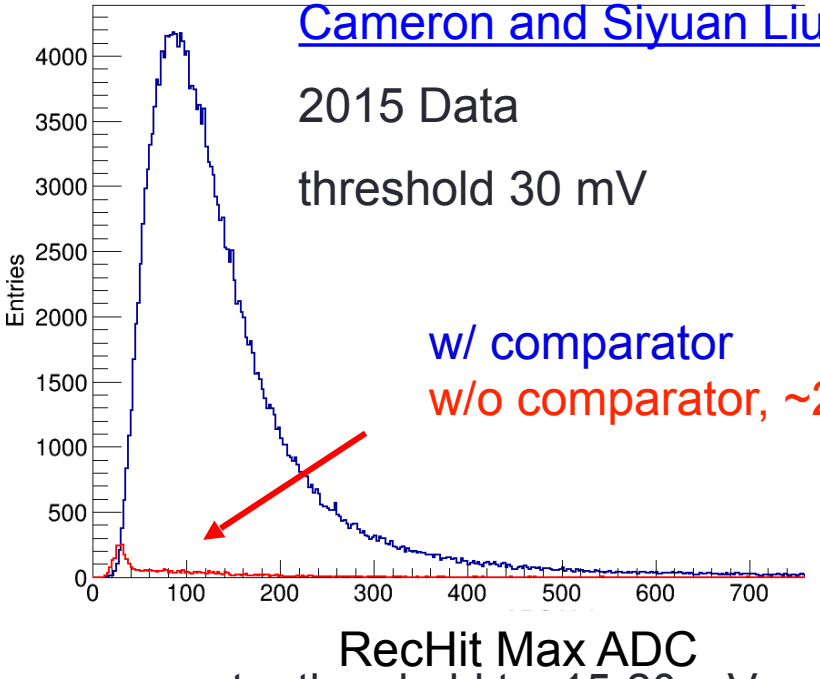
ME1/1A (/108)	ME1/1B (/130)
46%	45%
15%	19%
21%	14%
11%	16%
7%	6%

eventdisplays showed how CLCT threshold=3 recovered muons

Comparator Threshold Reduction

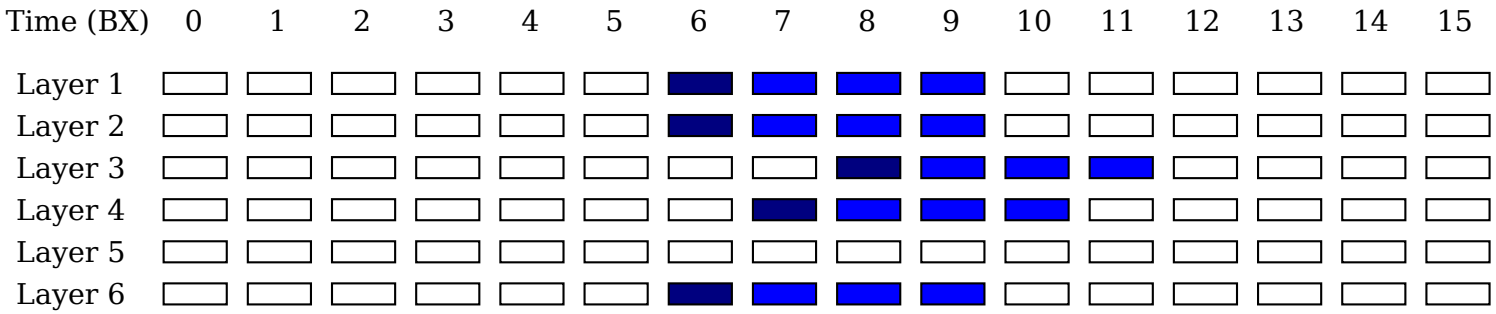
- ME1/1 comparator thresholds were 50 mV, higher than other CSC chambers
- Lower comparator threshold could improve comparator hit efficiency
- August 1, 2016, ME11 comparator thresholds were lowered to 30 mV, like rest of the CSC

with current comparator threshold 30 mV, fraction of rechit without comparator hit is ~2%



- Tests at b904 showed that further reducing comparator threshold to 15-20 mV could achieve comparator hits efficiency close to rechit efficiency
  - ➡ Noise control to be tested by real detector at P5

Extending Comparator Hit Persistence

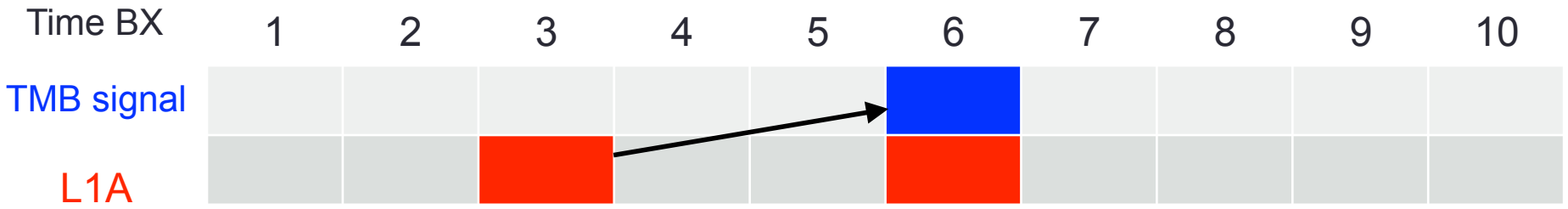


CLCT hit persist: extension of hit over time

e.g. one halfstrip on layer1 has hit on BX6 and then the hit is extended to persist on BX7,8,9

- In Run-2 setup, the comparator hits persistence is 4BX in total by default
- CLCT is constructed by finding the coincidences of comparator hits in all 6 layers in every BX
- Some event displays from real data showed that extending comparator hit persistence from 4BX to 5BX could benefit CLCT construction
- At P5, the change of increasing comparator hit persistence to 5 was applied to some CSC chambers on Nov. 13th 2018 and analysis will come in future

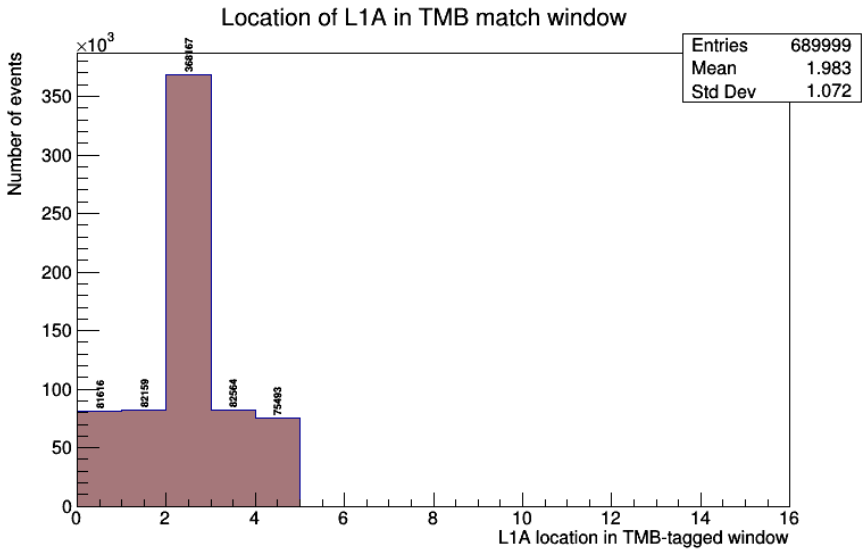
TMB-L1A Matching Window Reduction

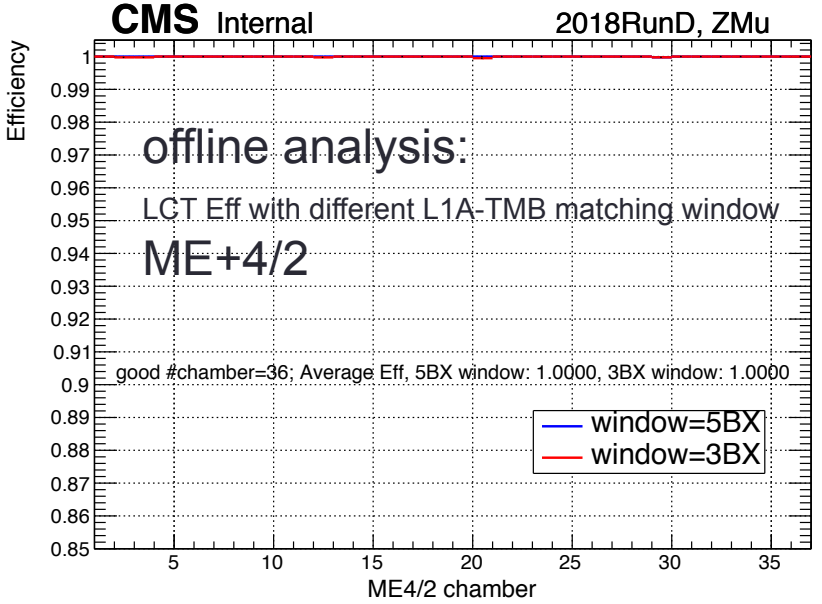


with wide L1A-TMB matching window, earlier L1A (wrong one) read out TMB data while correct L1A fails to read out it

- TMB-L1A matching is to initiate readout of TMB raw hits
- Previous L1A that is 2BX earlier than the real L1A could read out TMB data before TMB data sees real L1A.
- Reducing the TMB-L1A matching window from 7BX to 5BX could recover **~0.25%** TMB data loss by preventing wrong L1A-TMB matching
  - ➡ This changes was done for ME+4/2/8 on Sep. 2018 and analysis results would come in future
  - ➡ Another offline analysis showed no LCT efficiency loss even if L1A-TMB matching window is reduced to 3BX for ME+4/2

L1A-TMB Matching Window Reduction: 7BX to 5BX for ME+4/2/28





- L1A-TMB matching window for ME+4/2/28 is reduced to 5BX and with proper configuration changes, L1A location distribution is also centric in 5BX window
  - Flat distribution in two shoulders (bin0,bin1, bin3 and bin4) + good CSC timing resolution may indicate that the window can be further reduced. (Note: HL-LHC, CMS L1Trigger rate ~750k)
- Offline analysis showed no LCT efficiency loss even if L1A-TMB matching window is reduced to 3BX for ME+4/2
  - Associate L1A location in TMB matching window to LCTs in CSC unpacker
  - Run Tag&Probe package to associate LCTs to reco muon
  - Check LCT efficiency of reducing L1A-TMB matching window. LCTs in denominator of efficiency definition are all probe LCTs in Tag&Probe method
  - Potential TMB data recover from window reduction is ~0.25%, from UCLA