

Joint Workshop w/ Muon Upgrade Group

Costas Vellidis & Jacobo Konigsberg - November 28, 2018

PHASE 2 L1 TRIGGER

MUON ALGORITHMS

LANDSCAPE

O Landscape

O Goals & some questions
O Group Organization
O Context: of Phase-2 L1 trigger
O Progress & work in progress

in very broad strokes

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PRESENTATION OUTLINE

o <u>Some references</u>

- Madison Phase-2 L1 Workshop June'17
 - https://indico.cern.ch/event/525046/
- Interim L1 Upgrade TDR Sept'17
 - CERN-LHCC-2017-013; CMS-TDR-017
- UK Phase-2 L1 Workshop May'18
 - https://indico.cern.ch/event/718306/
- C. Vellidis talk CMS Week June'18
 - https://indico.cern.ch/event/738430/
- L1 Phase-2 Annual Review, Nov'18
 - https://indico.cern.ch/event/766394/





THE NARROW LANDSCAPE













SOME OF THE ISSUES

• what gets done where?

MUON **TYPES**

CORRELATOR

- standalone MuTk, matched to TTk
- TTk matched to just muon stubs
- isolated, displaced
- slow, non-regional, topological





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- TTk matched to just muon stubs
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• how to deal with duplicates/fakes/missing tracks?

CMS

TRIGGER

MENU





- flexibility to grow, to upgrade
- issues of uniformity, cost

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 regional segmentation and TMUX issues displaced and/or isolated tracks in TT ? • how to deal with duplicates/fakes/missing tracks? • can outer layer TT stubs be used in the MTF's?

SOME OF THE ISSUES

• what gets done where?









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CMS

TRIGGER

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benchmark all phase-2 code in CMSSW

- modular for easy comparisons of TP's and algo's options
- validate vs. data [e.g. rates, low level occupancies etc.]



- displaced and/or isolated tracks in TT ?
- can outer layer TT stubs be used in the MTF's?

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SOME OF THE **ISSUES**

• how to deal with duplicates/fakes/missing tracks? • can outer layer TT stubs be used in the MTF's?









O Develop trigger algorithms for each muon type

- standalone, matched to TTk's (Tk-Tk, stub-Tk)
- isolated, displaced, slow, topological (e.g. $au
 ightarrow 3\mu$)
- include new, multiple-detector, systems for TP's and algorithms
- o Maintain high efficiency (>95%) at acceptable rates
- O Lower thresholds if possible
- o Optimize p_T , η , Φ resolutions
- O Demand good performance vs PU, with safety margins (~300)
- O Test robustness vs: inefficiencies, aging, dead regions, noise, neutron bcknd, etc.
- o Explore synergies across the different detector regions
- o Build SW infrastructure tools for development and optimization
- o Build FW/HW demonstrators consistent with phase-2 platforms to test and develop further

WORK ADVANCING RAPIDLY ON MOST FRONTS, BUT STILL ON R&D PHASE

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GROUP MAIN GOALS





o Formed (post iTDR) at UK Workshop, May'18

<u>https://indico.cern.ch/event/718306/</u>

o Subgroup of L1 P2 Upgrade Group

o Mailing list: <u>cms-l1p2-muon-algo@cern.ch</u>

- send requests for new subscriptions to: konstantinos.vellidis@cern.ch
- **O** Bi-weekly meetings
 - Tuesdays 14:30-16:30
 - typically very full Agendas
- o L3 Coordination meeting
 - bi-weekly, Thursdays 15:00
 - exchange info and discuss common issues



GROUP ORGANIZATION



CERN-LHCC-2017-013 CMS-TDR-017

The Phase-2 Upgrade of the CMS Level-1 Trigger

Interim Technical Design Report

CMS Collaboration





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GENERIC BI-WEEKLY AGENDA





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GENERIC BI-WEEKLY AGENDA





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PHASE-2 L1 ITDR DESIGN

Particle flow candidate creation assignment for all of the above Early MTD timestamping of all

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Phase II Project Overview: A. Zabi

- Project organisation & team assembled
- Project timeline & milestones (description of the steps towards the delivery of the TDR)
- Description of the system's interfaces and status of specification: Tracker, Pixel, MTD, Muons, Calorimetry & HLT.

Highlights on algorithms and Level-1 Menu: C.Vellidis, P. Harris & C. Botta

- Review of latest menu developments and plans.
- Recent progress algorithms (and performance) and challenges to address.
- Status of firmware implementations (resources & timing) and validation results.

Status of hardware: D. Acosta

- Focus on recent progress of the multiple R&D lines (prototypes submission & validation).
- Recent board test results (example of test setups) as well as system demonstrators.
- Associated services: software, infrastructure, use of HLS etc.

Architecture consideration: J. Berryhill

- Architecture developments based on targeted trigger object performance and future optimisations according to physics need and LHC running conditions.
- Examples of architectures, evaluation of the timescale to identify a target system design.
- Considerations on instrumentation (R&D and Technologies available) and demonstration.
- Possible planning on construction, timing alignment, commissioning and robustness of the system

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AGENDA ANNUAL REVIEW

14:05 → 14:50	Overview of the Phase II Upgrade L1 Trigger Project
	30min+15min discussion
	Speakers: Dr Alexandre Zabi (LLR-Ecole Polytechnique CNRS-IN2p3), Jeffrey Berryhill (Fermi National Accelerator Lab. (US))
	PhaseIITrigger_Proj
4:55 → 16:05	Highlight on the trigger algorithms development, performance studies and implementation
	 C. Vellidis Muons (20 min) Calorimeter algorithms, tracker based objects, PFlow and Vertexing (25 min) P. Harris Menu developments (10 min) C. Botta
	55 min + 15 min discussion
	Speakers: Cristina Botta (CERN), Konstantinos Vellidis (National and Kapodistrian University of Athens (GR)), Philip Colema Technology (US))
	MenuReport_Trigg 🖉 MuonStatusReport
6:05 → 16:30	coffe & Tea
6:30 → 17:15	Progress on Hardware for the Phase II Trigger
	30min+15min discussion
	Speaker: Darin Acosta (University of Florida (US))
	Phase2TriggerHard Phase2TriggerHard
7:20 → 18:05	The Phase II Trigger Architecture and Interfaces
	30min+15min discussion
	Speaker: Jeffrey Berryhill (Fermi National Accelerator Lab. (US))
	berryhill p2l1t arch

LOTS OF GOOD QUESTIONS BY REVIEWERS, NO WRITTEN REPORT AS OF YET...



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WORK IN PROGRESS

A Quick Overview

Details in the Muon Group presentations in this Workshop



O Assumptions so far

 Trigger primitives are as in Phase-1, muon track segments [in CMSSW] New TP developments should be tested and compared Using the "tracklet" algorithm for Track Trigger • With recommended # of stubs >3 and chi-square<100 [susceptibility to this to be studied]</p> • TMT algorithm also available and TT group developing a new hybrid algorithm => to be tested Regional segmentation as in Phase-1 • Algorithms & HW demos being developed so far specifically for Barrel / Endcap /Overlap Will consider later if to be reduced to two regions

• This is still the R&D phase

- Good to explore new/innovative algorithms and be able to compare performance For TDR baseline, find at least one good solution for each problem Post-TDR continue with optimization and consolidation

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MUON ALGORITHM DEVELOPMENT OVERVIEW



o Barrel standalone muon reconstruction

- Via Kalman Filter algorithm UCLA, Ioannina, Athens
- Implemented in 2018 Run 2
 - Optimized algorithm fits in same FPGA with legacy algorithm
 - Very reasonable phase-2 rates (few KHz @ 20 GeV)
 - Similar efficiency as legacy BMTF
 - Very good solution for triggering on displaced muons [next slide]
 - no beam-constrained propagation
- Will be used during Run 3 data taking



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Kalman-Filter and legacy algorithm running simultaneously during 2018 data taking on XILINX Virtex 7-690T FPGAs

2018 zero-bias data

rate (kHz) vs p_T threshold

muon rec. efficiency vs pT



o Barrel KF displaced muon reconstruction

- Use cosmic data in collisions as a proxy
- Significant improvement in efficiency for displaced muons w/ dxy > 30 cm
 - across all p_T's
- Low rates O(10 KHz) for $p_T > 20$ GeV
 - Super low for dimuons
- More comprehensive simulation studies with displaced muons samples in progress



Efficien

0.2

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BARREL DEVELOPMENTS OVERVIEW









o Endcap standalone muons Florida, Fermilab

- One problem to solve: non-linear rate vs PU
- New phase-2 algorithm EMTF++
 - Uses hits in all muon detectors: CSC, RPC, GEM, MEO, iRPC to form more precise patterns consistent with muon trajectories
 - Replaces phase-1 BDT ⇒ DNN trained with info from stubs in

patterns to determine the muon p_T of the track

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φ θ bend	ME1/1	ME1/2 · · ·	ME2 ✓ ✓ ✓	ME3	ME4 ✓ ✓	RE1 ✓	RE2	RE3	RE4	GE1/1	GE2/1	ME0 ✓ ✓
φ θ bend F/R	ME1/1	ME1/2 ME1/2 ME1/2 ME1/2 	ME2 	ME3	ME4	RE1	RE2	RE3	RE4	GE1/1	GE2/1	ME0
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See endcap presentations on Thursday

ENDCAP DEVELOPMENTS OVERVIEW



SingleMu22 rate vs PU {0:85}





o EMTF++ performance

- sharper turn on, higher efficiency
- ~10kHz @ 20 GeV => x3 rate reduction !
- Low rate & linear with PU !



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ENDCAP DEVELOPMENTS OVERVIEW





o TT tracks matched to EMTF standalone muons

- Use dynamic matching window $\Delta R(p_T)$
 - instead of constant ΔR as in TDR
 - can tune windows to desired efficiency
- sharp turn-on, higher efficiency
- ~10 kHz @ 20 GeV => x5 rate reduction



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o TT tracks matched to muon stubs

- Also use dynamic matching window $\Delta R(p_T)$
- Used CSC or RPC stubs only so far
- Station 2 => low rates and high efficiency
- Very reasonable rate (10-20 kHz) @ ~20 GeV
 - Station 1 rate significantly higher



PU200 - efficiency vs pT {0-100 GeV}

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ENDCAP DEVELOPMENTS OVERVIEW





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o First test algorithms on phase-1 HW platforms (as with barrel), then move to phase-2 platforms • Aim to test in parallel in Run 3

CTP7-based system using simulated files for muons and for TT test matching and displaced muon algorithms



- TP algorithm (simple) propagation and fixed matched windows)
 - synthesised with HLS
 - implemented in CTP7 board for demonstration
- Small resource usage (~1%) but large latency (100 clock
- \rightarrow ~0.5 µs) for track propagation
- Investigating ML methods for
- propagation (reduce latency)
- classification: matched and unmatched muons (displaced)

See presentations on Thursday

Implementation of the p_T DNN in MTF7 setup



- Tried VU9P US+ FPGA, Device ID: xcvu9p-flga2104-2-i
- Targeted by the USCMS APD board 0
- Reuse factor =1, Clock = 333MHz

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xed Latency is 24 cycles 333MHz this is 72ns

The algorithm should fit comfortably in FPGAs considered for Phase-2 boards

- \succ Low latency, easily fits in FPGA
- Can prune the NN to further reduce resource usage
- > EMTF++ part is getting started
- > Plan to install and test the NN algorithm, in Run 3

TAMU



o First step is testing the phase-1 algorithm in phase-2 conditions

O Naive Bayes Classifier

 Assumes the lo a muon has a g log-likelihoods in each detectc player(pT | $\Phi_{dist in la}$



• The maximum log monitor prisonosci as the muon p_T

OPU140 vs PU200

- efficiencies similar slow turn on
- But rates are now reasonable ~ 20kHz @ 20 GeV

See OMTF presentations on Thursday

OVERLAP DEVELOPMENTS



rates (kHz) vs p_T {0-200 GeV}





o TT track + muon stub

- A straightforward extension of the algorithm proposes to replace muon Φ with ΔΦ between TT track and muon stub in the log-likelihood of the hit positions
- The first preliminary version of the algorithm is almost implemented in the OMTF emulator (**n** not yet included)
- Work ongoing to develop a TTtrack-stub likelihood
- Performance and optimization will follow

OVERLAP DEVELOPMENTS

efficiency vs p_T {0-100 GeV}



OMTF efficiency in the plateau ~98%

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- A development framework:
 - Full simulation+emulation chains for BMTF, OMTF, EMFT
 - Ability to compare algorithms, apples to apples, with the full chain
 - Universal Muon Ntuple format to facilitate studies, for reproducibility and long-term development

• Need complete MC menu (vs PU), up to high PU

- Single muon and neutrino gun samples
- High-p_T muon physics: tt, Z', H=>mm
- Low p_T muon physics: j/psi, B-physics
- Displaced muon samples w/displacement range
- Special cases e.g. tau=>3mu etc. etc.
- Need ability to deteriorate detectors
 - Inefficiency, aging, noise, neutron background





Already organised for 2019 :
1st Workshop (March) → Converge on baseline algorithms and menu.
2nd Workshop (May/June) → Converge on hardware and architecture

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TIMELINES & TIMELINES

Milestone	Date	Description
ITDR.L1.1	Q3 2017	Interim Report submitted
ITDR.L1.2	Q1 2018	Software emulator demonstrates implementation of core phase-2 menus with prototype algorithms
ITDR.L1.3	Q2 2018	Prototype algorithms implemented in firmware
ITDR.L1.4	Q2 2018	Benchmark performance baseline and menu for representative sample of core trigger algorithms
ITDR.L1.5	Q2 2018	Definition of hardware technology implementation baseline
ITDR.L1.6	Q3 2018	First hardware prototypes produced
ITDR.L1.7	Q4 2018	1st-generation demonstration setups show local comparison with emulators
ITDR.L1.8	Q4 2018	Updated core trigger algorithms implemented in software emulator
ITDR.L1.9	Q1 2019	Updated core trigger algorithms implemented in firmware
ITDR.L1.10	Q1 2019	Benchmark performance baseline for updated core trigger algorithms
ITDR.L1.11	Q1 2019	Initial architecture defined for slice tests
ITDR.L1.12	Q2 2019	Updated hardware prototypes produced
ITDR.L1.13	Q3 2019	2nd generation demonstrators show integration and scaling; allows global/full- chain comparison with emulator
ITDR.L1.14	Q1 2020	Technical Design Report submitted

TDAQ: Annual Review

Full project review: assess projections for performance, hardware prototype status, plans towards architecture... 13/11/2018



TDAQ AR A. ZABI

TOWARDS A TDR FOR 2020

- and firmware for the year 2019.
- February/March \rightarrow add description of the baseline algos & menu in TDR.
- potential) to UPSG for approval.
- fulfil performance requirement exposed in February should be met.
- Level-1 TDR review and editing.
- **September 15th 2019:** Finalise the TDR and TRIDAS approval. Release to ARC.
- November 31st 2019: TDR finished (Collaboration comments implemented)
- adjusted depending on LHCC load? (Discussed with Frank/Didier if they really need 3 months and if 2 months are acceptable?)
- meeting (question for Frank/Didier: this can happened at the same time?)
- **XX June 2020:** Full approval by LHCC, publication of the TDR

October/December 2018: Preparing Annual Review. Starting to write the TDR now: organisation/ chapters. What are the plots and results required from the L3 groups ? Finalise planning of hardware

Feb/March 2019: Converge on studies of algorithms and their performance. Baseline for all objects and complete menu for phase II scenarios. All plots to be approved at the L1 Trigger workshop

March/April 2019: Submission of performance plots and physics related studies (physics reach/

May 31st 2019: Preparing review of all hardware and architecture. Presentation of results from demonstrators for each subsystem and architecture at the 3rd workshop. All specifications needed to

June 30th 2019: Integration of the hardware description and architecture into the TDR. Start internal

October 31st 2019: All comments and modifications from the ARC integrated. *Submission for CWR*. **December 15st 2019** (or January 2020): TDR Submission to LHCC (delay before submission to be

XX February/March 2020: Scientific Approval from LHCC & UCG kickoff meeting during LHCC

O Significant progress since the iTDR

- Standalone and TT track matching algorithms well advanced in Barrel and Endcap. Overlap catching up.
- Displaced muon algorithms advancing in Barrel. Endcap and Overlap need to catch up.
- o FW advancing on all fronts. Barrel KF already running in P5
- O Demos advancing on phase-1 HW platforms, need to move to phase-2 when boards available
- Still lots to do: algorithms for other muons types: isolated, slow, multi-region, close-together etc.
- TDR outline being worked on => confident we'll reach a solid baseline

IN SUMMARY







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TDAQ AR A. ZABI

INTERFACE WITH MUON SYSTEMS

WHAT KIND OF TRIGGER PRIMITIVES

DT Stubs: definition here (same as phase I) **RPC Clusters:** definition here (same as phase I) **CSC Stubs:** same format as phase I (improved algo and timing) New Trigger primitives (Endcap):

iRPC hits: no eta segmentation, precise timing **GEM ME0 stubs:** precise position (eta/phi) and direction

Table 8.9: Improved RPC (iRPC) trigger	Table 8.12: Muon Endcap ME0 Station stub word definition					
Quantity Detector ID ASIC ID Channel ID Signal time rising edge Signal time falling edge	N bits 5 2 6 14 14		QuantityN bits ϕ coordinate10 η coordinate5Pattern7Quality2Total24			
Total RPC hits = 41 bits	41		Table 8.10: Muon Gas Elec	Extron Multiplier (C Quantity ϕ sector η partition Pad number Chuston size	GEM) trigg N bits 2 3 6 2	er cluster digi definition.
			GEM clusters = 14	Total	<u> </u>	

GEM Clusters: grouping hits in GEM layers (also sent to CSC to build CSC-GEM TP w/ CSC format)



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