# A Level1 ME0-Pixel Muon Trigger for HL-LHC

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*Thanks also to the work by J.Kim (SNU), J.Lee and H. Lee (KNU) on the electron Pixel-based L1 Trigger studies for HL-LHC which closely inspire the ME0-Pixel Seeding.*

# Outline

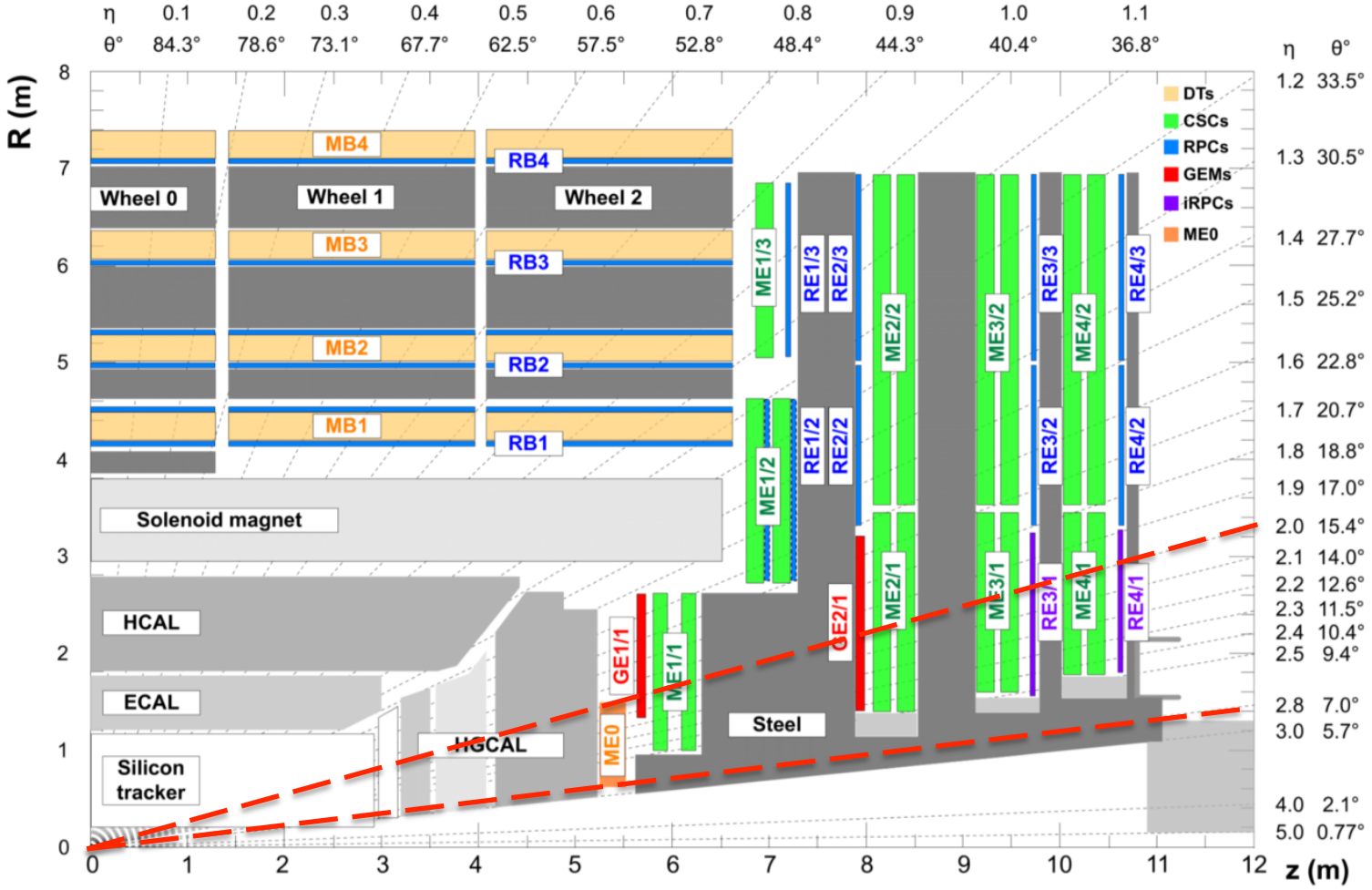
- Introductory remarks on the L1 Pixel based trigger feasibility studies
- Feasibility studies on a L1 Pixel based Muon trigger using the ME0 as a seed.
- Preliminary ideas about the hardware possible implementation

# Introductory remarks

- A collaborative effort has very recently started between people working on the ME0 detector and on the L1 Pixel based Trigger project
- The goal is to study the feasiblity and benefits of a Level 1 trigger combining the ME0 with the Pixel informations.
- This is work in progress, still in the preliminary phase
- It closely follows the feasibility studies we already achieved for the electron *and especially the strategy we defined as PiXTRK (see next slides)*
- *This trigger is a **seeded trigger:** the SEED is provided by the ME0.*

# **L1 Pixel based Muon trigger seeded by ME0**: *preliminary feasibility studies*

# *ME0 & Pixel detectors for HL-LHC*

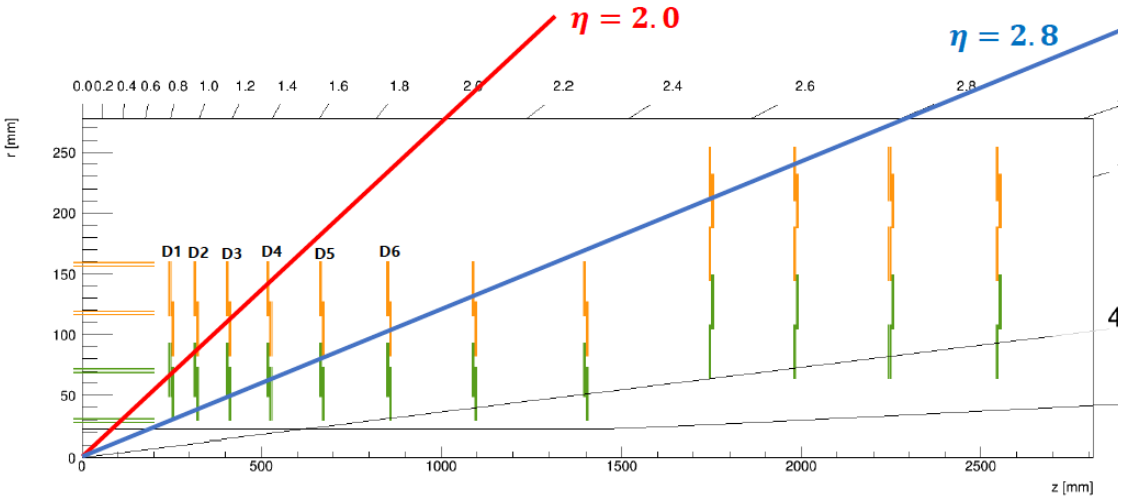


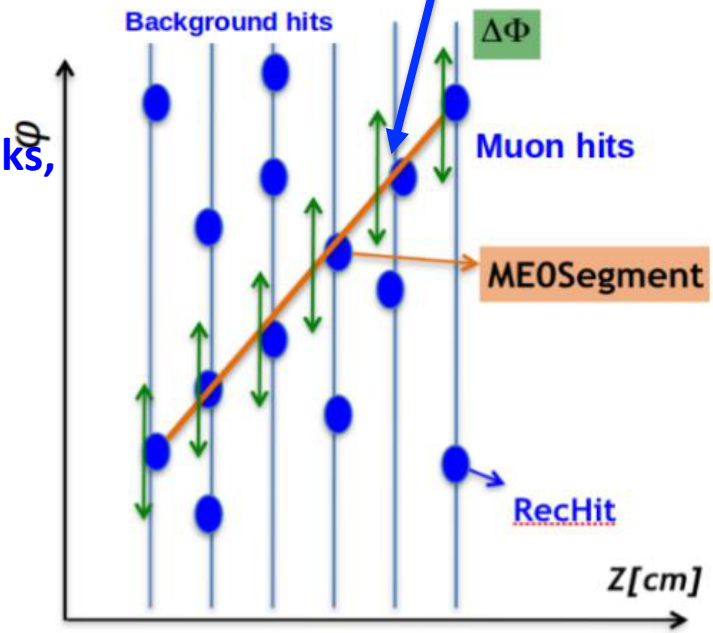

- ME0 covers the **forward region** defined by: $2.0 < \eta < 2.8$
- The Pixel disks can be matched with ME0 in this overall region and:
  especially in $2.4 < \eta < 2.8$ not covered by the Outer Tracker

# The ME0 muon track segment: the SEED

**The SEED is provided by the ME0 Segment.**
This ME0 segment is defined from the hits aligned along the 6 layers of this detector.

**Next: Look for the pixel clusters, in at least 3 out of 4 disks, matching with the ME0 segment**




***The preliminary feasibility study presented here uses a sample of 2 M. single No PU muons based on CMSSW_9_3_7 simulation framework.***
***And the study is conducted within CMSSW_10_1_5 framework.***

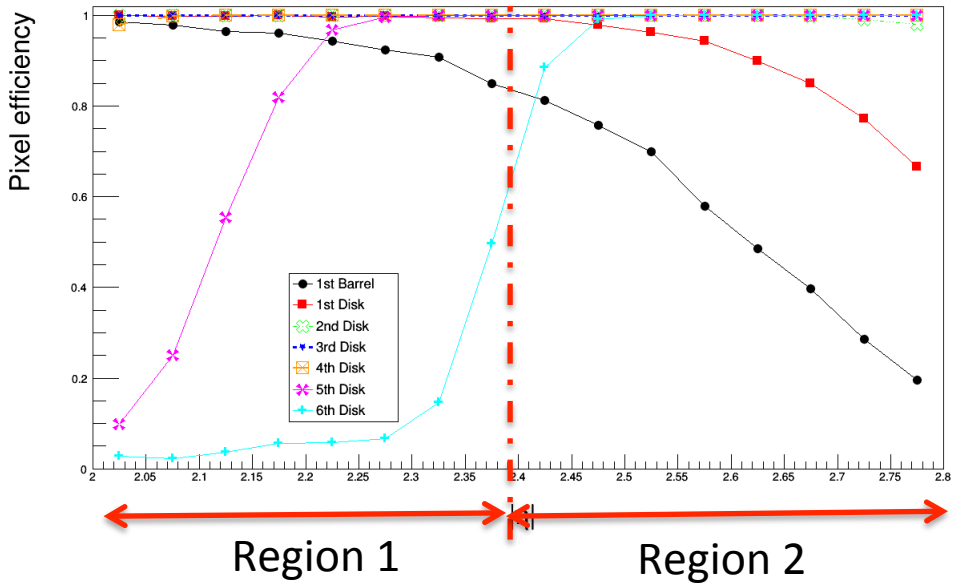
# PiXTrK strategy applied to ME0 Muons

***1) Selection of disks regions with highest efficiency:***

Two regions in η are defined gathering each 4 disks.
They correspond to a pixel efficiency of 100%.
The pixels are chosen as being the closest ones to the ME0 segment.

$$eff = \frac{\#\ of\ event\ passing\ me0\ \&\ pixel}{\#\ of\ event\ passing\ me0}$$

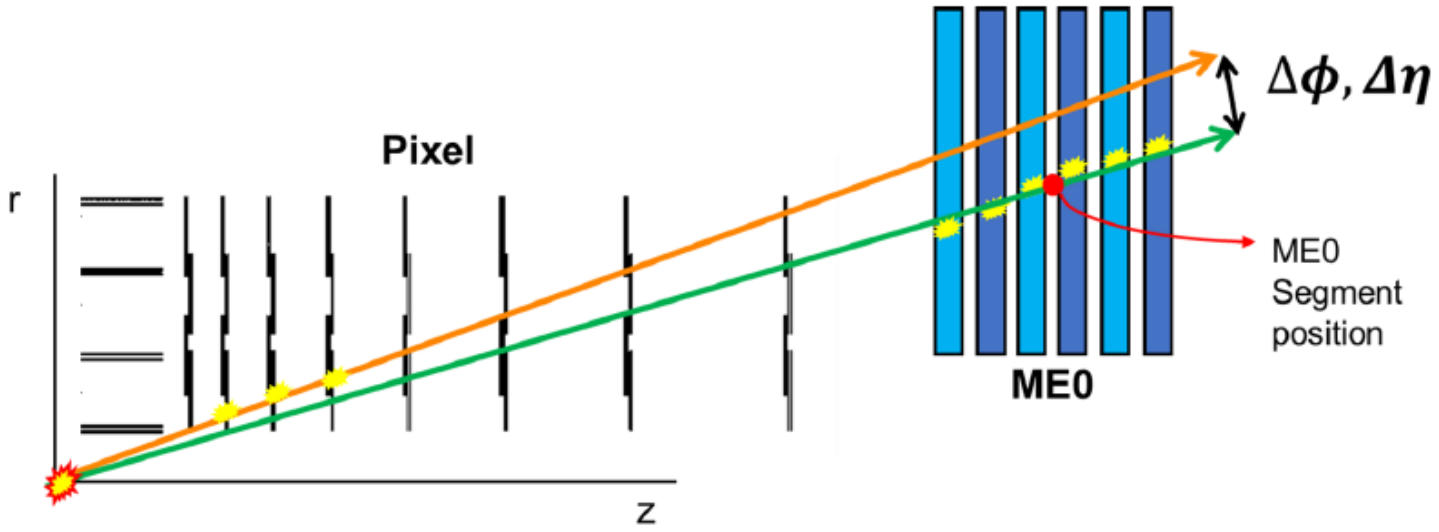
| | Selection of pixel |
|---|---|
| **Region 1** | D1, D2, D3, D4 |
| **Region 2** | D2, D3, D4, D5 |



# PiXTrK strategy applied to ME0 Muons (cont'd)

***2) Signal Windows: definition***

- Define $\Delta\phi$, $\Delta\eta$ from vectors connecting ME0 segment, pixel hit and primary vertex.
- Signal window is measured by matching pixel track and ME0 segment.



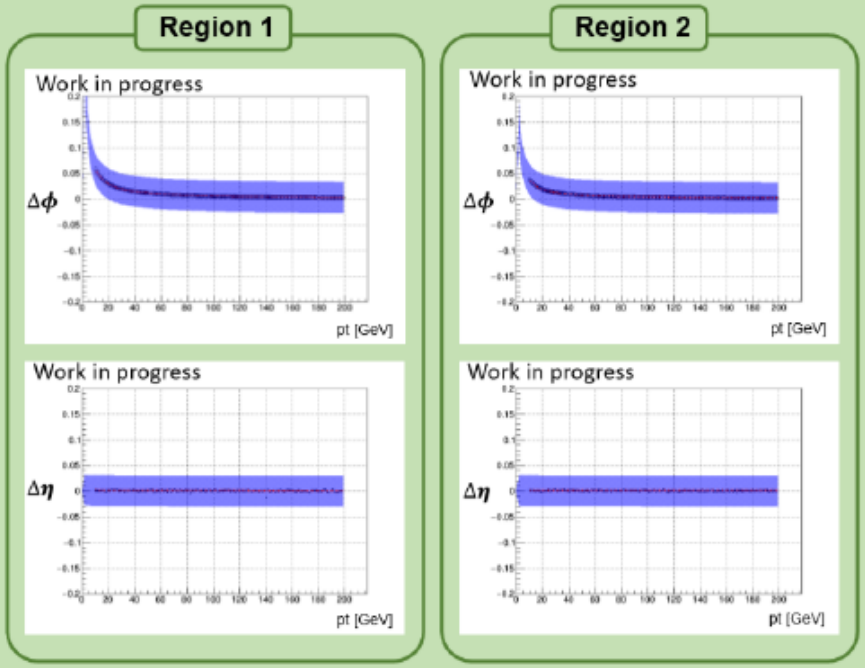

The matching between ME0 segment and the Pixel track segment is based on requesting clusters in 3 out of 4 disks

# PiXTrK strategy applied to ME0 Muons (cont'd)

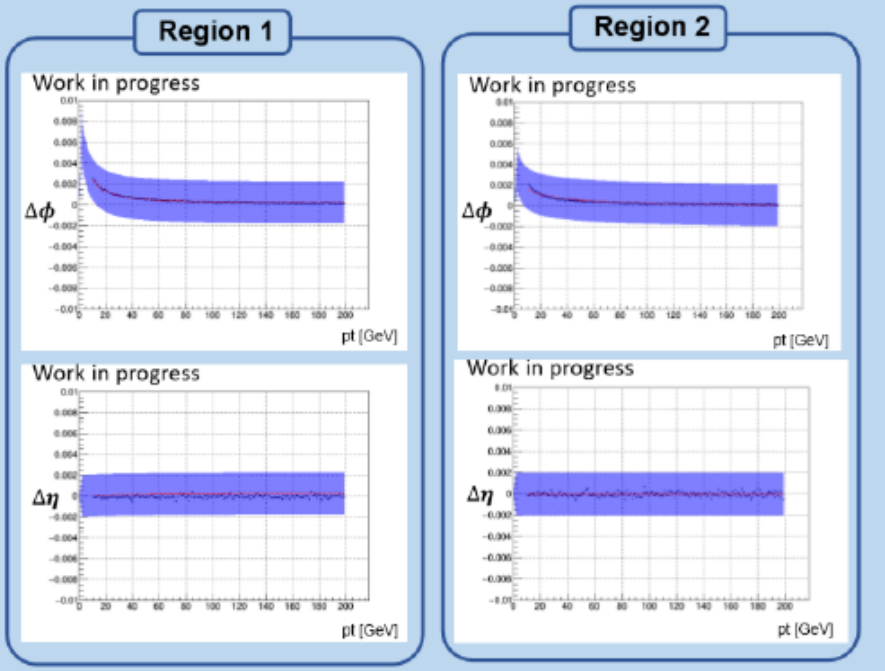
### *3) Δη & ΔΦ Signal windows for ME0-pixel matching and pixel-pixel matching*

- ME0-pixel matching SW and pixel-pixel matching SW are calculated by median value of $\Delta\phi$, $\Delta\eta$ according to gen-level Pt.
- Muon signal is determined to pass all signal window.

**Example of ME0-pixel matching SW ($D_{1st}D_{2nd}$-ME0)**



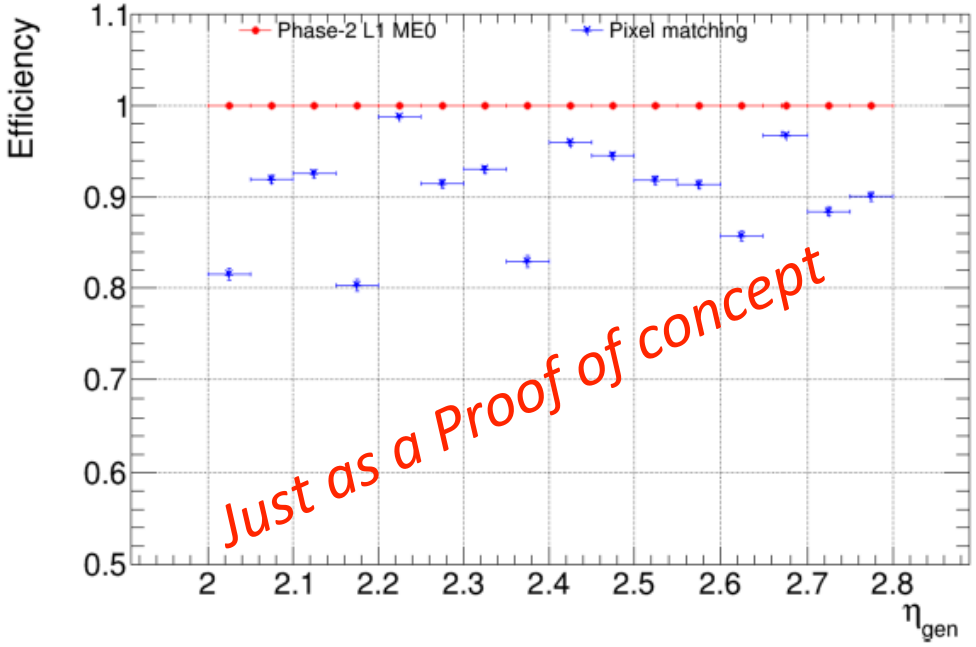

**Example of pixel-pixel matching SW ($D_{2nd}D_{3rd}$-$D_{3rd}D_{4th}$)**




9

# PiXTrK strategy based result:

## *L1 MEO-pixel Trigger efficiency as a proof of concept*




$$eff = \frac{\#\ of\ event\ passing\ L1\ ME0}{\#\ of\ gen\ level\ events}$$

$$eff = \frac{\#\ of\ event\ passing\ all\ signal\ window}{\#\ of\ gen\ level\ events}$$

| Width of signal window | | | |
|---|---|---|---|
| Signal window | | Region1 | Region2 |
| ME0-Pixel matching | $\Delta\phi$ | 0.03 | 0.03 |
| | $\Delta\eta$ | 0.03 | 0.03 |
| Pixel-Pixel matching | $\Delta\phi$ | 0.002 | 0.002 |
| | $\Delta\eta$ | 0.002 | 0.002 |

This trigger efficiency is very preliminary; it is just here as a proof of feasibility of the PiXTrK algorithm applied to the Muon case.

***!! To fully perform this trigger efficiency and Rate estimate, ME0 MUST BE included within the CMSSW10 Simulation framework***

On our side we are ready to finalize these feasibility studies.

# Preliminary idea about the possible hardware implementation

To be combined:
The FE/Readout ME0 detector system
with
the FE/Readout Pixel detector system
within the defined
HL-LHC L1 Trigger architecture

The ingredients to do it are:

# The Front End ASIC for Pixels at HL-LHC developed by RD53

With the following features embedded in:

- Clusterization
- A second fast level trigger included in its design, that can be used as L0 or Region of Interest Fast trigger signal,
- Allowing to send the corresponding clusters to the upper level of the Pixel and L1 trigger architecture

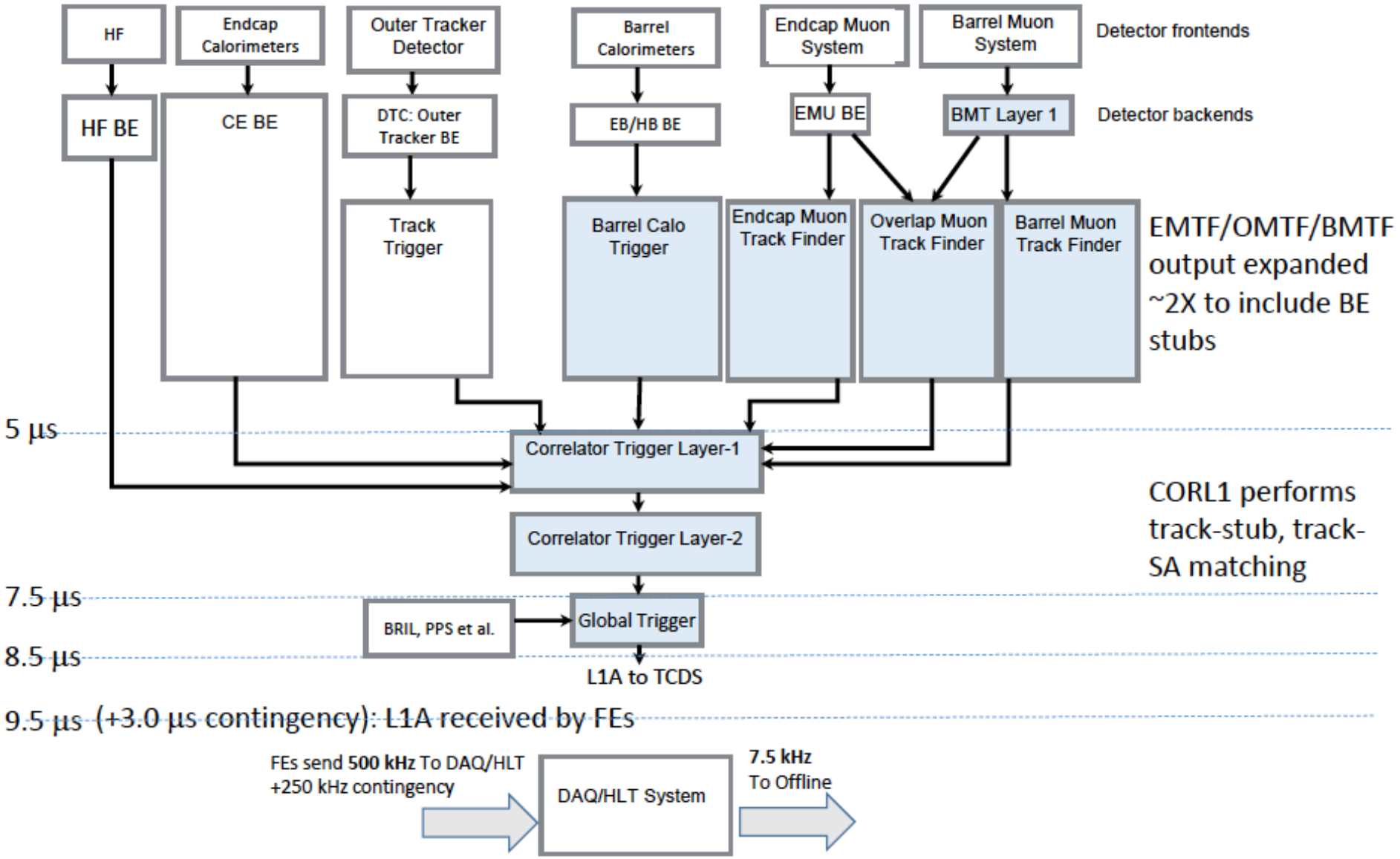
# L0 – RoI signal possibly included in the L1 overall trigger architecture for pixels & MTD

*Slide from J. Brookes at the RAL Workshop, June 2018*

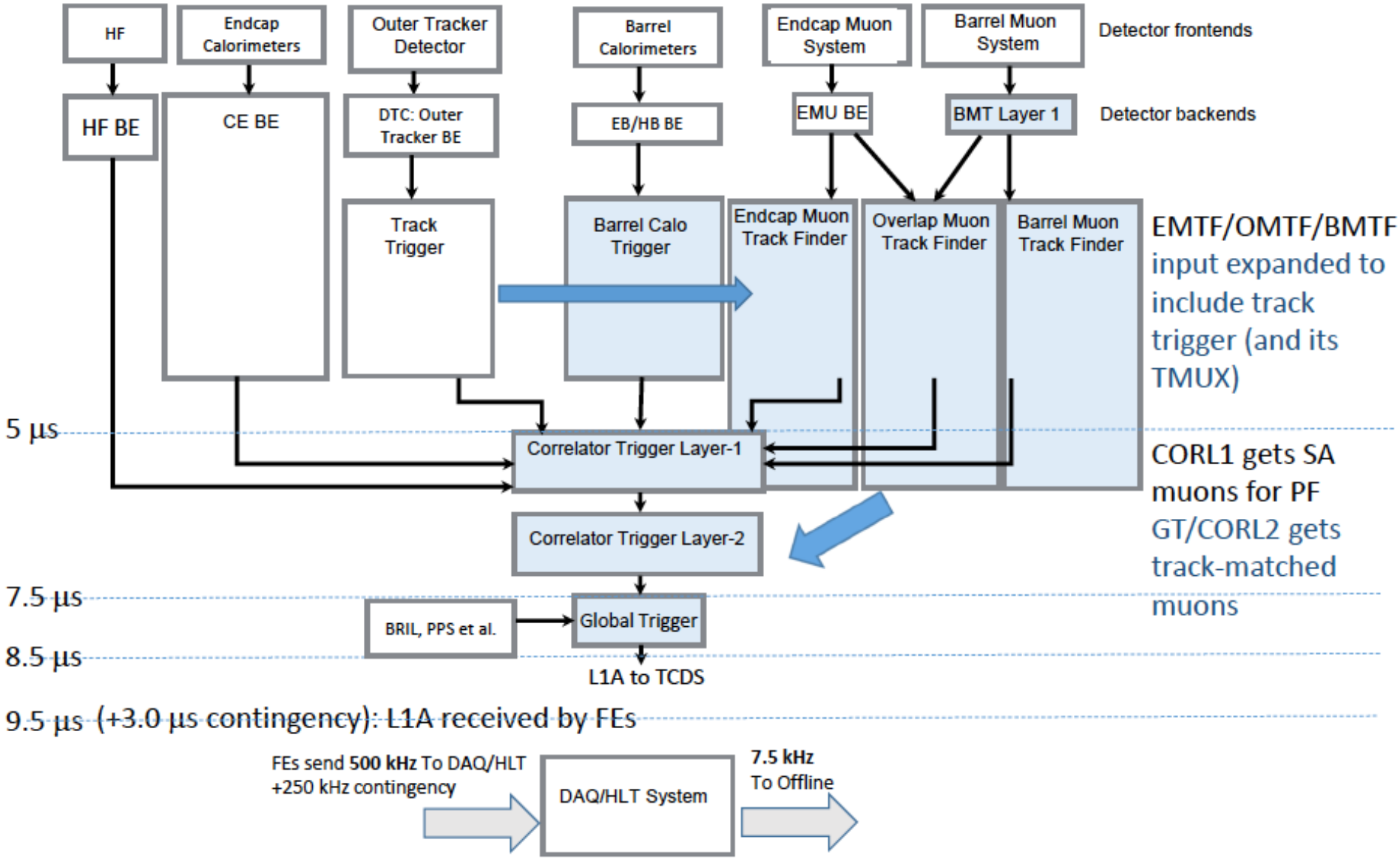
## L0 Trigger

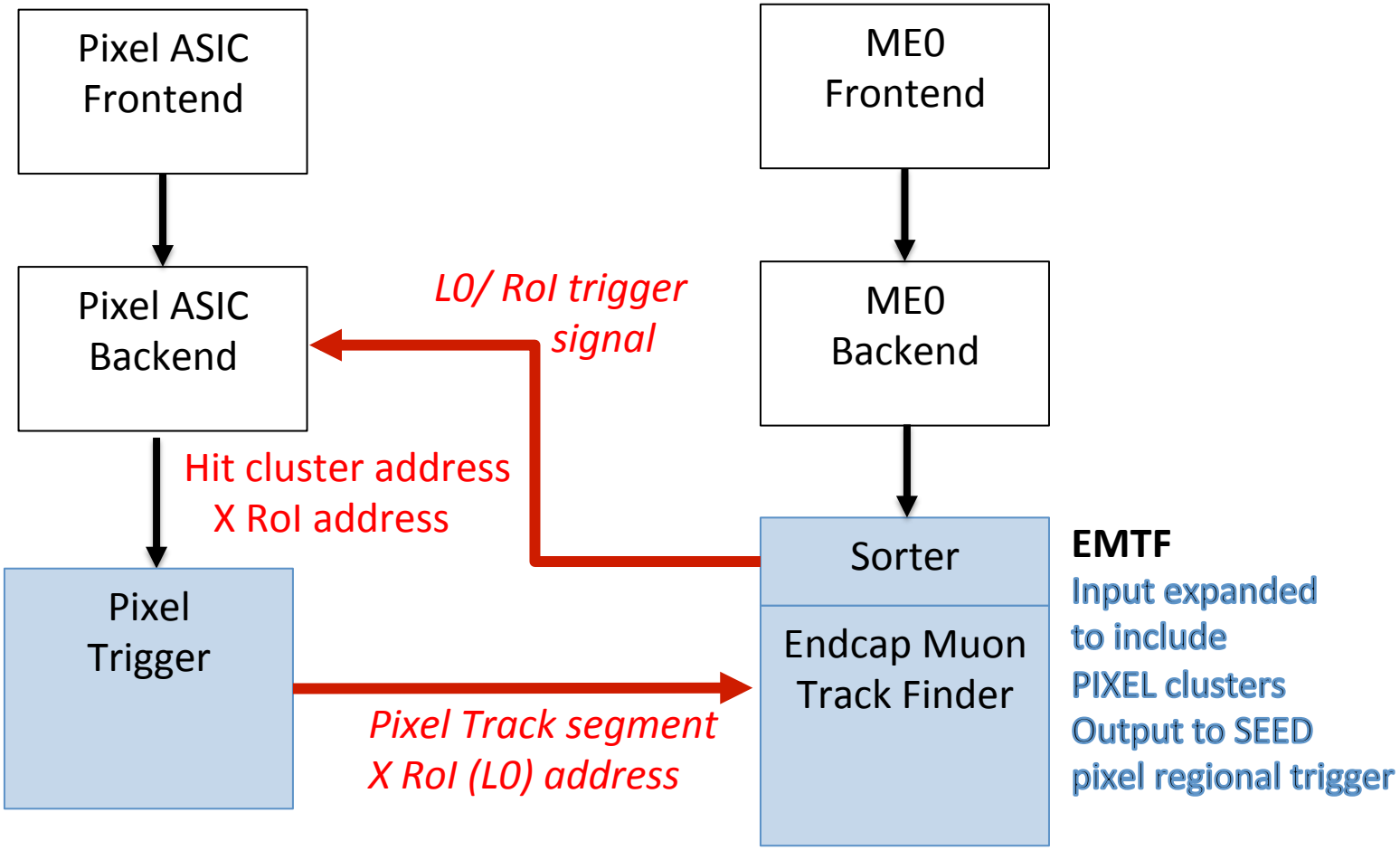
- Current L1 Trigger design assumes all sub-detectors included in L1T can produce trigger-primitives at 40 MHz
- However, it is conceivable that we could provide a L0 trigger to sub-systems that need this, eg. pixels or MTD
  - Generate a trigger from calo/muon(/track?) information early in the chain
  - Send ROI information to pixel/MTD front-ends
  - Constraints arise from latency, internal L1 bandwidth & processing, and introduce new requirements on DAQ/TCDS

# Muon-Track Matching Scenario A: defer to CORL1



# Muon-Track Matching Scenario B: integrate with MTF






Still in progress:

- Pixel ASIC seeded by L0 can quickly send the “Full address” => the location of the corresponding clusters & L0 correspondence (RoI)
- This information might be processed in the FED FPGA with a PiXTrK-like algorithm

In order to reconstruct segments with their geographical address, to be sent to the End Cap Muon Track Finder?

# To conclude

- Matching the information of the ME0 detector with the pixel disks that cover all the needed η region looks feasible and promising: to evaluate the benefits in terms of performances need to implement the ME0 detector within the CMSSW10 framework.
- The corresponding PiXTrK algorithm is developed.
- The basic ingredients to construct a seeded L1 pixel-ME0 based Muon trigger are available both on the pixel FE ASIC and readout side as well as on the ME0 side
- Need a meeting with the experts to study how to make it feasible i.e. gather these different pieces
- The meeting will be prepared next week at CERN during the CMS week.