RPC Link System

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Institute for Research in Fundamental Science (IPM)

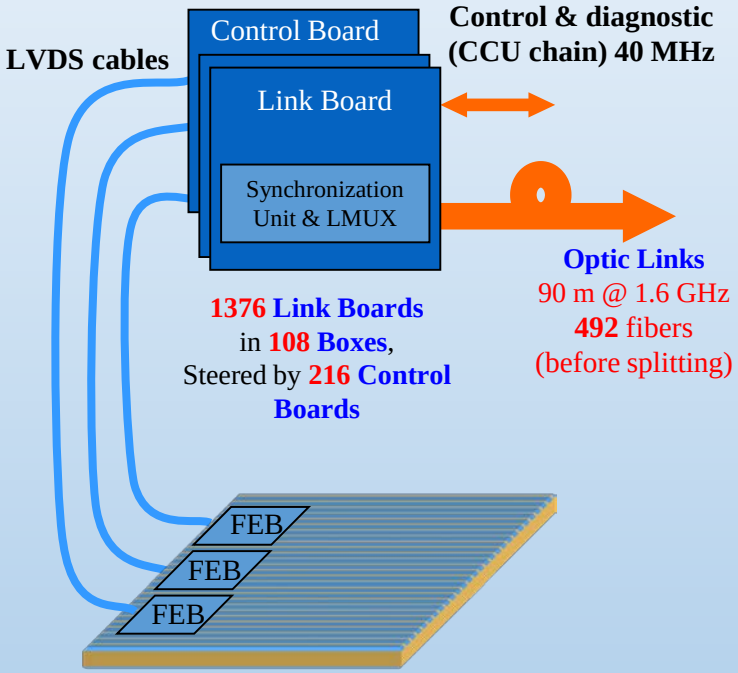
on behalf of the RPC Group

Joint P2 Muon Upgrade + P2 L1 Muon Algorithms workshop

29th November 2018

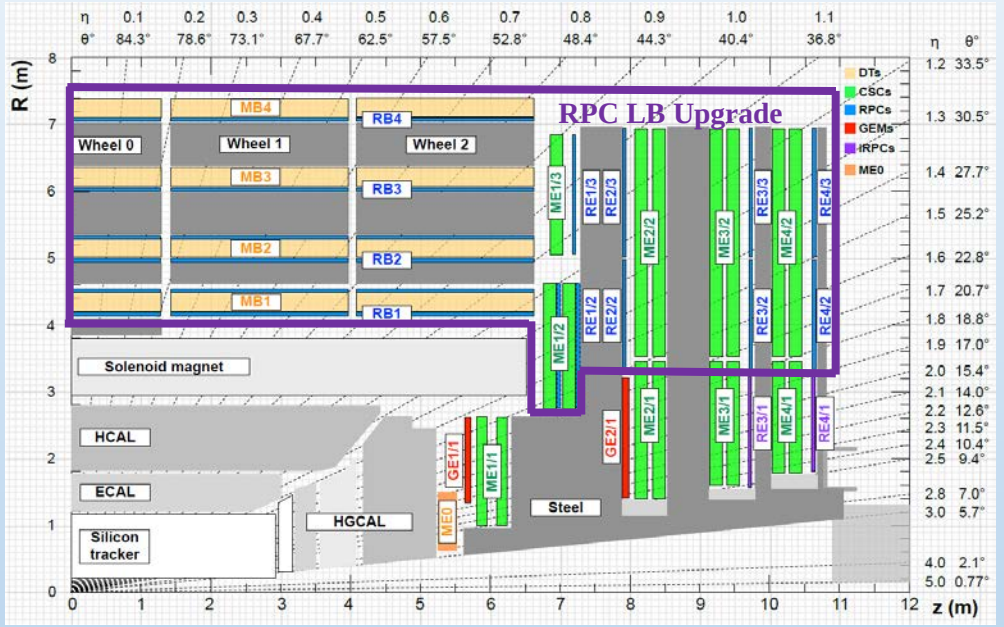
Present RPC Link System

Present Link Board System



Upgrade Motivation

- RPC signals synchronization, **timing resolution is 25ns**
- Data transmission speed is about **1.6 Gbps**
- Control, diagnostic and monitoring of the Link system has been designed based on **CCU ring** (combination of copper cable and fiber optic), very susceptible to electromagnetic interference



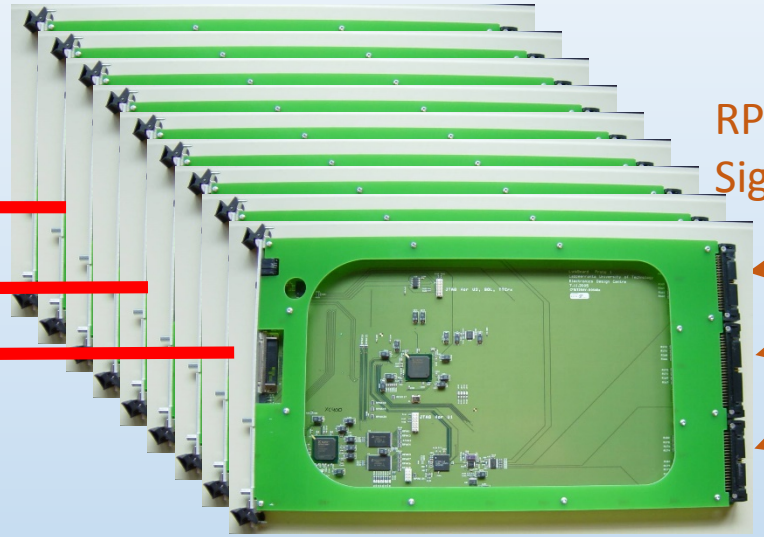
- CCU ring is not very fast, the bandwidth (40 MHz) share between 12 control boards
- Electronic aging, presently the Link system is already 13 years old

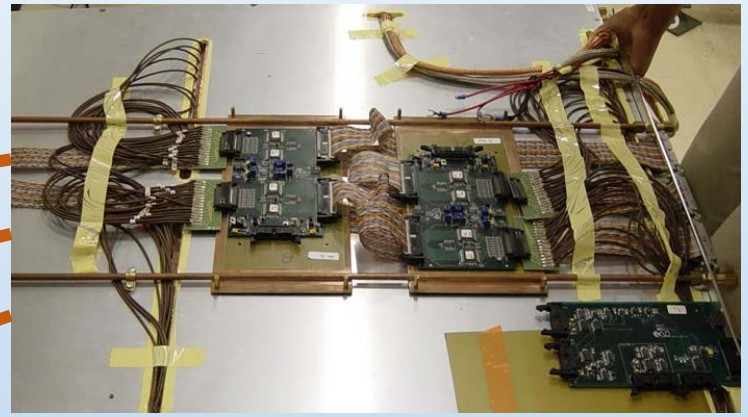
RPC Dara taking Chain

GOL chip output 1.6 Gbps

Legacy PAC / TwinMux , CPPF , OMTF

RPC Signals





Link Board

Slow Controller and Central TTC

Command and Control 40 Mbit/sec

TTC Clock 40.08 MHz

Command and Control (Wire / Redundant)

I^2C Command and Control

Control Board

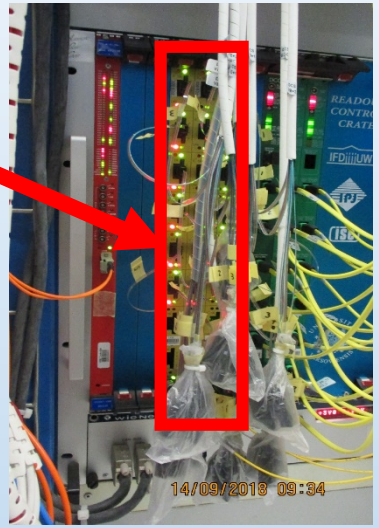
Present Slow controller cards in Rack No. S1F03

- The Slow controller Cards (SCC) placed in Readout Control Crate (RCC)
- Dimension of the SSC Cards and RCC crate is 9U
- Each SCC has 8 fiber optic driver mezzanine boards
- Each one of this mezzanine board drives one optical link
- Each optical Link connected to one CCU Ring via the Opto-hybrid module that installed on the Control board
- In each CCU ring we have 12 Control boards which is connected together as a serial ring

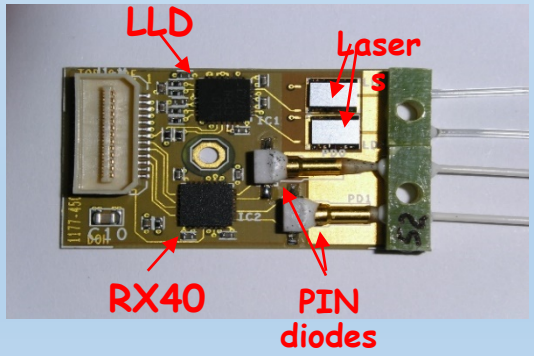
- In total, we have **3 slow controller Cards** installed in the Readout Control Crate and **drive 18 CCU Rings**

Slow **C**ontroller **C**ard

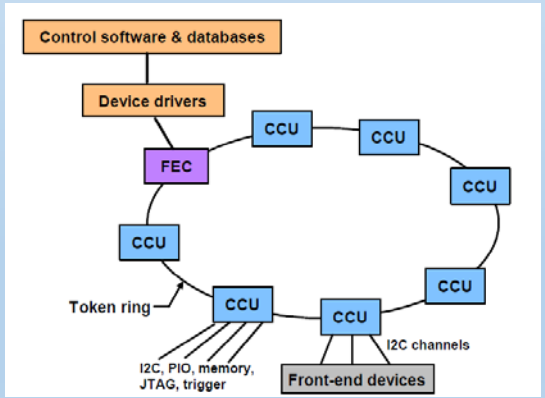
Readout Control Crate



3 Slow controller Cards has been installed on Readout Control Crate specify inside red frame

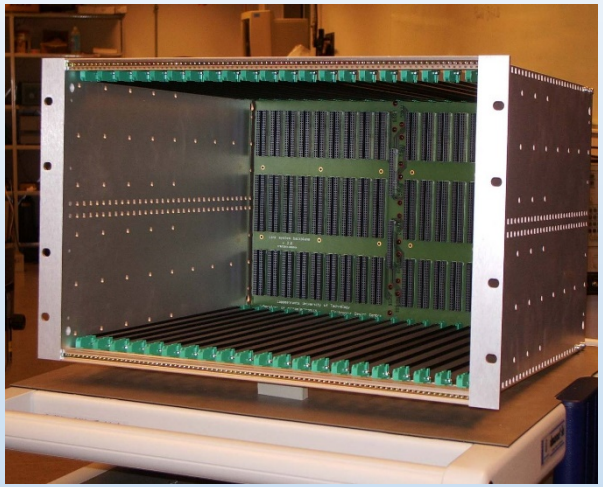


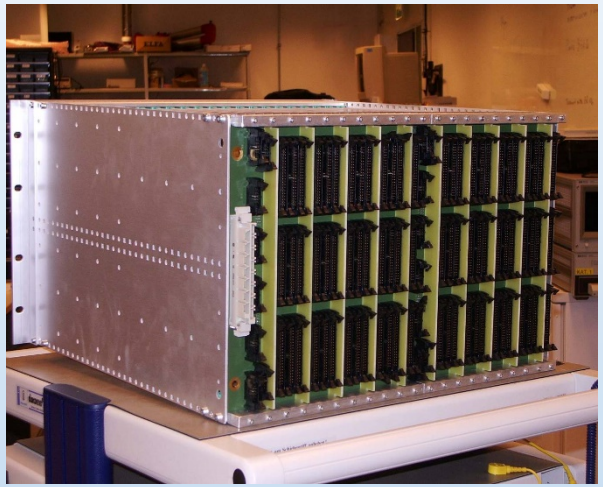
Opto-Hybrid Module



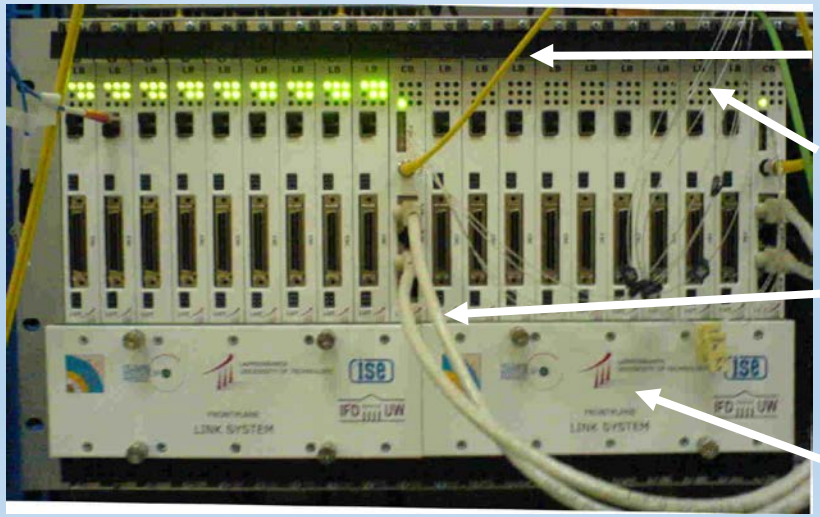
CCU Ring

Present Link system Crate





Customized VME Crate - Link Board Box (LBB)



TTC Fibers (Yellow)

Slow Control Fibers (fiber string)

Slow Control Copper Cable

Front Panel (Local bus)

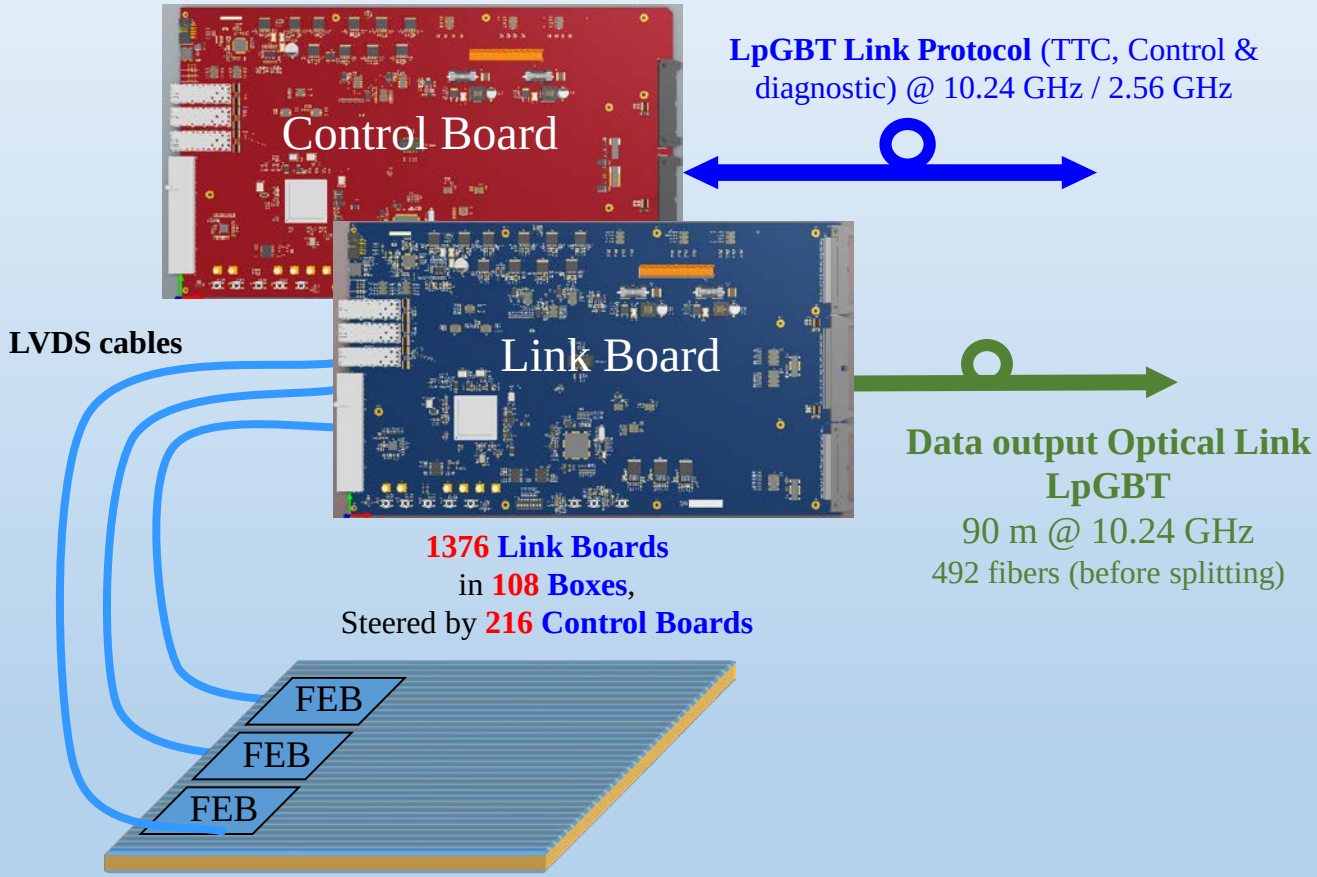
Back Plane

- RPC Signals
- FEB control signals
- Power Supply (3.85V, 2.5V)

- **For the Upgrade Phase-II, The LBB and Back Plane remain unchanged**
- **Only front panel PCB Layout will be modified**

New Link System Overview

Upgrade Phase-II of New Link system



LpGBT Link Protocol (TTC, Control & diagnostic) @ 10.24 GHz / 2.56 GHz

Data output Optical Link LpGBT
90 m @ 10.24 GHz
492 fibers (before splitting)

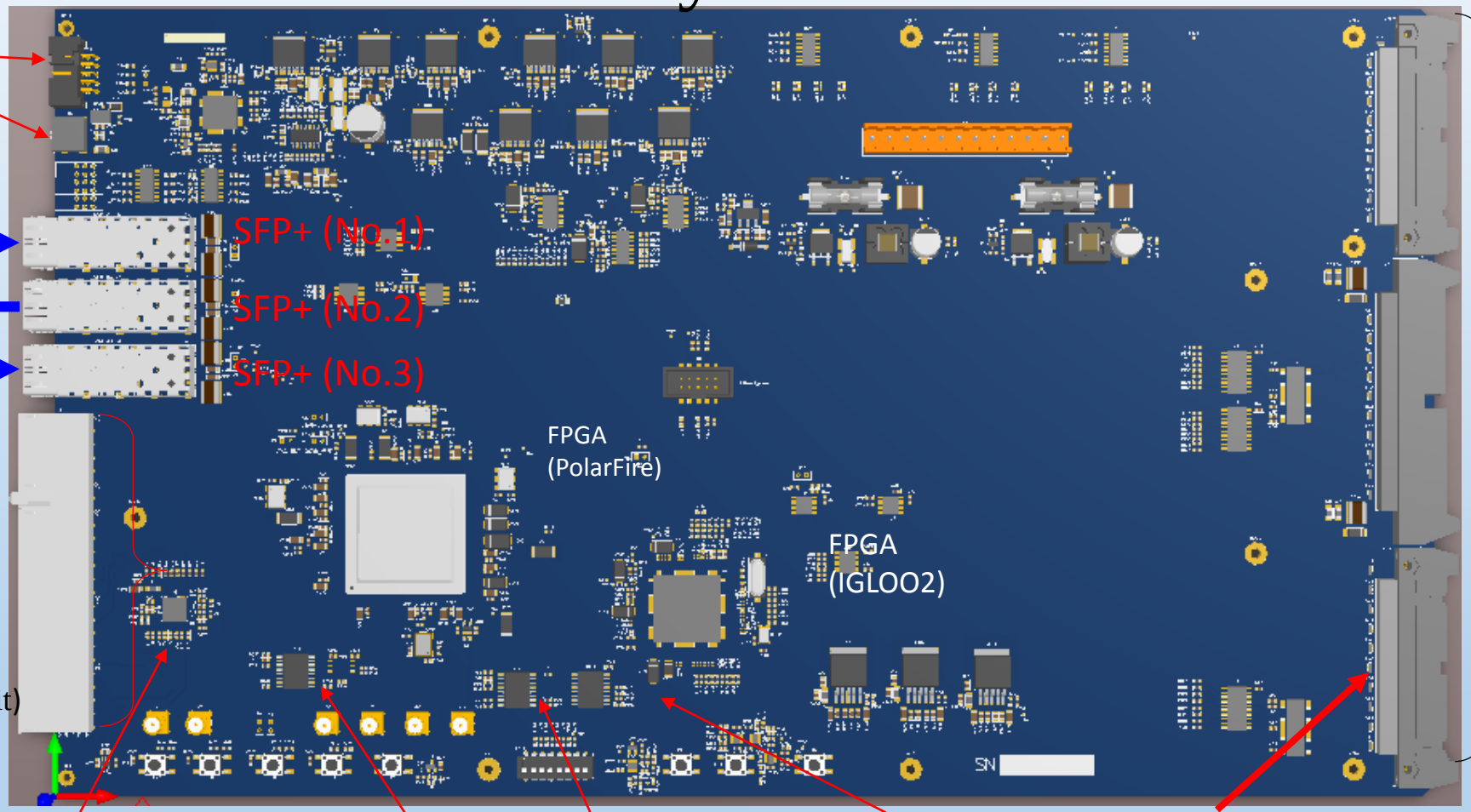
1376 Link Boards
in **108 Boxes**,
Steered by **216 Control Boards**

Resistive Plate Chambers
Up to 6 layers of detectors.
480 chambers in Barrel, **648** in Endcaps

New Link system Futures :

- High resolution Muon timing measurement with **High resolutions** TDC in steps of **1.5ns**
- High data rate output on optical Link at **10.24 Gbps**
- Data output inform of **Muon Clusterization**
- Communication with **off-detector electronic** based on the **GBT / LpGBT Protocol**
- Adjustable timing window for each channel (96 different timing windows), background and noise reduction
- **Flash Base FPGA**, Lower power consumption, Soft starting (Lower surge current), **Zero-SEU for configuration** memory, the SRAM memory protected by some hardware IP core
- Improved Control and Diagnostic communication techniques (GBT Link protocol), increase the Speed and Reliability, peer-peer Fiber optic connection for each Control board
- Remote Programming as well as local programming

New Link Board: 3D PCB
New Layout wrt TDR

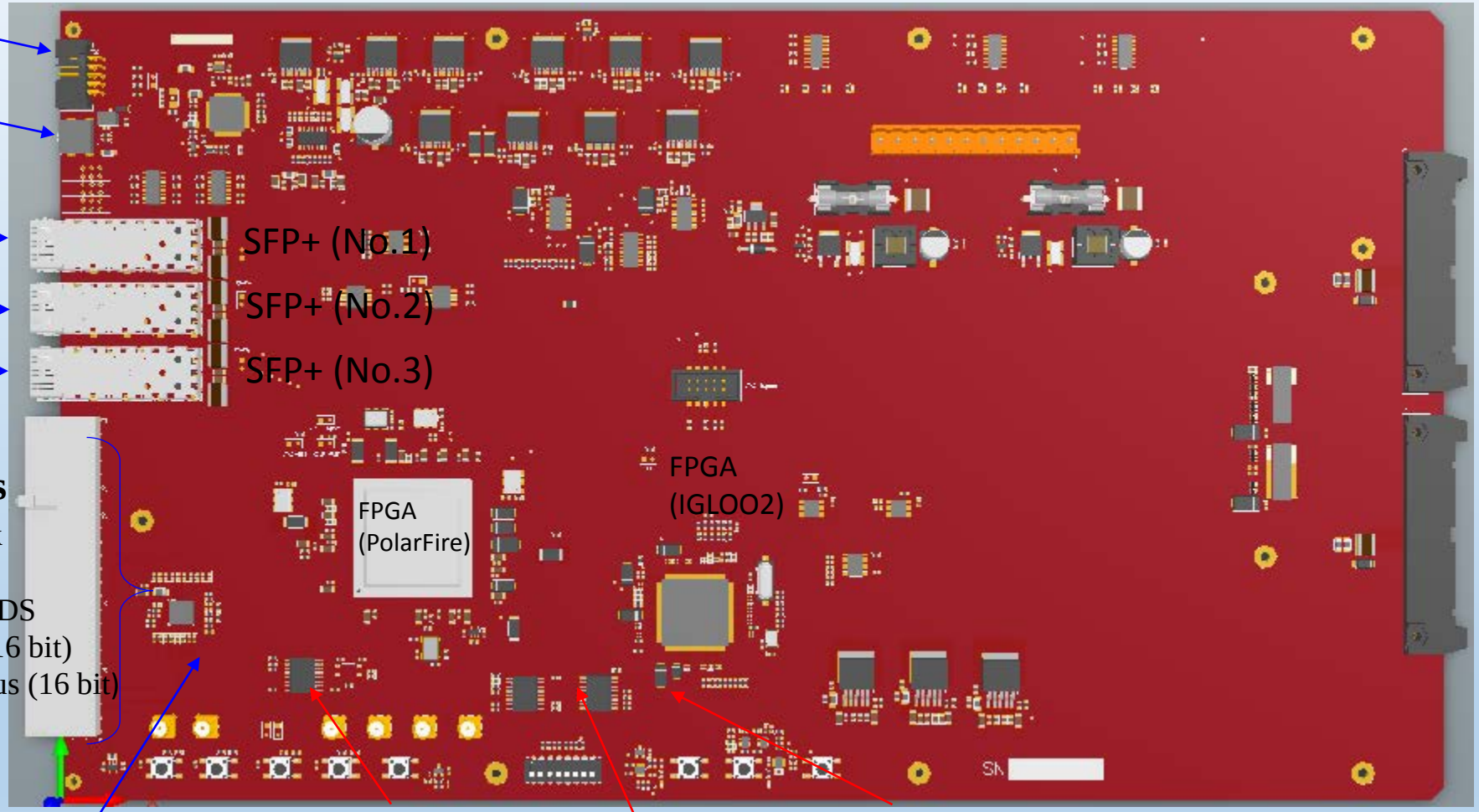


Local Bus

- TTC Clock
- 12 GTX
- 40 Pair LVDS
- Data bus (16 bit)
- Address Bus (16 bit)

- 96 LVDS INPUT RPC Input Signals
- 24 LVDS Output RPC Test Signals

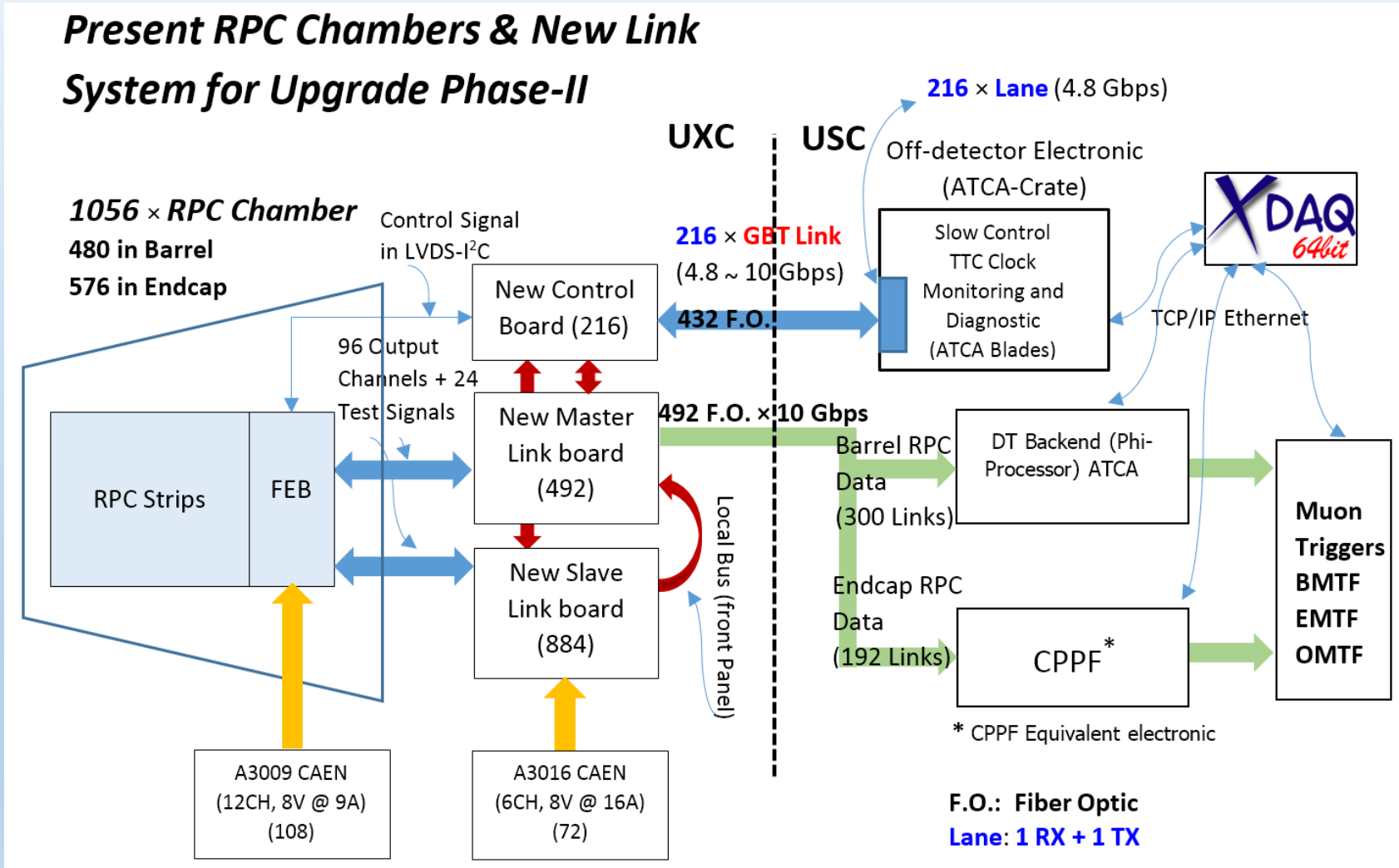
New Control Board: 3D PCB
New Layout wrt TDR



Local Bus

- TTC Clock
- 12 GTX
- 40 Pair LVDS
- Data bus (16 bit)
- Address Bus (16 bit)

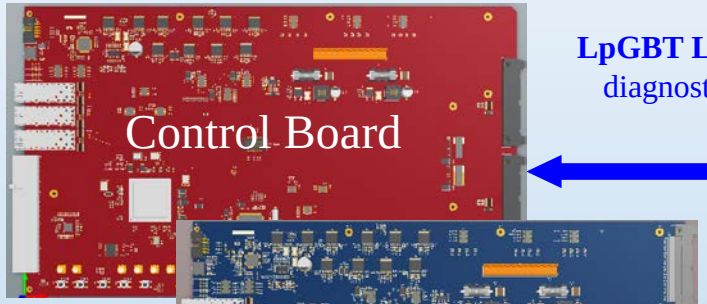
New Link System connection to the RPC Off-detector Electronic and Muon Trigger



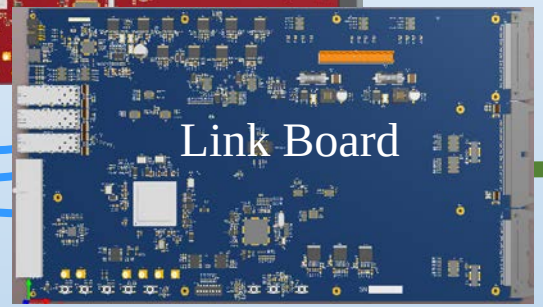
- In addition wrt to TDR, all the functionalities of present Slow controller are proposed to be handled with new RPC Off detector Back-end electronics
- The New Off-detector Back-End Electronics is under responsibility of China Institute of high energy physics (IHEP)

Link System Data Output to the Back-end

Upgrade Phase-II of New Link system



LpGBT Link Protocol (TTC, Control & diagnostic) @ 10.24 GHz / 2.56 GHz



LVDS cables

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in **108 Boxes**,
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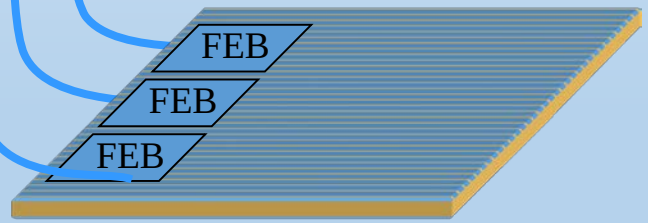
Data output Optical Link
LpGBT
90 m @ 10.24 GHz
492 fibers (before splitting)



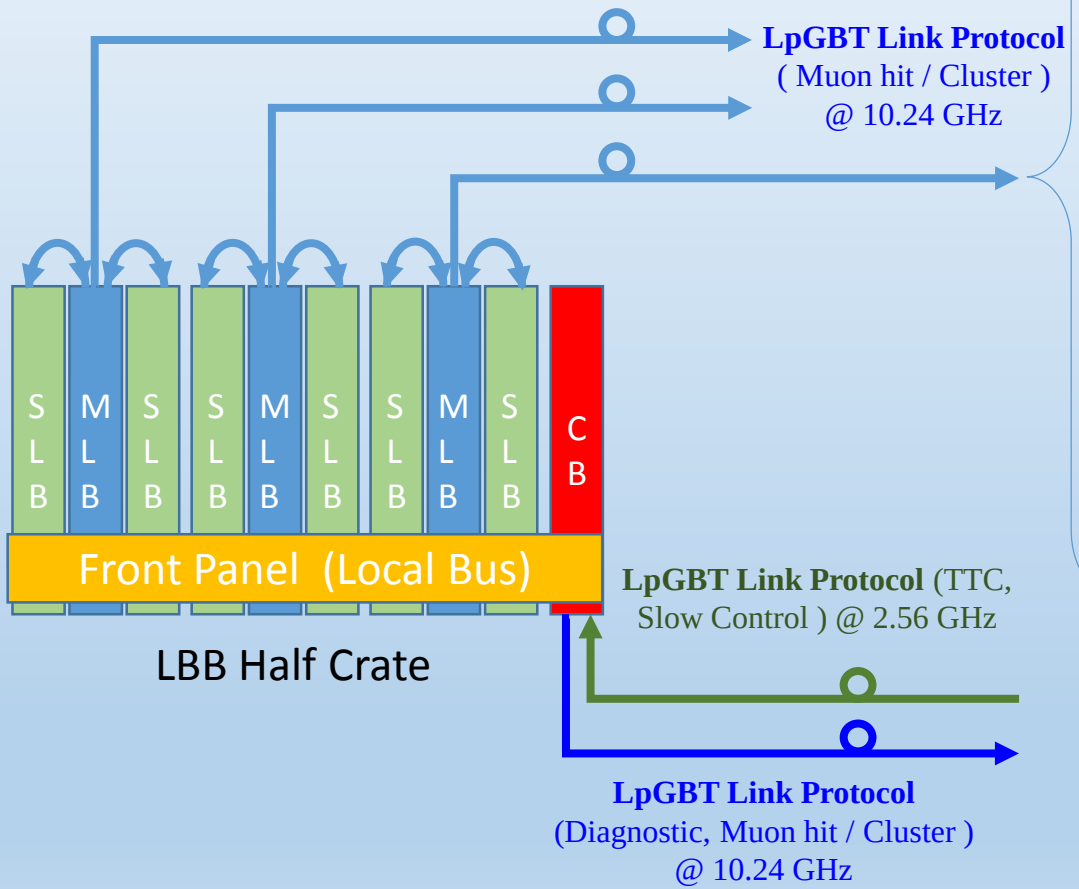
Resistive Plate Chambers
Up to 6 layers of detectors.
480 chambers in Barrel, **648** in Endcaps

New Link Board data output Futures

- Data Protocol : **LpGBT (FEC5)**
- Output data rate on optical Link: **10.24 Gbps**
- Data output inform of **Muon Clusters**
- Data is transmitted as a frame composed of:
  - Header
  - The data field
  - A forward error correction field: FEC5 / FEC12

	uplink	
	10.24 Gbps	
	FEC5	FEC12
Frame [bits]	256	
Header [bits]	4	
Data [bits]	232	204
FEC [bits]	20	48
Correction [bits]	10	24
Efficiency	91%	80%
Max Number of Clusters / BX	13	11

New Link system Data Frame format



			Cluster No. x					
5	Data frame format (bit)	Number of Clusters (1~13) (Maximum = 13)	Start of Cluster (1~96)	Cluster Width (8 strips)	Cluster sub-bx resolution(1~16)	LB Number	Partition Delay	EOD
6	211	4	7	3	4	2	2	1

8	Timing Signeture & Data alignment (BC0 , BCN) (bit)	
9	13	
10		Maximum Data Size (bit)
11	Total Bits	
12	224	232

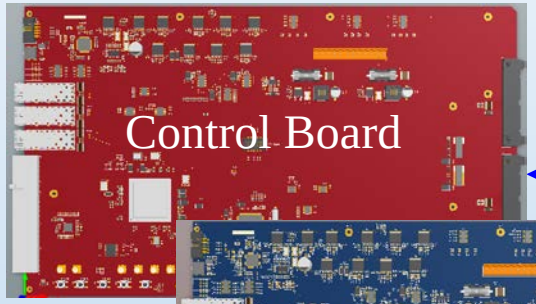
256 bit / BX

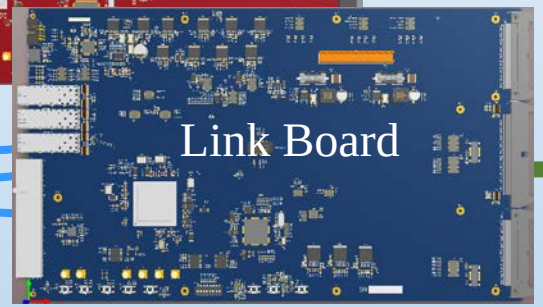
Header (4 bits)
(Delimits the frame boundaries)

Forward Error Correction (20 bits)
(Allows to correct transmission errors)

Link System Data Communication with RPC off-detector Back-end electronic

Upgrade Phase-II of New Link system





LpGBT Link Protocol (TTC, Control & diagnostic) @ 10.24 GHz (FEC5) / 2.56 GHz (FEC12)

LVDS cables

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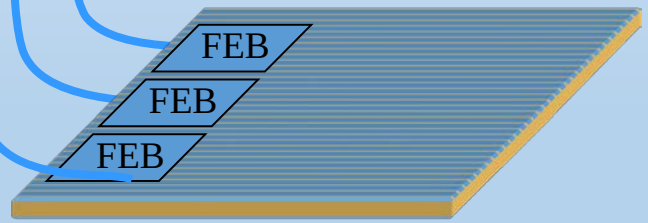


Resistive Plate Chambers
Up to 6 layers of detectors.
480 chambers in Barrel, **648** in Endcaps

New Control Board data in/output Futures :

- Data Protocol : **LpGBT**
- **Uplink** Data Rate : **10.24 Gbps (FEC5)**
- **Downlink** Data Rate **: 2.56 Gbps (FEC12)**
- Data output inform of **Muon Clusters**
- Data is transmitted as a frame composed of:
  - Header
  - The data field
  - A forward error correction field: FEC5 / FEC12

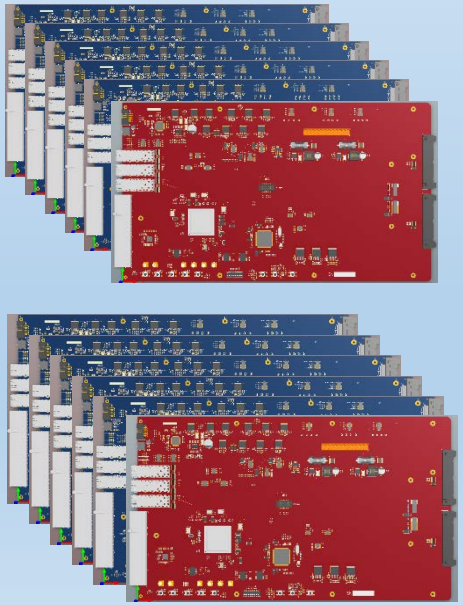
	Uplink		Downlink
	10.24 Gbps		2.56 Gbps
	FEC5	FEC12	FEC12
Frame [bits]	256		64
Header [bits]	2		4
Data [bits]	232	204	36
FEC [bits]	20	48	24
Correction [bits]	10	24	12
Efficiency	91%	80%	56%

Preparation for Primary and Advance tests
RPC off-detector Back-end Simulator

- Demonstration plan based on HTG-710 high performance Card.
  Most important Features :
  - Xilinx Virtex-7 V2000T, 585T, or X690T FPGA
  - x2 CXP Ports (120 Gig each) **-> 24 Full duplex 10G Links**
  - x8 PCI Express Gen2 /Gen 3 edge connectors
    - Gen 2: using FPGA hard-coded PCI Express Gen2 controller
    - Gen 3: using soft PCI Express Gen 3 IP core
- With each **HTG-710 card** we can handle **18 new Link boards** and **2 new control boards** simultaneously ; **one LBB**

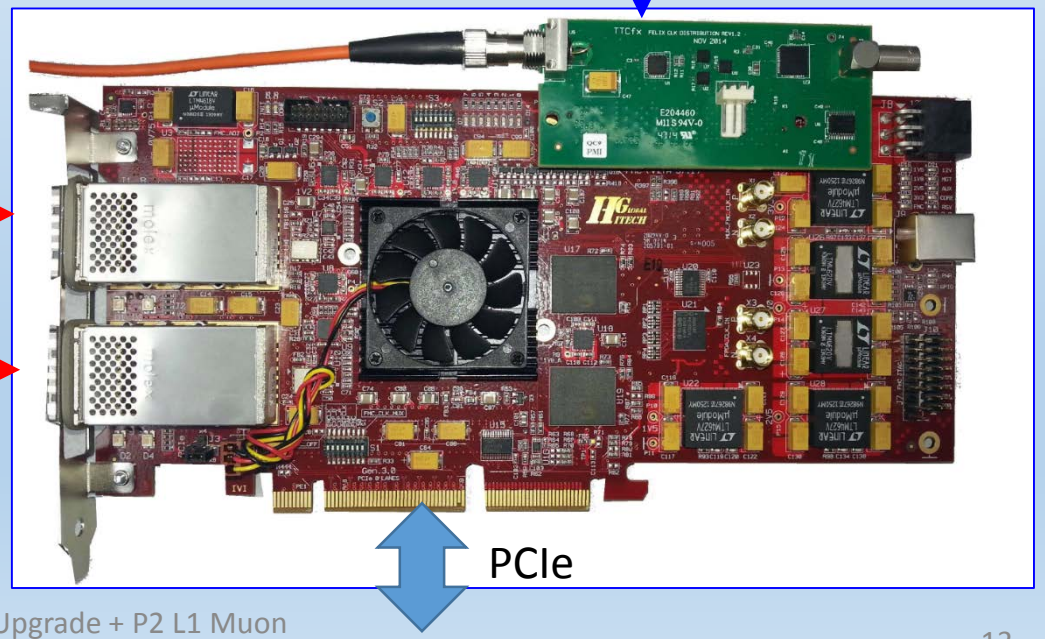
GBT-FPGA and ***Embedded Linux*** will be implemented into the HTG-710 FPGA

TTC Clock

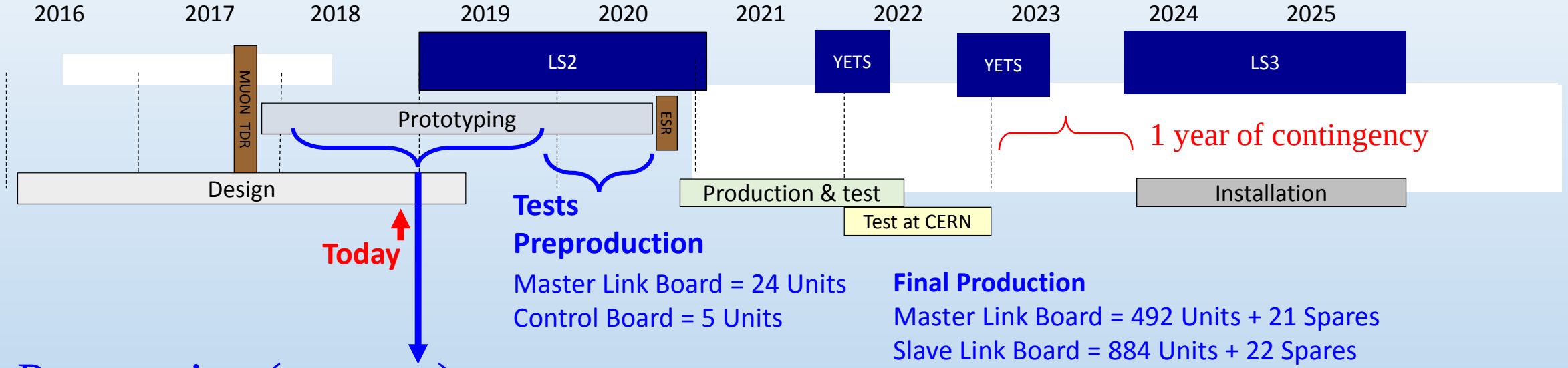


12 × SFP+ (10 Gbps)

12 × SFP+ (10 Gbps)

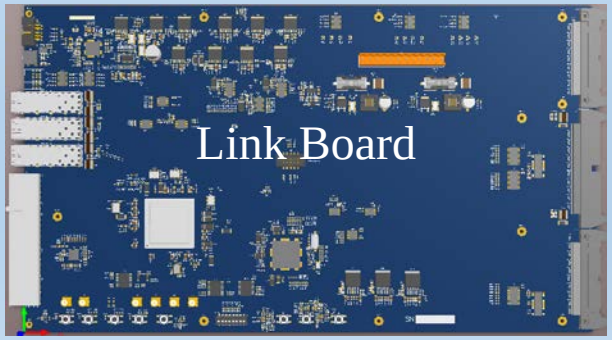


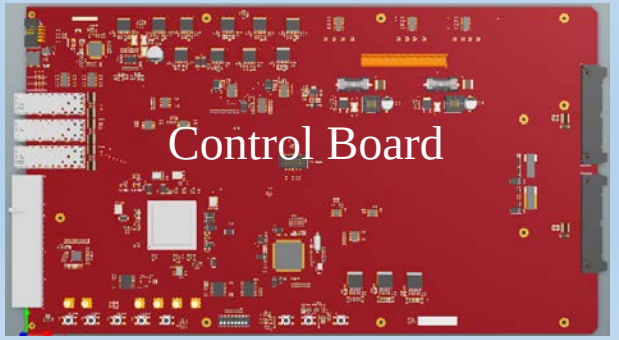
Link System Upgrade Phase-2 Timeline



Prototyping (2018-2019)

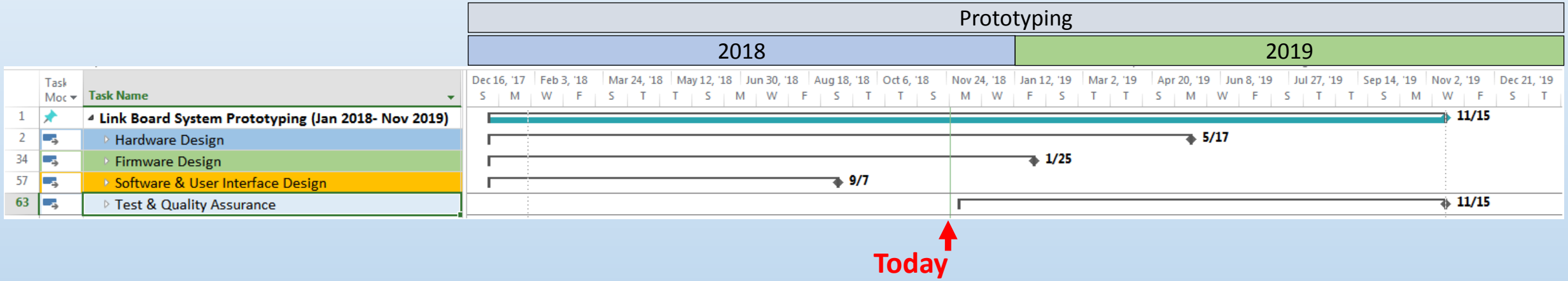
- PCB Layouts of **Link board** and **Control Board** have completed
- FPGA Firmware developing is in progress
  - Clusterization Algorithms
  - Implementing the LpGBTx IP core
  - High resolution TDC
  - System communication and Control
  - Remote Programming





LB Upgrade Timeline Prototyping Status (2018)

- Timeline of the Link System Prototyping

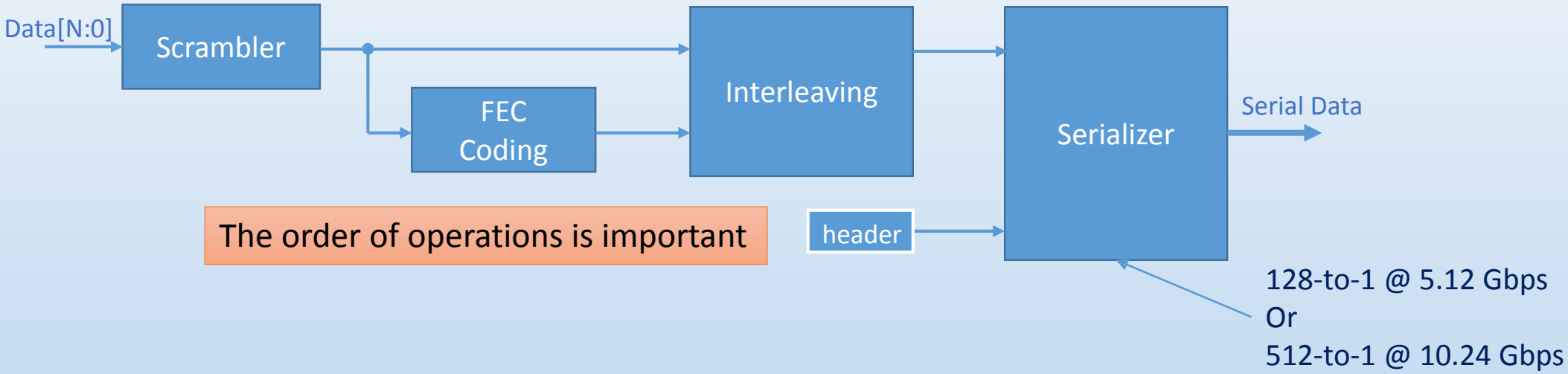


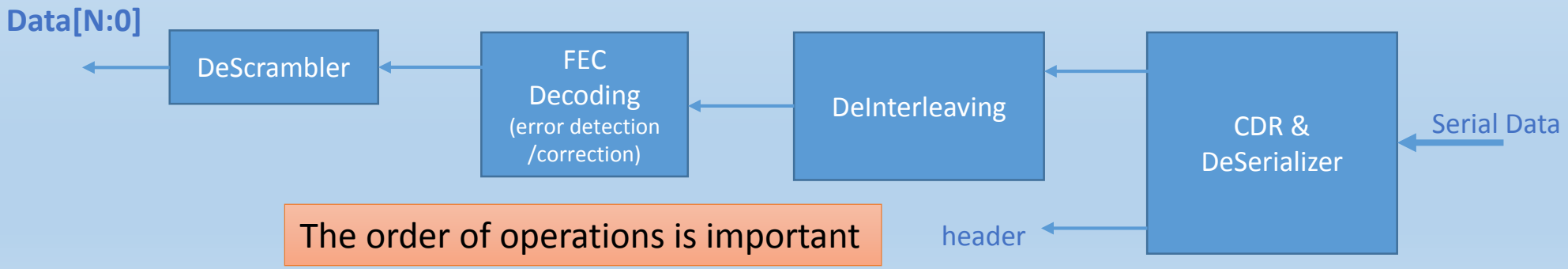
- Project Status (2018):
  - Hardware (PCB Layout) of Link board and Control boards has been completed
  - Signal Integrity (SI) and Power Integrity (PI) of LB/CB PCB Layout has been completed
  - Component procurement for more than 30 sets of LB and CBs, waiting for the delivery from Vendors (to middle of February/March of 2019)
  - Half parts of the Firmwares have designed and it will be continuous to end of 2019 (firmware modification)
  - GUI for primary tests has completed

Conclusion

- Present system will be work very well until LS3
- New Link system Will be installed in LS3 (2024-2025)
- High resolution timing measurement (Sub-BX) in order of 1.5ns
- Data protocol based on LpGBT, 256 bit/BX @ 10.24 GHz (FEC5)
- During Prototyping, Link system will be test with RPC off-detector Back-end Simulator (one LBB) and at least one RPC spare chamber in 904.
- Hardware design layout of LB and CB has done and we are in Procurement and component delivery phase
- Prototypes of LB and CB will be ready at the Q1 of 2019.

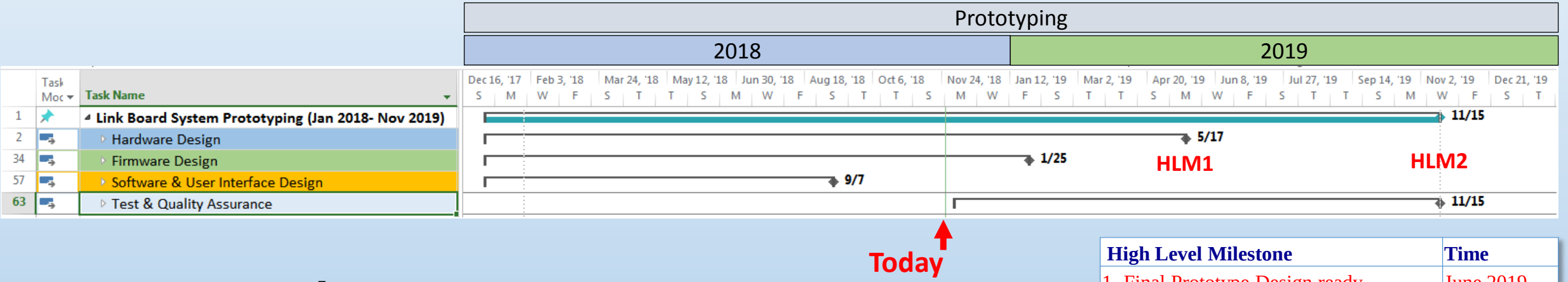
Uplink/Downlink data path





LB Upgrade Timeline
Prototyping on First Half of LS2 (2019)

- Timeline of the Link System Prototyping



- Project tasks on 2019:
  - Mounting components on the PCBs
  - Test and run some basic functions to find out behavior of Hardwares
  - Completing the firmwares and implementing firmwares on the LB/CB
  - Completing the firmware and softwares of the RPC Back-end simulator
  - System Primary Tests and validation Q3 and Q4 of 2019

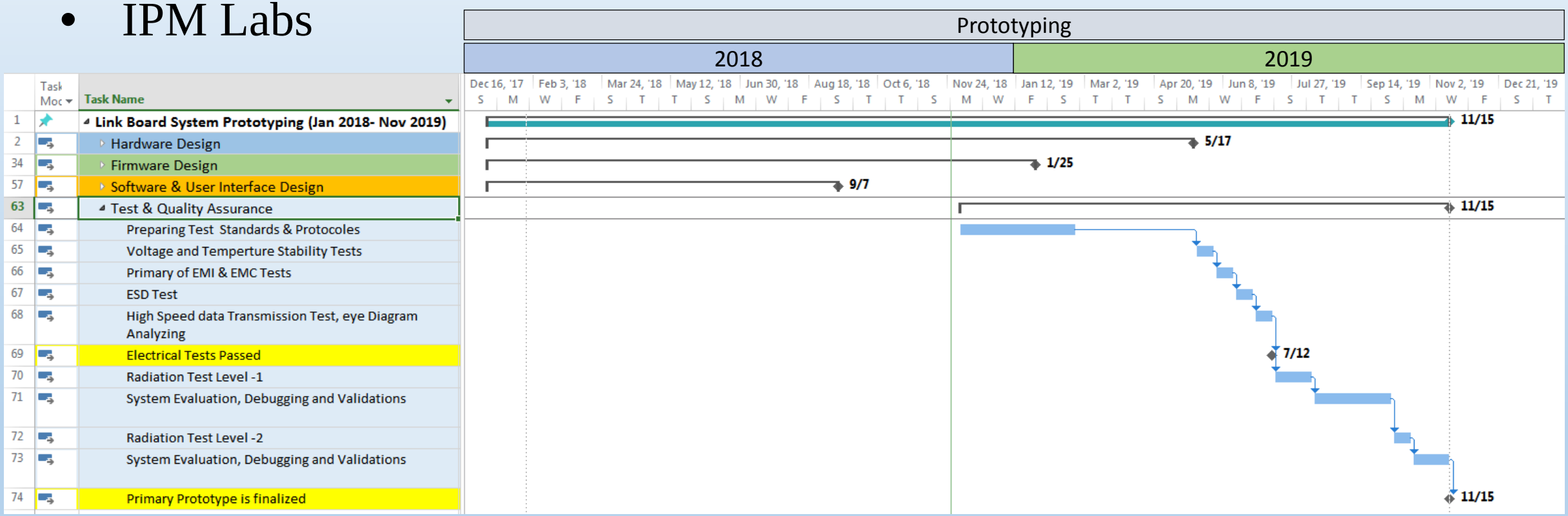
High Level Milestone	Time
1- Final Prototype Design ready	June 2019
2- Initial Validation of final prototype at production site	October 2019
3- Final Validation of final prototype design at CERN	September 2020
4- Prototype and documentation finalized	October 2020
5- Electronics System Review	October 2020
6- PCB fabricated and components received	April 2021
7- First half of the link boards and control boards assembled and tested	November 2021
8- Second half of the link boards and control boards assembled and tested	March 2022

LB Upgrade Timeline

System Primary Tests and validation

Q3 and Q4 of 2019

- Timeline of the Link System Prototyping Tests and Validation
- IPM Labs



- Link system validation for Preproduction

LB Upgrade Timeline
System Advance Tests and validation
2020

- Link system Preproduction will be done in Q1 of 2020
  - 25 Link boards
  - 5 Control Boards
  - Only final PCB Layout will be ordered
  - Components are ready for mounting
  - Burning tests and Quality control
- Preparation for advance tests in Q2 of 2020
  - Investigation of Link system performance via off-detector/back-end Simulator
- Advance tests in Cern on Q3 of 2020 (HLM3)
- Electronic system Review (HLM4,5)

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