Proposal for RPC Backend and Status

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Outline

• Requirement of P2 RPC Backend (BE) Electronics
• First CMS Prototype for RPC BE
• Further Development:
  – New Trigger Requirement
  – Meeting DTH
• iRPC solution case
• Summary
Requirement of P2 RPC Backend (BE)

• Functionalities
  – Fast Control
    • Interfacing to CMS DTH To get TTC/TCDS (Backplane)
    • Providing TTC to FE Electronics (GBT)
  – DAQ
    • Accepting DAQ from FE Electronics (GBT)
    • Sending data to Central DAQ via CMS DTH (Panel)
  – Slow Control
    • Interfacing to Slow Control (MCH/PC)
  – Trigger Layer1 Processor for Barrel and Endcap

• ATCA compliant module
First Prototype for RPC/CMS

• Complete Module
  – Carrier Board (new design for CMS, Full ATCA size)
    • To get TTC/TCDS via Backplane from DTH ( ~10Gbps)
    • Distributing TTC to AMCs (max 10Gbps)
    • Providing interconnection between AMCs (DAQ) (~ 10Gbps)
    • IPMC/MMC
  – AMC for Control/DAQ (present, double AMC)
    • GBT with FEE (4.8 Gbps) for iRPC
  – AMC for CPPF
  – RTM (backups)
General Purpose BE / ATCA Carrier Design

- **FPGA:** Ultrascale Kintex xcku060
- **RAM:** 16 GB DDR4 (8 chips)
- **MGTs:** 16.3 Gbps
  - 4 links to each AMC card (currently: 4 x600 Mbps LVDS)
  - 12 links to ATCA backplane
  - 1 link to RTM (10G Ethernet)
- **GbE switch:**
  - 4 xFPs/2CPPFs ,
  - 1 switch FPGA,
  - 1 uplink to ATCA Base Interface
  - 1 RTM RJ45
- **10 Gigabit Ethernet to RTM(SPF+)**
- **Configuration**
  - Programmable MGT clock
  - CPLD as JTAG hub
Backplane chains test 10 Gbps OK

◆ Backplane Communication
  ◆ 12 Backplane channel point-to-point connection between two blade,
  ◆ 10Gbps/ch for Backplane connector.
  ◆ 24 hours, No error on 12.5Gbps.
◆ Results: 10Gbps OK
AMC and RTM links tested 10Gbps OK

AMC MGT 10G

AMC MGT Pre-Cursor 12.5G

12 hours, No error on 10Gbps and 12.5Gbps.

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**R&D Status with RPC BE/Concentration**

- **ATCA:** 1 Carrier + 2 AMC Processor + 1 RTM
- **AMC Processor**
  - Data throughput
    - 3 MiniPoD, support 360Gb/s INPUT,
    - 2 MiniPoD, support 240Gb/s OUTPUT
  - XC7VX415T-2 (Virtex-7)
    - Core FPGA for data processing,
    - 48 channel GTH Transceivers,
    - Support up to 13.1 Gbps per channel.
  - XC7K70T-2 (Kintex-7)
    - Control FPGA,
    - Configure and Control CPPF.
  - AT32UC3A1512 (Atmel)
    - MMC, Module Management Controller.
- **Carrier**
  - Ultrascale Kintex xcku060
  - Designed for RPC backend
  - Communication with CMS DTH
  - Link speed 12-16.3Gbps
Common ATCA board development

- Carrier modification to match CMS DTH
  - TTC
  - Slow control
  - RPC DAQ
- AMC processor for iRPC and RPC control
- AMC processor for concentration of RPC/CSC at least, better also iRPC and GEM inputs before Endcap tracker finding
  - 10 Gbps inputs
  - 26 Gbps output
Characteristic of this module

- Similar Module designed for PANDA Project
  - DOI: 10.1109/RTC.2010.5750331, arXiv:1806.09128v2
- Similar Module taking data at Belle II/PXD
  - https://indico.mitp.uni-mainz.de/event/119/session/1/contribution/58/material/slides/0.pdf
  - https://indico.desy.de/indico/event/7866/session/3/contribution/55/material/slides/0.pdf
- Modularity
  - Carrier Board will match with DTH for TTC
  - AMC board for Control/DAQ
  - AMC board for trigger Concentration/layer1 processing/Fan-out
- Inter-changeability
  - AMC board can work both as ATCA/daughter or in uTCA crate (see later for iRPC)
Further Development

• Improve to Implementation of iRPC control and DAQ
• Standardized Carrier for CMS DTH
• Control/DAQ card improve for DTH
• Discuss/design for Endcap RPC Layer1 concentration with CSC, and/or more if possible
• Collaboration with DT colleagues for application if possible
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1. Prototype+Joint Test electronically
2. Integration MTCA system
3. Migration to ATCA if necessary and possible
RE3.1/4.1 Backend Electronics (TDAQ+TTC/SC)

Data

GBT

EMTF

CPM – Central Partition Manager
LPM – Local Partition Manager
PI – Partition Interface
Summary

• An RPC Backend Electronics Solution is given
• A prototype for CMS is presented with similar application in PANDA and Belle II experiments
• iRPC solution is briefly described
• Characteristic of modularity of this ATCA board make it a multi-purpose module for iRPC Control, iRPC DAQ, iRPC trigger, RPC Backend, Trigger layer1 concentration/processing,... hoping more applications
Backups
Prototype Module at IHEP

- Similar modules now taking data at Belle II
- No DTH function yet!
RE3.1/4.1 Off-Detector/Backend Electronics (TTC/SC + TDAQ)

- First Hardware (ofde) Prototype ready
  - uTCA Compatible
  - Double AMC Card
  - V7 FPGA for processing
  - K7 FPGA for Control
Status of Firmware Development

• Demo/test system at TriggerLab/IHEP ready
  – GBT transmission and receiving done
  – FEE Code expected from Lyon friend in November, will confirm again.
Demo system with Data flow

- The system works
- Should be checked with Lyon code
- Should be joint tested with Lyon FEE

The diagram shows the data flow between the PC Server, AMC13, MCH, and the ILA capture boards. There are two fibers (3m each) connecting the boards. The system is divided into the Request Board and Reply Board, with data capture and bitfile download processes indicated.

Local Mini-system diagram

2 Fibers (3m each)

PC Server

Fiber Loopback
IP Bus

MCH

AMC13

ILA capture

ILA capture

Reply Board

Request Board

MicroTCA crate
GBT BANK Implementation in test board

- GBT-FPGA is implemented in CPPF step by step, firstly is the protocol layer (also known as GBT BANK) as shown following:
  - The scrambler/descrambler, RS encoder/decoder, SerDes which are the main functions in GBT-FPGA are implemented in this level.
- This test is done in one CPPF board, one GTH channel at 4.8Gbps, in fiber (3m) loopback mode.
- Customized 4bits (slow control) + 80bits (user data) = 84bits fake data to verify the functionality of the GBT BANK after migrated to CPPF.
- The test results show that GBT BANK performs well in CPPF.
  - Data captured in ILA shows the RX data is as the same sequence as the TX data, latency is not measured.

84bits TX data
84bits RX data

![GBT BANK Implementation Diagram](image)
RPC Upgrade Schedule/New DAQ Backend

New Link System/New RPC DAQ

1. ATCA Prototype
2. ATCA/TTC-DAQ protoT
3. Final ATCA
4. Production
5. Integration

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RE3.1/4.1 BE Electronics
LHC/CMS TTC System

Slides from J. Troska M. Hansen, J. Hegeman, F. Meijers, P. Vichoudis CERN-PH-ESE & CERN-PH-CMD
CMS TTC structure

- Overall system can have
  - Up to 12x LPMs
  - Up to 8x PIs per LPM
  - Total 96 partitions
- It is possible to add a redundant PM crate
  - For debugging, (sub-) system commissioning

AMC13 – CMS μTCA readout board
FMM – Fast Merging Module

CPM – Central Partition Manager
LPM – Local Partition Manager
PI – Partition Interface
TTC – Timing, Trigger & Control
TTCrx – TTC Receiver ASIC
TTS – Trigger Throttling System