Validation and Reliability Tests for the new VFC-HD

V. Schramm

on behalf of

S. Eitelbuß, M. Gonzalez Berges, J. O. Robinson, M. Saccani, M. A.Stachon,
W. Viganò, C. Zamantzas and all other involved

BI Seminar 11.01.2019

Volker Schramm
BE-BI-BL
volker.schramm@cern.ch

Agenda

- Introduction
- Methodology & Objective
- Test Setup
- Test Results
  - Validation Tests
  - Burn-In (ongoing)
  - Run-In (ongoing)
- Summary & Outlook

Introduction

The **VFC-HD** board is a new multi-purpose VME carrier board developed in BI

Main challenges:

- Complexity
  - 1200 mounted components, 12 layers
  - VME, *Arria V* FPGA, DDR3, DCDC, FMC, SFPs, …
- Serves a variety of different users & applications
- Dependability and performance requirements
- Production of 1200 units

➔ To ensure a good and dependable performance upon installation, **validation** and **reliability testing** is put in place.

Methodology & Objective

Design

- Specifications ✓
- Predecessor analysis ✓
- MTTF prediction ✓
- Failure Modes, Effects & Criticality Analysis ✓
- Design Review ✓

Production (& Tests)

Reception Tests

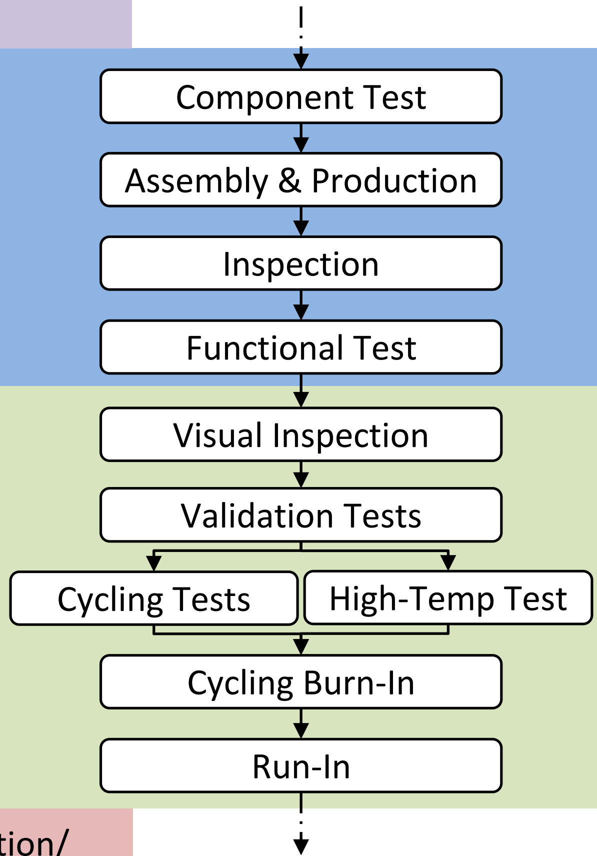
Installation/ Commissioning

Operation

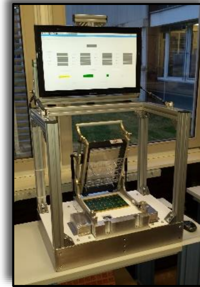
Dependability methodology applied upon planning and design through production, testing and installation to system operation

- Addressing dependability during the full life cycle
- Validation (functional, environmental, quality)
- Reliability assessment & improvement
- Risk reduction & risk assessment
- Mitigation of (late) design changes
- Methodological approach (re-useable; universal; evolving)

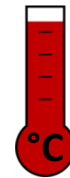
Methodology & Objective

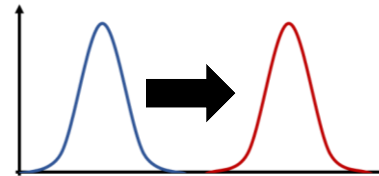


Various tests & checks implemented at the manufacturer:



Test strategy after reception at CERN:





Agenda

- Introduction
- Methodology & Objective
- Test Setup
- Test Results
  - Validation Tests
  - Burn-In (ongoing)
  - Run-In (ongoing)
- Summary & Outlook

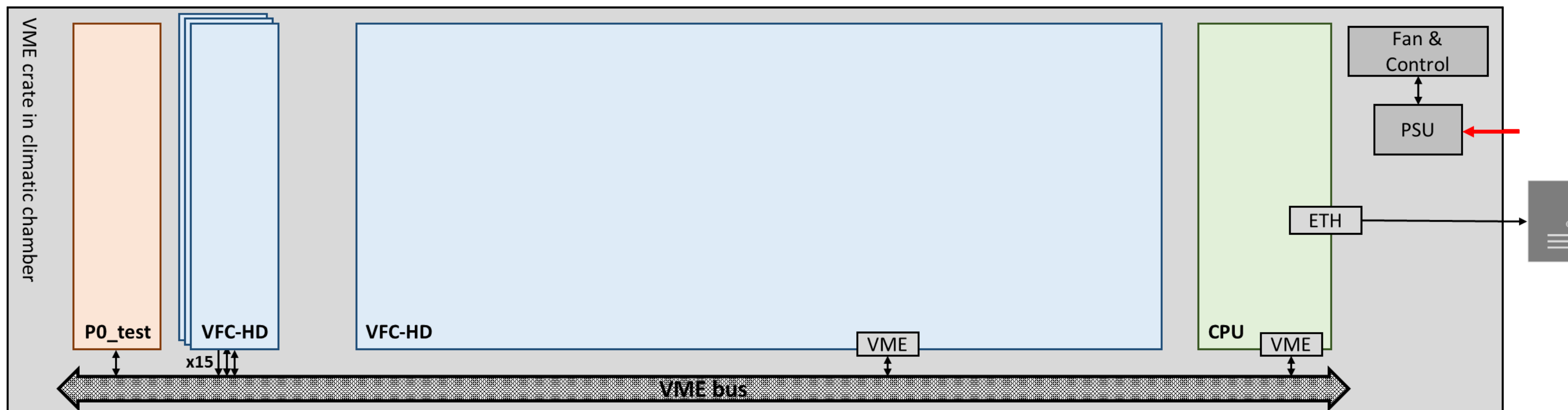
Test Setup

Hardware

Visual Inspection:
- Digital microscope *Tagarno FHD UNO* (92x magnification)

Validation & Burn-In:
- Climatic chamber *Binder MKF240* for temperature and humidity
- Other procurements & modifications: Crate, FMC/SFP loopback modules, custom boards, cables, fibres, …

Run-In:
- 8 VME crates in 2 racks + PSUs, CPUs, cabling, …



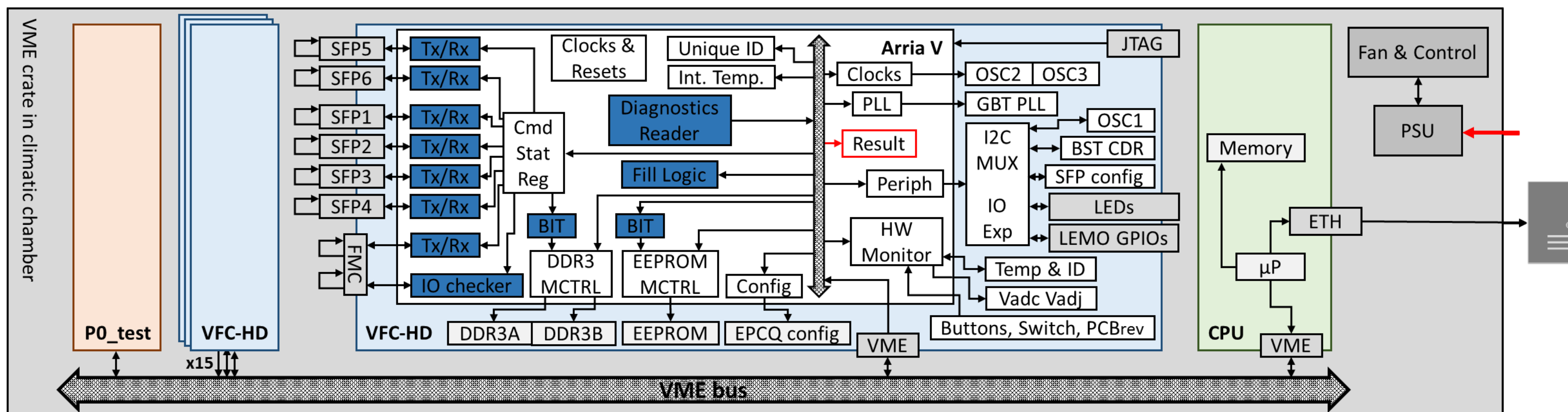
Test Setup

Firmware

Test firmware constantly checks all board functionalities in parallel & saves the results:

- Sends/writes & reads back
- Checks various values: f_{clocks}, temperatures, voltages, …
- Loopback for SFPs, FMCs & LEMOs
- FPGA self checking

→ Results register is read by the CPU card



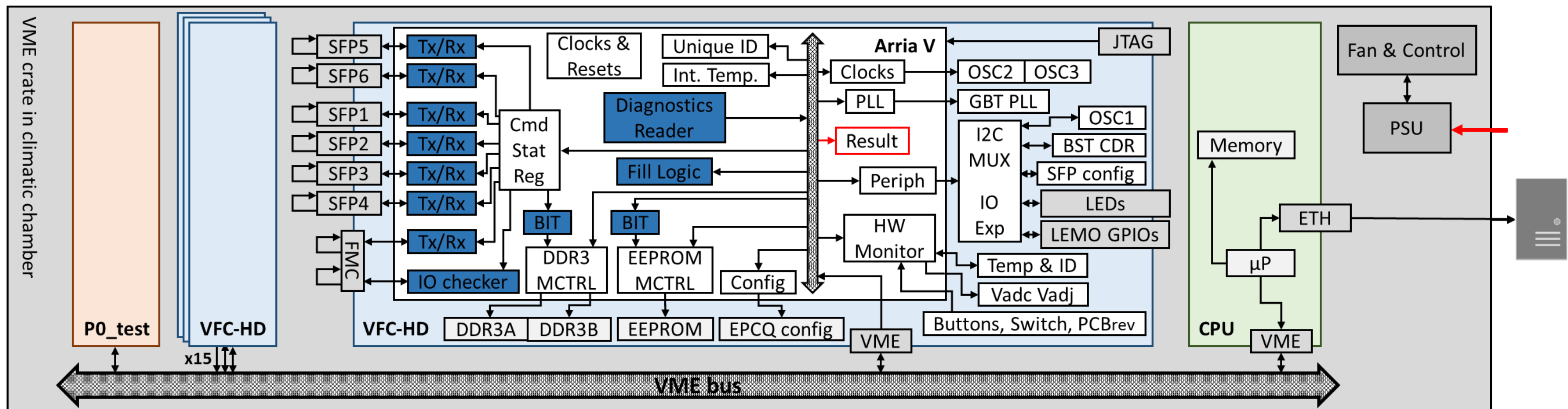
Test Setup

Software

CPU card communicates the test results to the database:

- Cyclic results reading depending on selected test
- Data logged on NXCALS with Spark for queries
- Asset management integrated to register and follow up devices

→ Expert application provides a GUI



Test Setup

Expert application

Global operational tab

16x DUTs

Graph configuration

Bar code reading

Status LEDs

Test selection

cfv-6546-blmrun1

File Help

Operational | Slot: 04 | Slot: 05 | Slot: 06 | Slot: 07 | Slot: 08 | Slot: 09 | Slot: 10 | Slot: 11 | Slot: 13 | Slot: 14 | Slot: 15 | Slot: 16 | Slot: 17 | Slot: 18 | Slot: 19 | Slot: 20 | Global configure | Bar Codes

Test: RunIn

Slot	BarCode	BST	ETH	APP1	APP2	APP3	APP4	FMC	DDR3A	DDR3B	EEPROM	FPGA	FLASH	CLOCKS	VADC	P0	MISC	CRC	BitTime	RealTime	BitRdNb	Status	Command
04	10082	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
05	10146	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
06	10081	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
07	10001	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
08	10142	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
09	10159	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
10	10057	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
11	10147	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
13	10026	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
14	10108	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
15	10041	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
16	10052	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
17	10153	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
18	10021	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
19	10109	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop
20	10075	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	■	17:53:33	66717	2148	ACTIVE	Start Stop

Start Test | StopTest | Start Publication | Stop Publication | Export

<none>

Many thanks to:
M. Gonzalez Berges, J. O. Robinson & M. A. Stachon

Test Setup

Expert application

Status LEDs

Asset creation

Custom Graph

File Help

Operational Slot: 04 Slot: 05 Slot: 06 Slot: 07 Slot: 08 Slot: 09 Slot: 10 Slot: 11 Slot: 13 Slot: 14 Slot: 15 Slot: 16 Slot: 17 Slot: 18 Slot: 19 Slot: 20 Global configure Bar Codes

Functional Graphs DebugSys DebugAppBitMsg AssetManager

Test Active: Errors:

BurnIn

Fmcl2c_ErrorCounter — Ddr3B_ErrorCounter — Eeprom_ErrorCounter — ArriaVInternalTemperature_Temperature — BstCdr_ErrorCounter — Button_ErrorCounter — TempAndIdSensor_Temperature

BitReadNb

[Nov 14, 2018 4:57:25 PM] : BurnIn graph displayed ...

Many thanks to:
M. Gonzalez Berges, J. O. Robinson & M. A. Stachon

Agenda

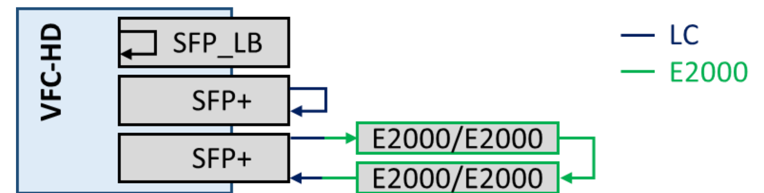
- Introduction
- Methodology & Objective
- Test Setup
- Test Results
  - Validation Tests
  - Burn-In (ongoing)
  - Run-In (ongoing)
- Summary & Outlook

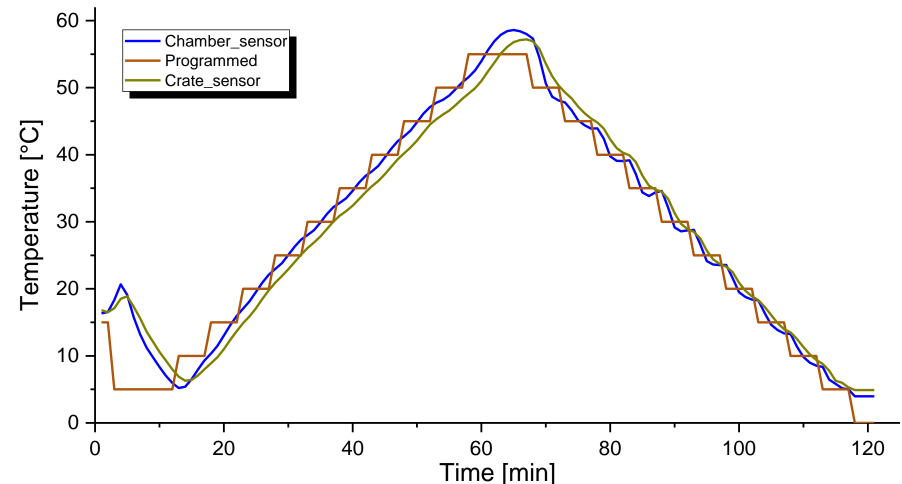
Validation Tests

1) Temperature/Humidity Cycling:

Functional & environmental validation + production approval

- Sample size: 2x pre-series
- Tests between 5-55°C & 10-90% RH
- Various SFP transceiver (*FT3A05D*) + fibre configurations
- Cycle tests in pyramid-shape or at constant conditions
- In total 11 tests performed





Validation Tests

1) Temperature/Humidity Cycling:

#1,2: Validation at temperature limits (low RH)

- No errors with SFP loopbacks

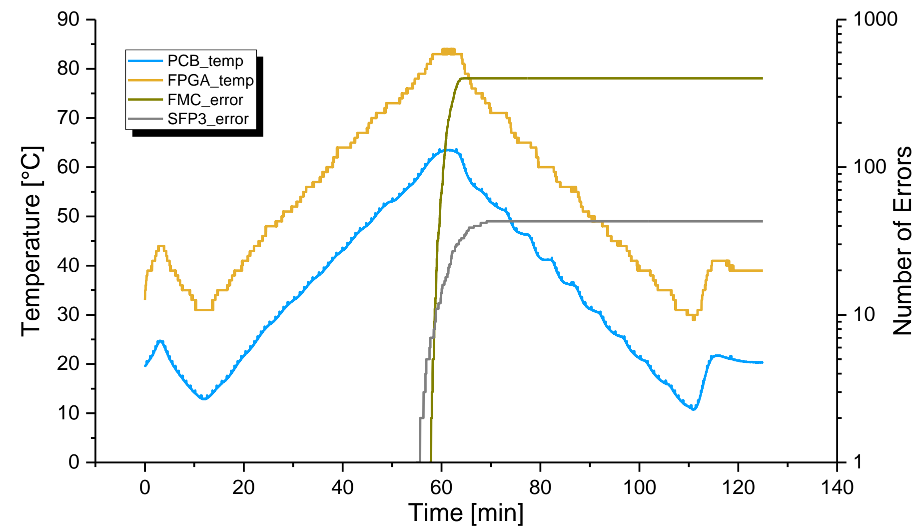
#3: Validation at 80% RH (25°C)

- No errors with SFP+ transceivers with fibre loopback (LC)

#4,5: 2h temperature cycling at 50/70% RH

- FMC loopback & SFP+ errors ≥50°C

#	T-range [°C]	RH-range [%]	Board A	Board B	Error A	Error B
1	5	<35	LB	LB	N	N
2	55	<50	LB	LB	N	N
3	25	80	LC	LB	N	N
4	5-55	50	LC	LB	Y	N
5	5-55	70	LB	LC	N	Y
6	35-55	50	LB	LC	N	Y
7	35-55	50	Mix	LB	Y	N
8	35-55	50	Mix	LC	Y	Y
9	30	50-90	Mix	LC	N	N
10	30	80	Mix	LC	N	N
11	40	80	Mix	LC	Y	Y



Validation Tests

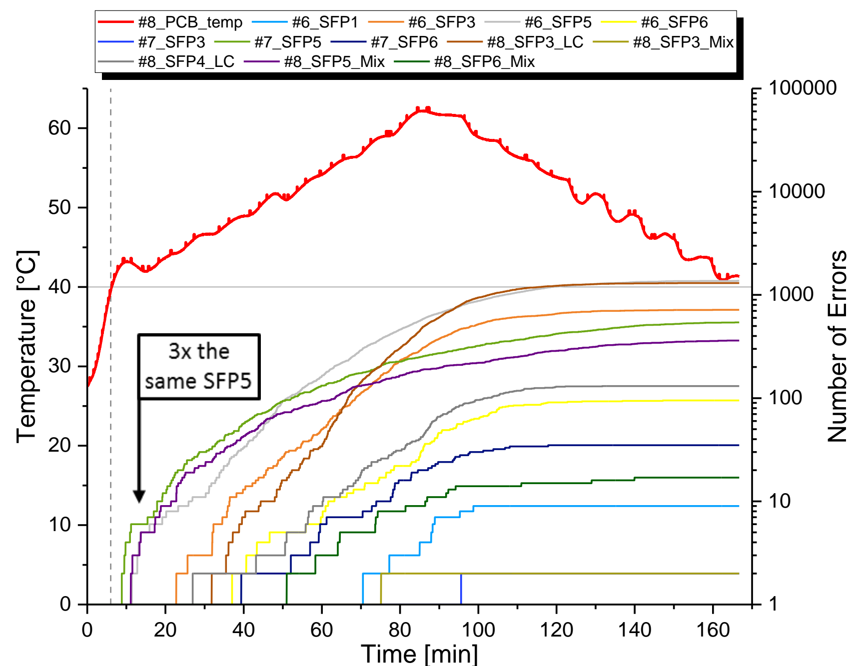
1) Temperature/Humidity Cycling:

#6-8: Further temperature cycling at smaller steps with different fibre setups

- Several SFP+ errors ≥ 40°C
- Wide spread of SFP+ quality
- Error rate ~ temperature

#	T-range [°C]	RH-range [%]	Board A	Board B	Error A	Error B
1	5	<35	LB	LB	N	N
2	55	<50	LB	LB	N	N
3	25	80	LC	LB	N	N
4	5-55	50	LC	LB	Y	N
5	5-55	70	LB	LC	N	Y
6	35-55	50	LB	LC	N	Y
7	35-55	50	Mix	LB	Y	N
8	35-55	50	Mix	LC	Y	Y
9	30	50-90	Mix	LC	N	N
10	30	80	Mix	LC	N	N
11	40	80	Mix	LC	Y	Y

#	T_{min} [°C]	SFP slot 1	SFP slot 2	SFP slot 3	SFP slot 4	SFP slot 5	SFP slot 6
4	57/54			40			
5	53/45	3		200			30
6	46/45	8		700		1300	90
7	44/**40**					500	30
8^{Mix}	42/**40**			1		350	16
8^{LC}	46/45			1300	130		



Validation Tests

1) <u>Temperature/Humidity Cycling:</u>

#9-11: Cycling and constant humidity tests

- Limitations when cycling with crate inside the chamber
- Not possible to control humidity reduction
- Validation for 80% RH at 30°C ✓
- Errors at 80% RH and 40°C X

#	T-range [°C]	RH-range [%]	Board A	Board B	Error A	Error B
1	5	<35	LB	LB	N	N
2	55	<50	LB	LB	N	N
3	25	80	LC	LB	N	N
4	5-55	50	LC	LB	Y	N
5	5-55	70	LB	LC	N	Y
6	35-55	50	LB	LC	N	Y
7	35-55	50	Mix	LB	Y	N
8	35-55	50	Mix	LC	Y	Y
9	30	50-90	Mix	LC	N	N
10	30	80	Mix	LC	N	N
11	40	80	Mix	LC	Y	Y

T_{max} (≤ 80% RH) = 30°C
T_{max} (≤ 50% RH) = 40°C

Validation summary:

- No VFC-HD board failures
- FMC errors most likely a combined effect of temperature & firmware → solved with new FW
- Further investigation for SFP+ errors above 40°C needed (possible RX saturation due to short fibre length)

Validation Tests

2) <u>High Temperature:</u>

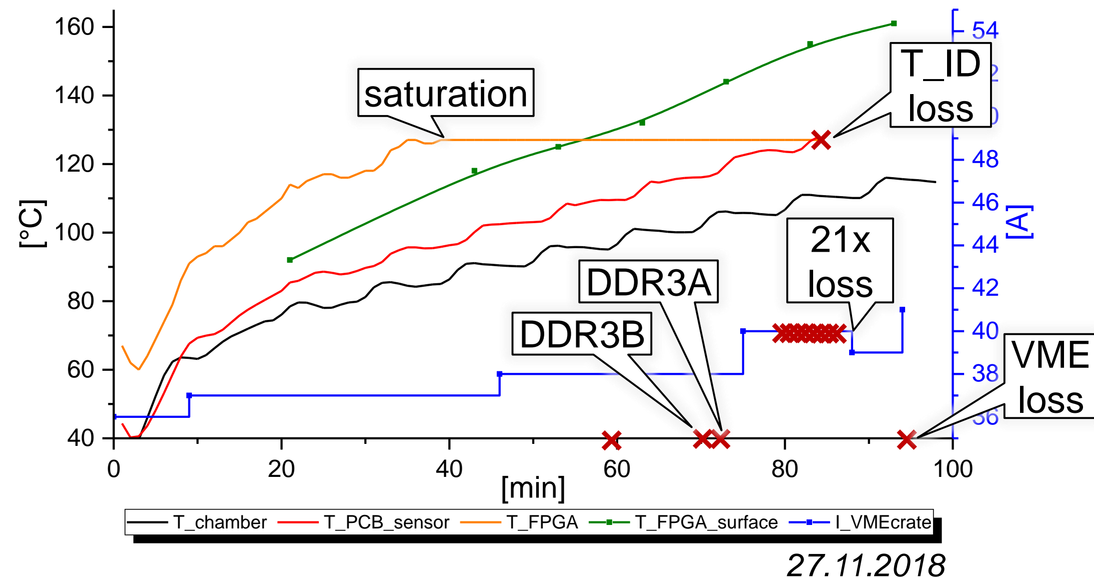
Trigger possible early failure mechanisms + production feedback

- 4 tested boards:

  (SFP + FMC loopbacks)

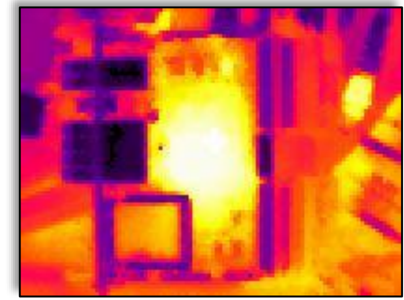
Date	Production batch	$T_{max_chamber}$ [°C]
26.07.2018	Pre-series	70
26.07.2018	Pre-series	70
31.08.2018	Version 2	100
27.11.2018	1st production batch	115

- Error-free communication until 95°C
- VME communication loss at 115°C → Test terminated
- Crate current consumption increased by **5A**
- $T_{max_FPGA_surface}$ = 161°C
- $T_{max_PCBsensor}$ = 128°C (in error)



Validation Tests

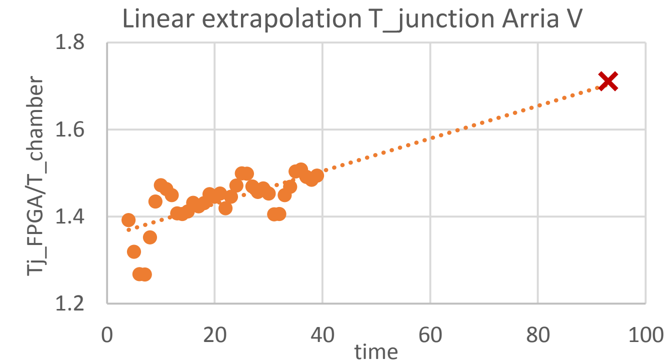
2) High Temperature:



- Linear extrapolation: $T_{j_max_FPGA}$ = **196°C**

  Datasheet: T_{j_max} = 125°C

  $T_{j_max_recommended}$ = 85°C



- After cooling down full recovery of all functions

27.11.2018

Tests summary:

- Reliable board operation up to 95°C
- No hardware failures up to 115°C → Successful ✓

➔ **Robust design & production**

Agenda

- Introduction
- Methodology & Objective
- Test Setup
- Test Results
  - Validation Tests
  - Burn-In (ongoing)
  - Run-In (ongoing)
- Summary & Outlook

100°C: Raising tension with raising temperature in front of the climatic chamber ☺

Screening & Reliability

<u>Reliability engineering basics:</u>

Reliability: $$R(t) = 1 - F(t) = \frac{f(t)}{\lambda(t)}$$

Failure Rate: $$\lambda(t) = \frac{No.of\ failures}{\sum t_{Device}} = \frac{f(t)}{R(t)}$$

Constant failure rate for electronics during useful life (exponential distribution): $$R(t) = e^{-\lambda t}$$

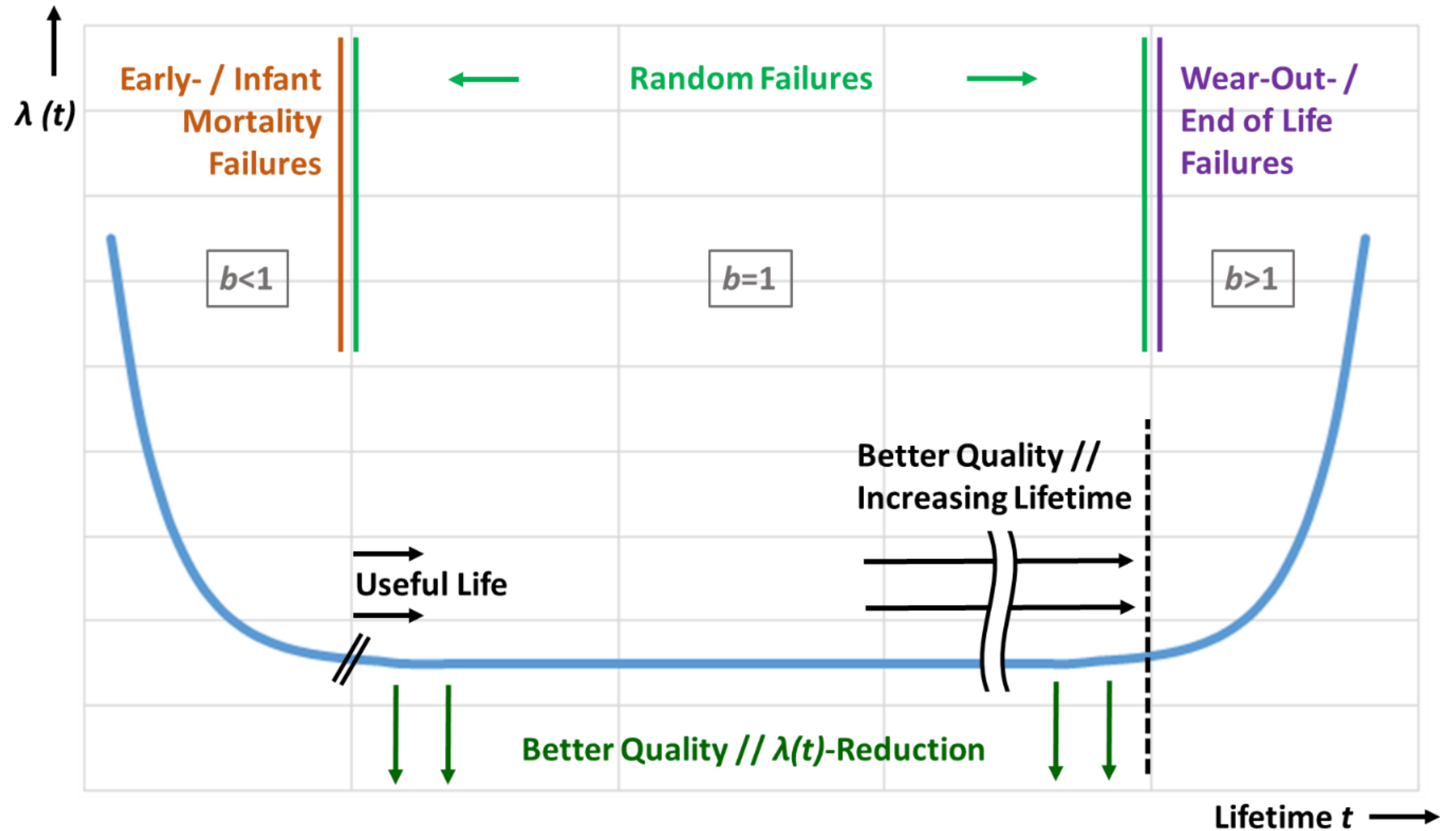
Mean Time To Failure: $$MTTF = \frac{1}{\lambda}$$

Mean Time To Failure for Chi-Square distribution confidence level: $$MTTF_{CL} = \frac{2 * \sum t_{Device}}{\chi^2[CL; 2(r+1)]}$$

F(t)	Failure probability [%]
f(t)	Failure density function
T	Characteristic Lifetime
CL	Confidence level [%]
r	Number of failures

Screening & Reliability

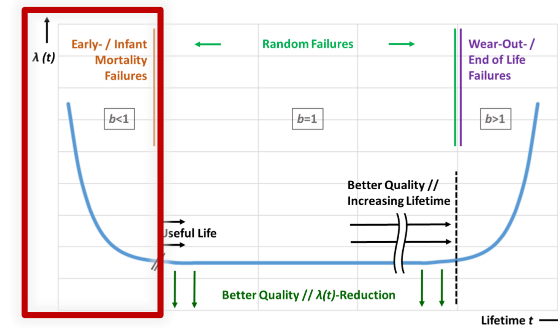
The bathtub curve:



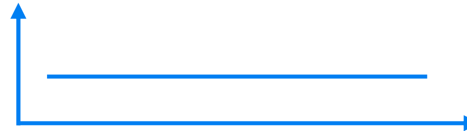
Weibull parameter b:

$$R(t) = e^{-\left(\frac{t}{T}\right)^b}$$

Screening & Reliability



- Burn-In and Run-In to screen for early life failures and to assess the (minimum) reliability
- Strategy comprises two steps:
  1) Temperature cycling to raise stress level
  2) Constant conditions to accumulate time & gain confidence

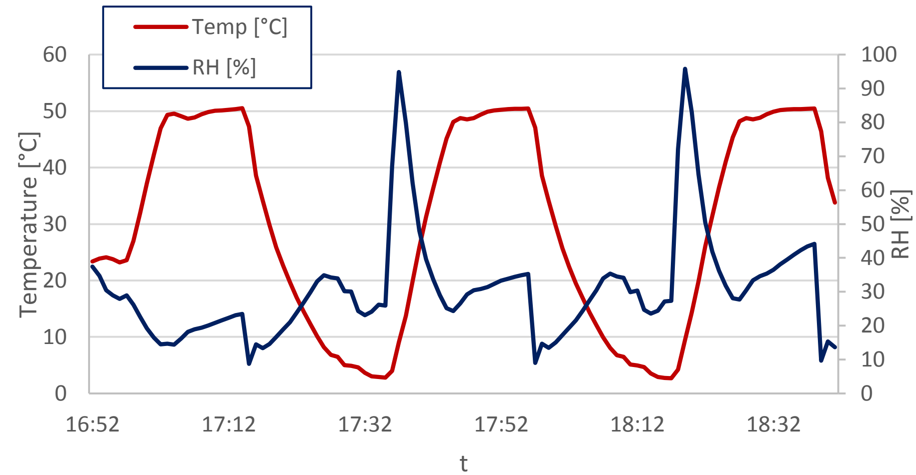


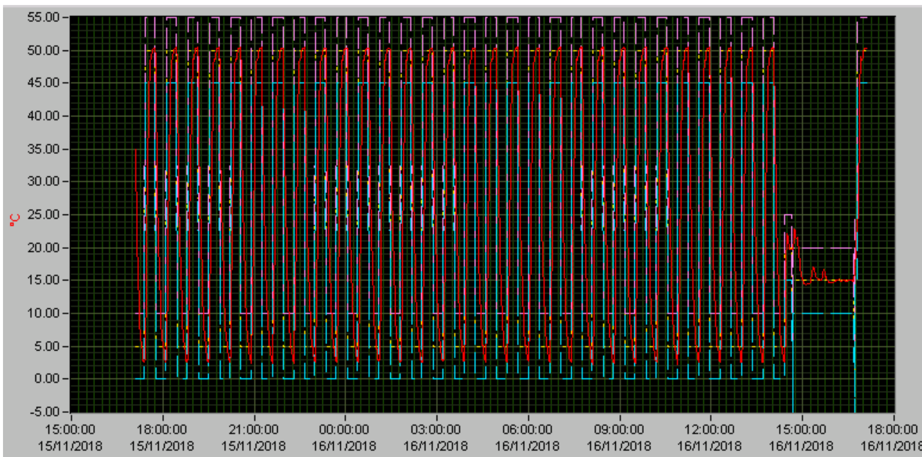
Burn-In Temperature Cycling	Run-In at constant (operational) conditions

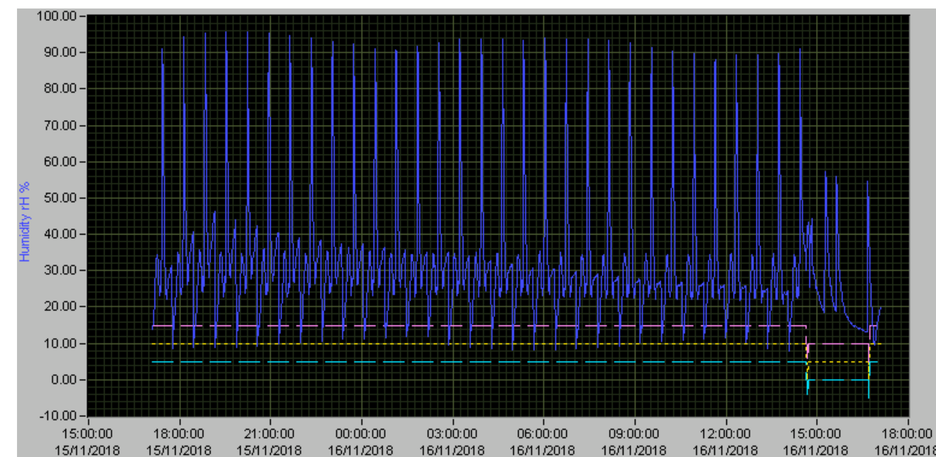
Burn-In

Temperature cycling to raise stress:

- No. of cycles: **30**
- Range: **5 to 50 °C**
- Rate of change: **5°C/min**
- Dwell: **12 min**
- Rel. humidity: **~20%** ! Short peaks of 90% RH, no condensation
- Total time: **22 h**







Burn-In

Tests started on *01.11.2018*:

- 25% of boards already tested; 304 out of 1200
- 12 boards failed the test
  - 4 different circuits (components) affected
  - 3 different causes of failure
  - Main cause of failure: Cleanliness of production
  - Main circuit affected: Pushbutton with R1, C1

Results are preliminary !
Full analysis to be followed up !

Batch	No. of tested boards	Sorted out during inspection*	Sorted out after Burn-In*	Failure/ Error
1	132	1 (+1 high-T test)	10	11
2	137	0	1	1
3	35	1	0	0
TOTAL	**304**	**2 (+1)**	**11**	**12**

* pending

Failures/Errors:	**12**
Cleanliness	9
Manufacturing	1
Other	1
To be investigated	1

Cleanliness breakdown:

Circuit	Count
Pushbutton + R1 + C1	6
IC2	1
IC35	2

- Most failures in batch 1 → Big efforts done to improve the situation:
  - Intensive collaboration with the manufacturer
  - Production process changes (handling, cleaning, inspection, documentation …)

Run-In

- Installation of 8 crates in building *6546*
- Tests without FMC, SFP & LEMO loopbacks
- Room temperature ≥ 30°C
- First 8 crates finished an extended Run-In before Christmas
  - No failures observed

- Status as of *09.01.2019*:

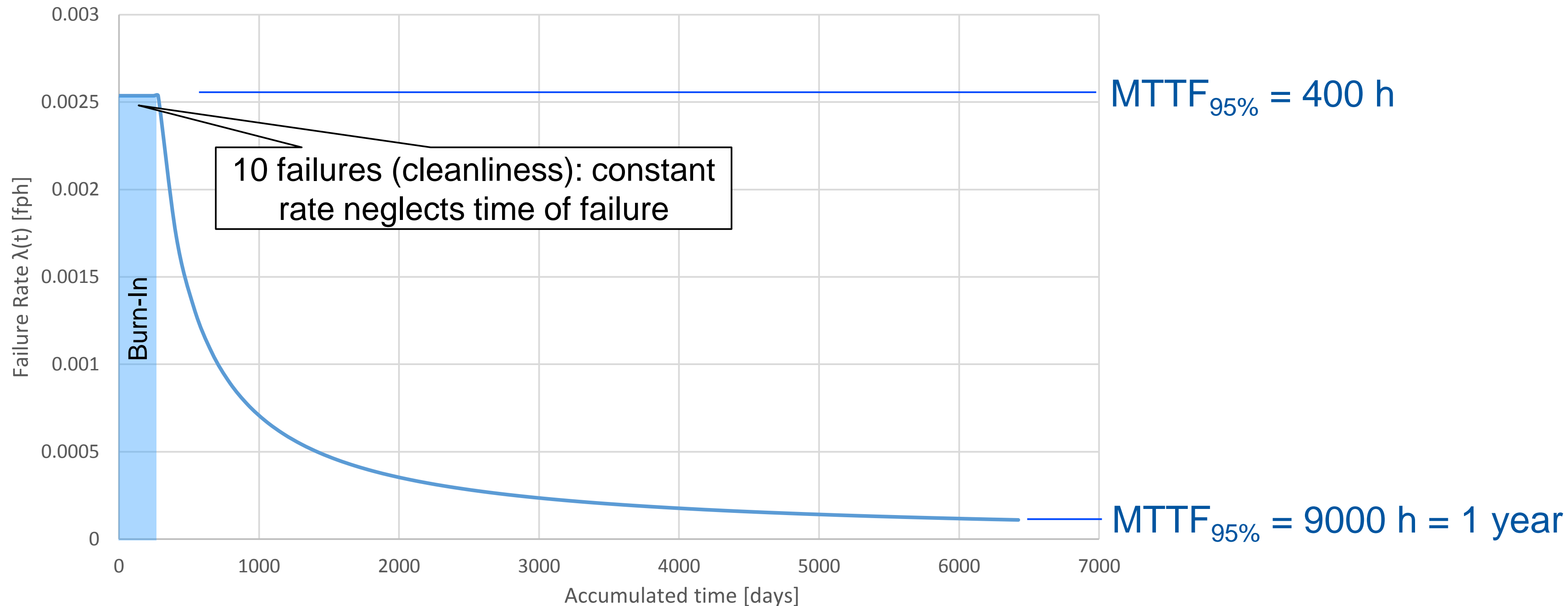
	Lot 1	Lot 2	Total
Start date	22.11.2018	22.12.2018	
End date	20.12.2018	*09.01.2018*	
Number of days	29	19	48
Number of DUTs	128	128	256
Failures	0	?	0
Device hrs	89 000	58 000	**147 000**

Preliminary !

Run-In

MTTF assessment from Burn-In and Run-In (all failures): *status of 09.01.2019*

- No stress acceleration considered; $T_{Run\text{-}In} \geq 30°C$



- High failure number of 1 single cause results in poor MTTF (no actual HW failures!)
- Failure cause was solved (mitigated) + no appearance during run-in

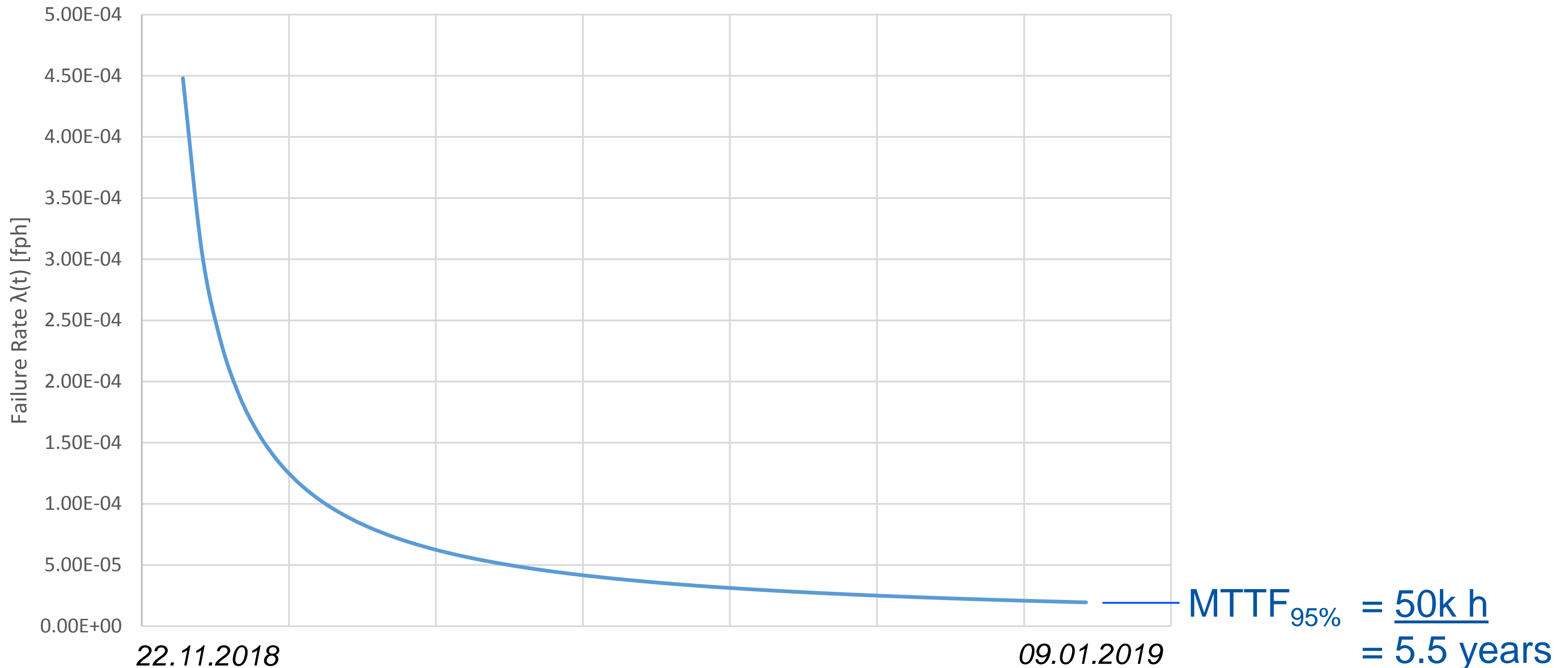
→ Censoring of the failures

Run-In

Preliminary !

MTTF assessment from Burn-In and Run-In (censored): *status of 09.01.2019*

- 150k accumulated device hours; $T_{Run\text{-}In} \geq 30°C$

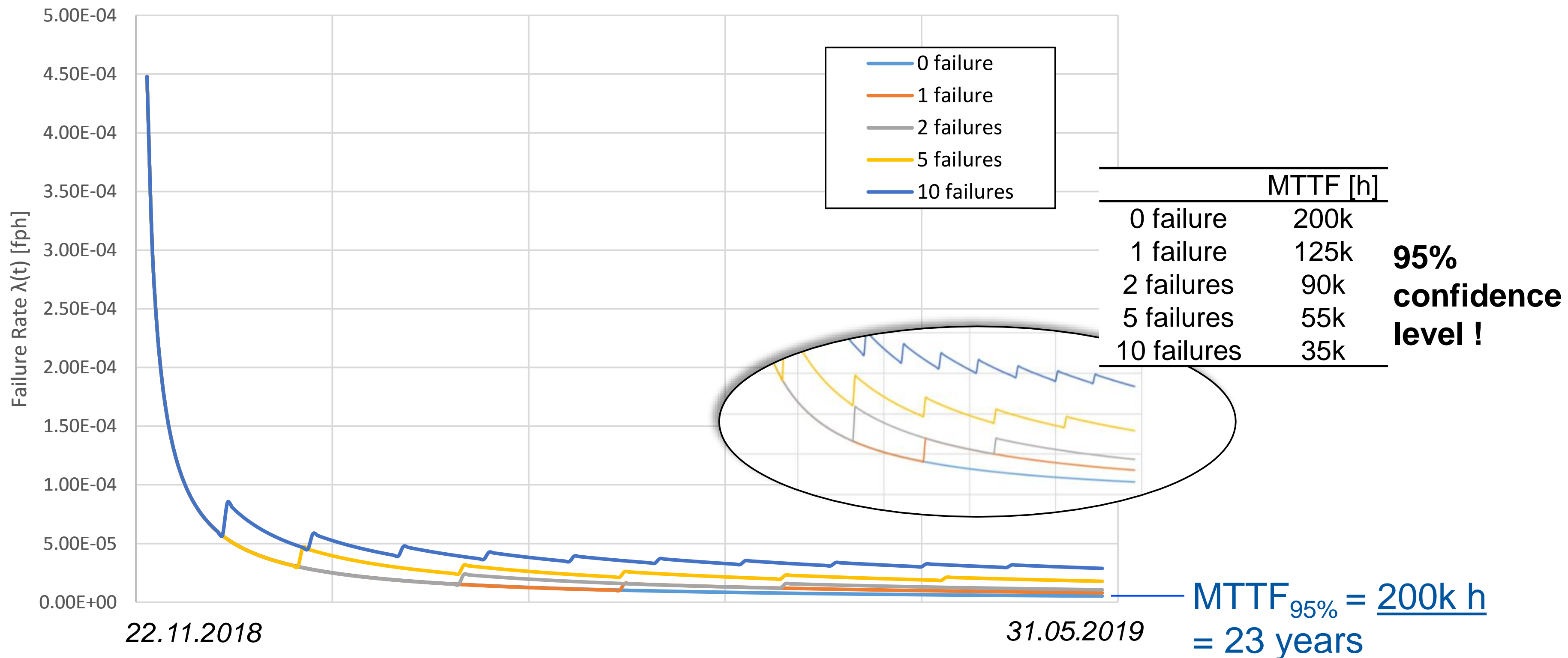


Run-In

Preliminary !

Possible MTTF prediction for future tests (censored):

- Assuming testing until 31.05.2019

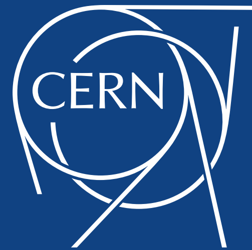


	MTTF [h]
0 failure	200k
1 failure	125k
2 failures	90k
5 failures	55k
10 failures	35k

Summary & Outlook

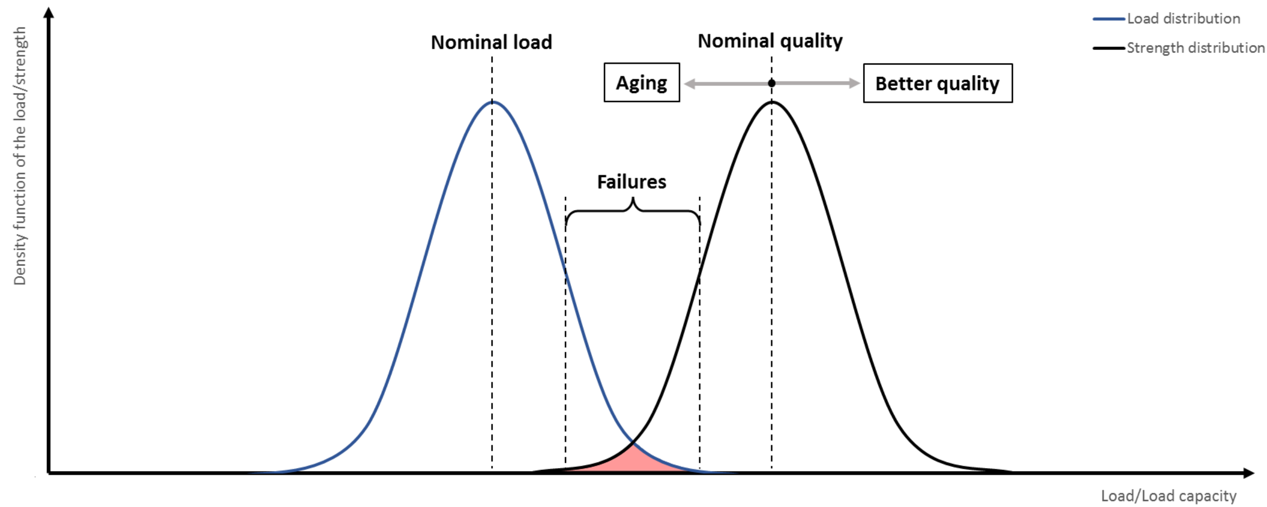
- Successful board validation at different humidity/temperature + at high temperature
  - SFP+ transceiver as bottleneck → Further investigation
- Screening (incl. inspection) turned out to be necessary
  - Until now: Good, reliable design → No PCB/component failures, but:
  - Production issues, mainly cleanliness, revealed during burn-in
    - Efforts done to improve the situation for 2nd & 3rd batch
    - Important to check production & to collaborate with manufacturer
  - Run-In very important to accumulate failure free (low FR) time and to obtain $MTTF_{min}$
    - 09.01.2019: $MTTF_{95\%}$ = 50k hrs (HW failures; no stress acceleration)
    - Final analysis and conclusions to be done after May
- Dependable design methodology proved to be of use
  - Might be used in a flexible way, but proper documentation necessary

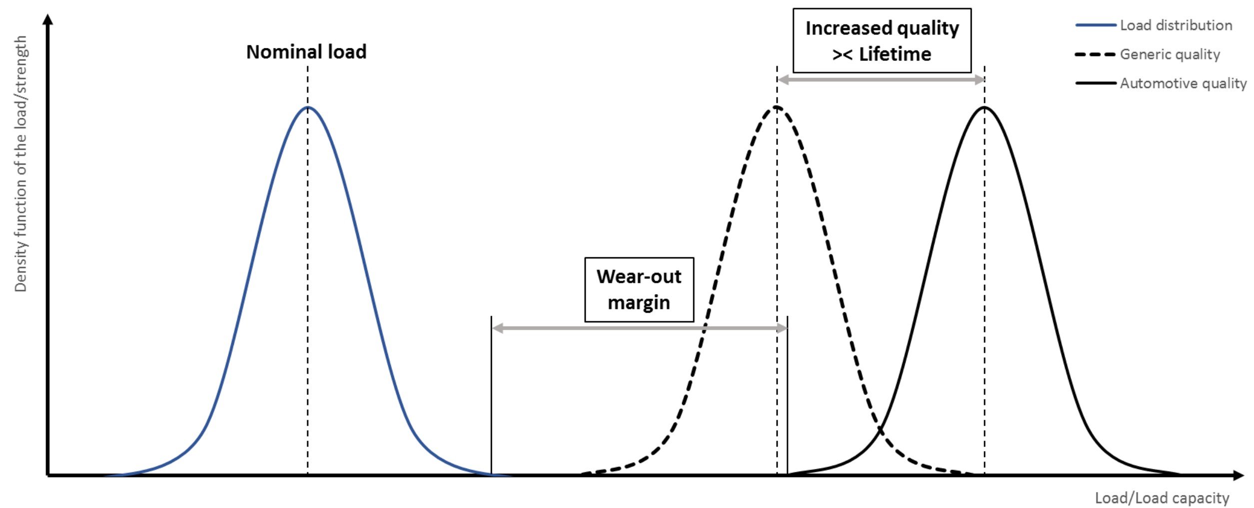
Thank you very much for your attention



And many thanks to all colleagues in BI-BP, BI-SW, BI-BL who contributed to this large project !

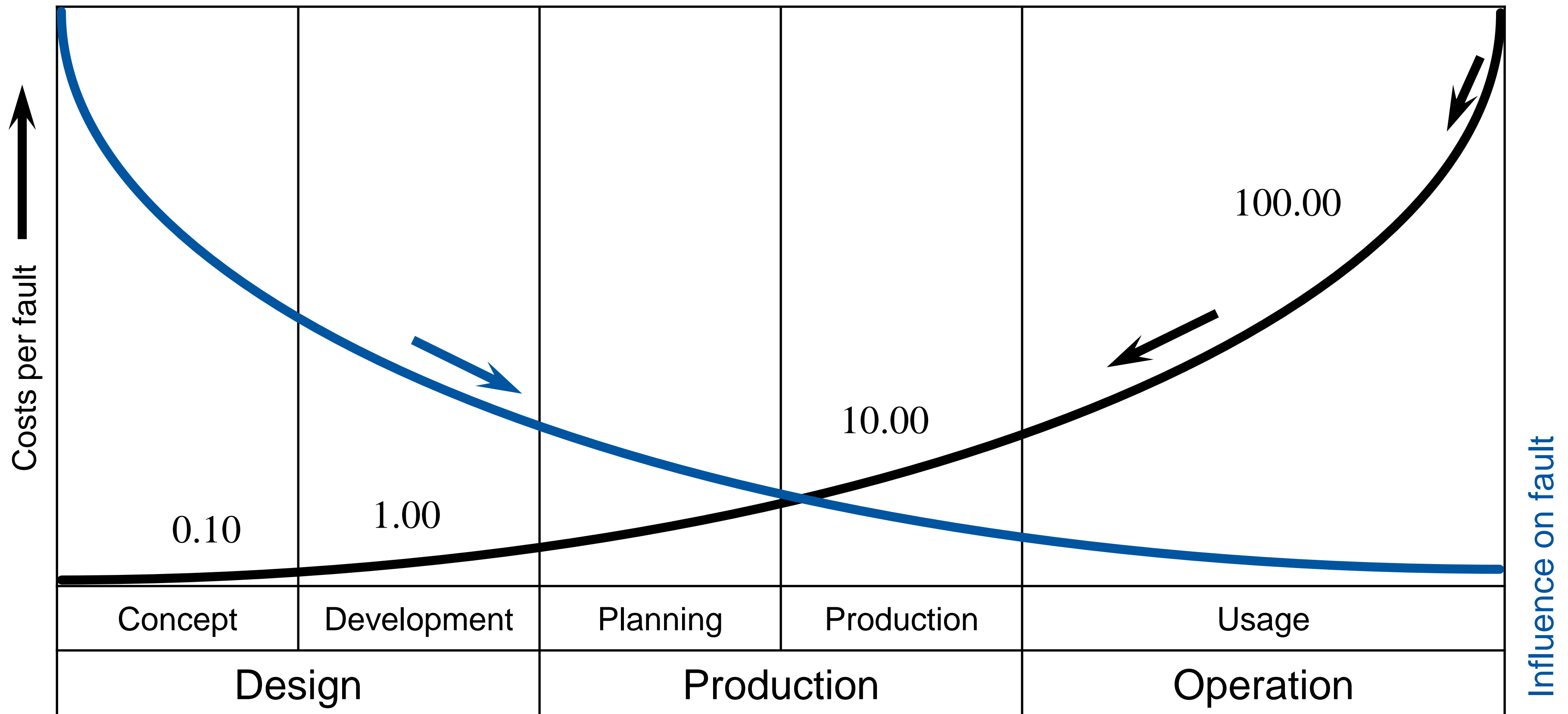
Backup





Backup

- Power of 10 rule: Fault costs during the product life cycle

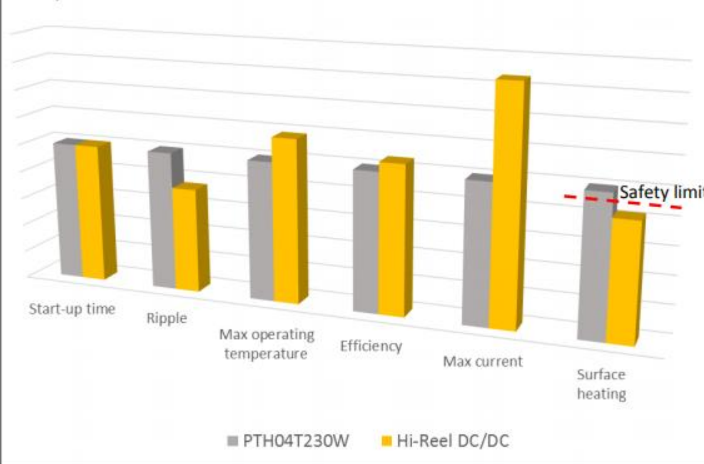


[B. Bertsche, *Reliability in Automotive and Mechanical Engineering*]

Backup

Backup

Performance comparison



- Start-up time: **7ms**.
- Ripple: **< 40mVpp**.
- Max Operating temperature: up to **100˚C**.
- Efficiency: **+6% when 6Amp** are supplied to the output.
- Maximum current: up to **10 Amp**.
- Direct contact safety: **51°C** for 6Amp.

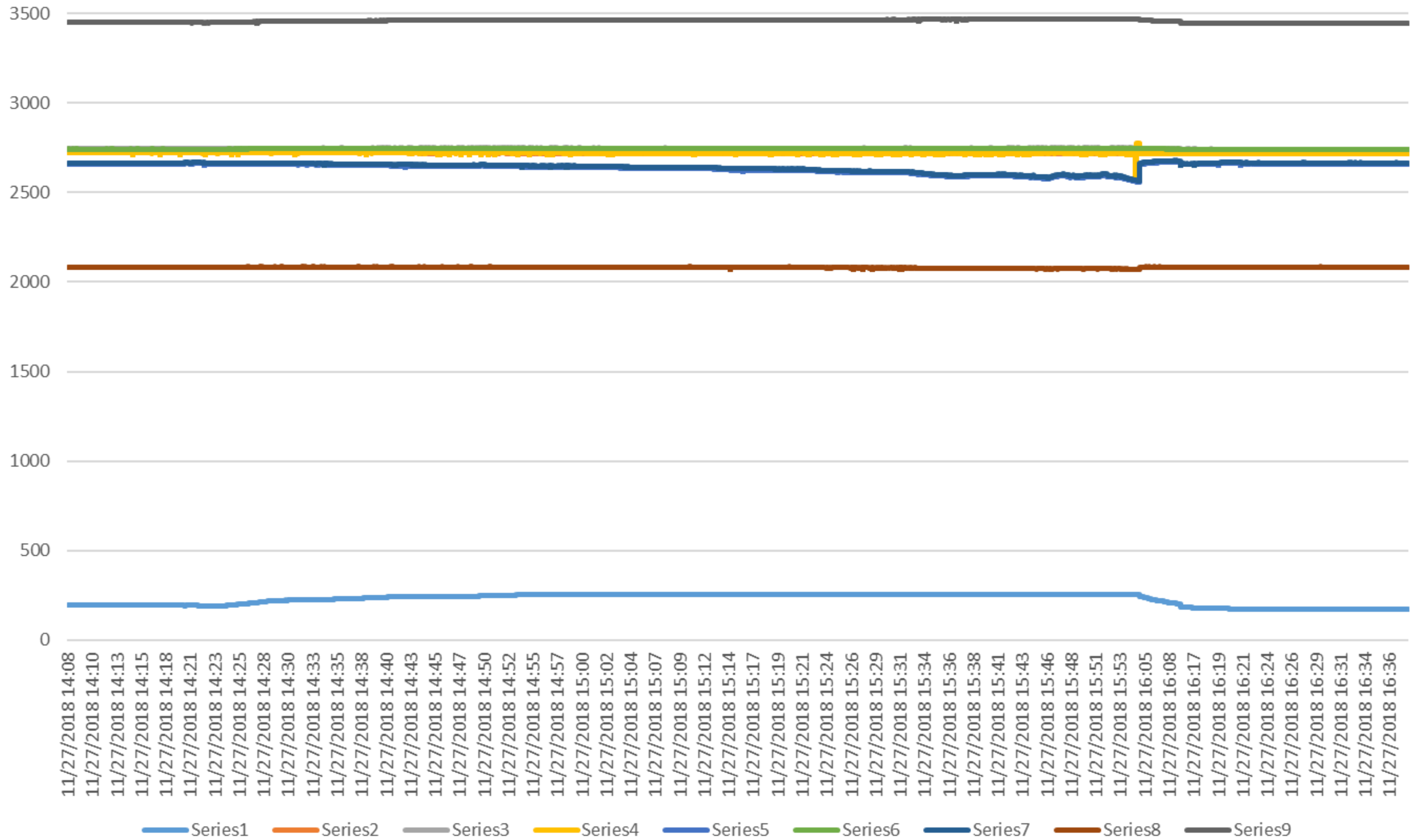
CERN Hi-Rel DC/DC Mean Time To Failure (MTTF)
> 1E+07 working hours
at 40˚C calculated with the Military Handbook 217 plus

We have built an efficient and reliable DC/DC converter

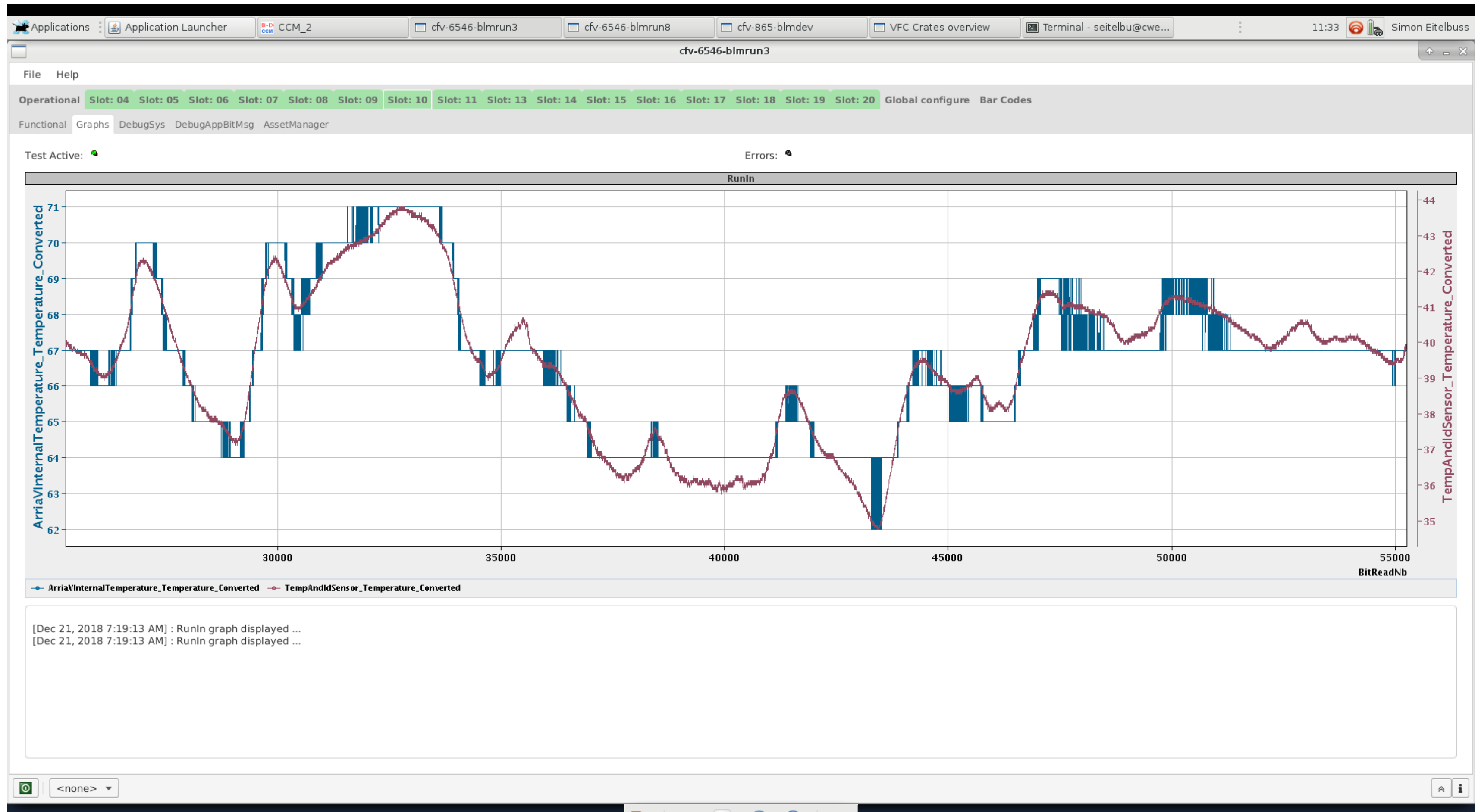
William Viganò (william.vigano@cern.ch) 5

[W. Viganò, *ATS – KT innovation day*]

Backup

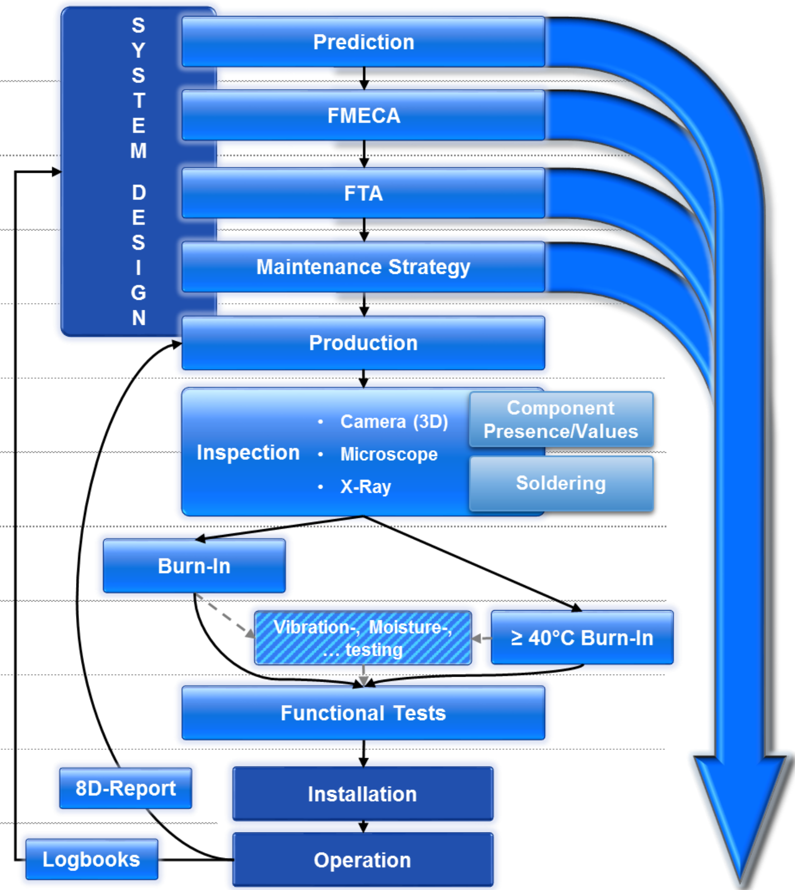


Backup



Backup

#	Actions		Q_{ind}	Q_{tot}
1	FMECA performed/foreseen		0.4	0.5
		Additional FTA	0.1	
2	Maintenance strategy defined			0.2
3	Well-known manufacturer (CERN experience)			0.2
4	Inspection	Camera (3D)	0.2	0.4
		Microscope / X-Ray (BGA)	0.2	
5	Burn-In at operating temperature		0.5	1
		At ≥ 40°C	0.5	
6	Functional PCB Tests			0.2
7	Failure analysis of field returns by manufacturers			0.1
8	Failure/Repair logbook; Jira-Tracking			0.4
		Q_{SUM} (≤3)		3
		AdjustmentFactor A_Q ($0.25 \le A_Q \le 1$)		0.250

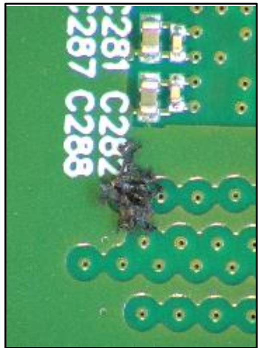


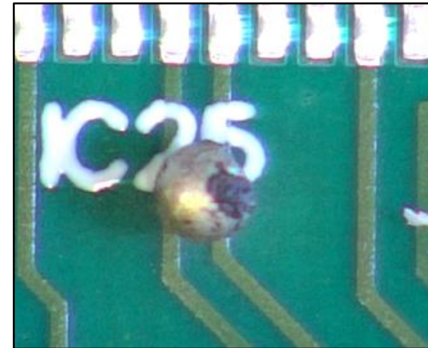
$$A_Q = 1 - \frac{1}{4} * Q_{SUM}$$

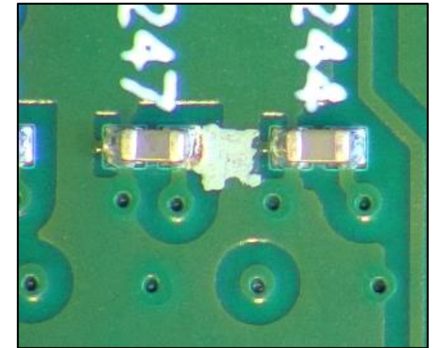
RASWG meeting, 02.03.2017

Backup

- Additional microscope inspection at CERN before burn-in
- Many findings for 1st batch (~50%), 9 boards failed:
  - Cleanliness
  - Handling (scratches, packaging, …)
  - Tolerances
  - Documentation







- After consultation with Norcott, situation improved for 2nd batch, but still not perfect: