Simulation of SET/SEU in microelectronics: AFTU software
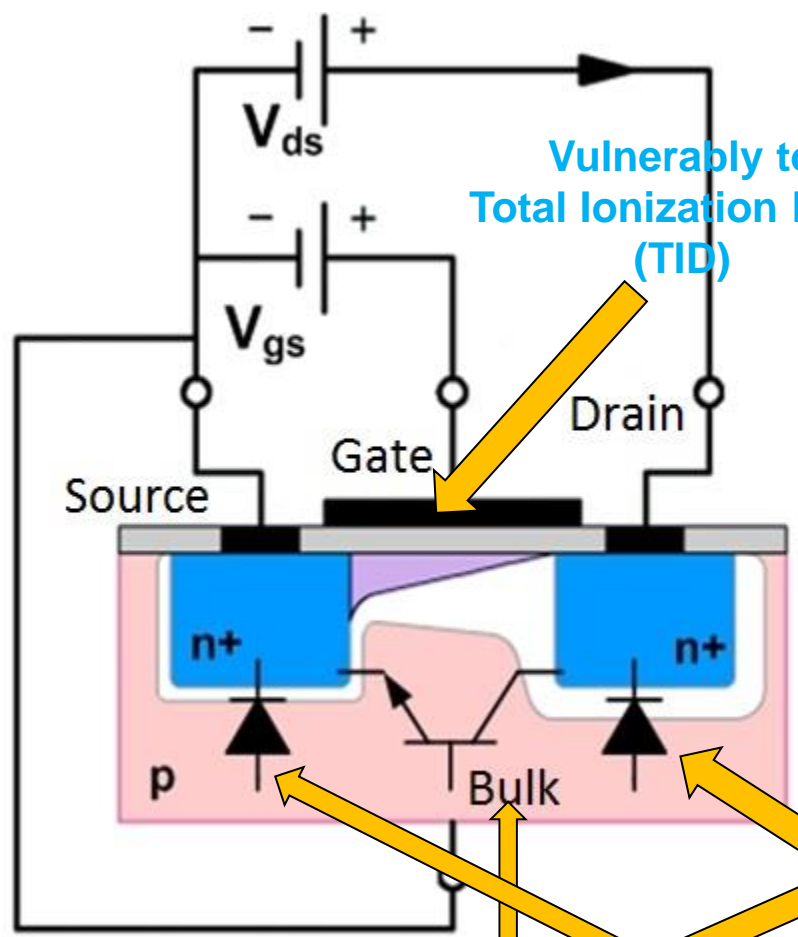
F.R. Palomo[1], F.Muñoz[1], F.Márquez[1], E.López-Morillo[1]
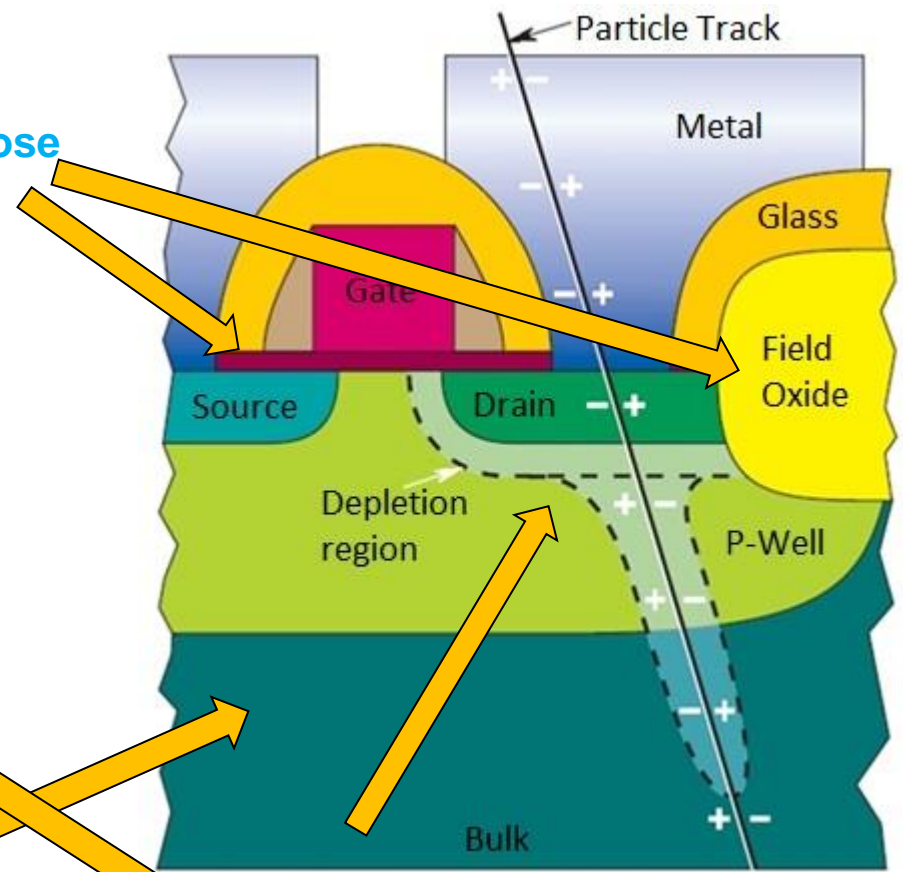Mohsine Menouni[2]
fpalomo@us.es
[1]Departamento Ingeniería Electrónica, Escuela Superior de Ingenieros
Universidad de Sevilla, Spain
[2]CPPM Centre de Physique des Particules de Marseille
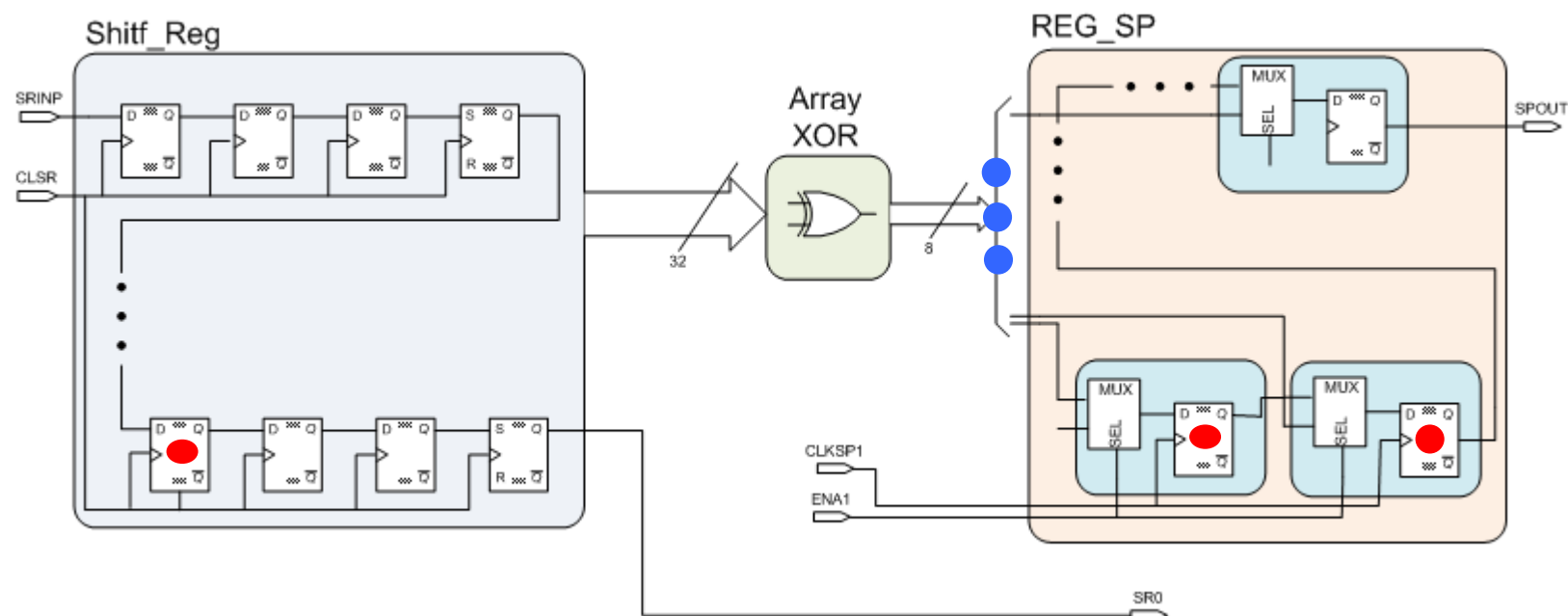Marseille, France

Radiation effects in Electronics

**Vulnerably to
Total Ionization Dose
(TID)**

**Vulnerably to Displacement
Dose Damage**

**Vulnerably to Transient
Ionization
(Single Event Currents)**
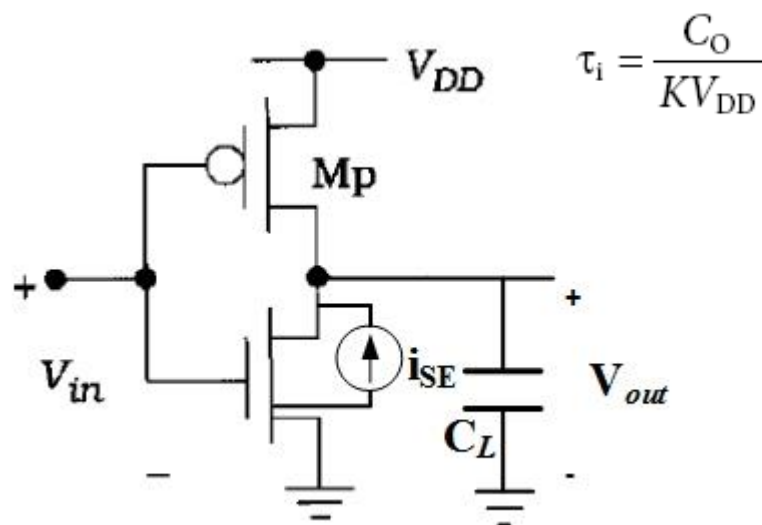
SEU (bitflips) and SET (glitches)

Single Event Upsets (Red) affect to memory cells producing bit flips
Single Event Transients (Blue) affect to any transistor, producing glitches
SETs effects are harder to detect and can produce Cascade Bitflips

SEE and Critical Charge

$$\tau_i = \frac{C_O}{KV_{DD}}$$

τ_i: inverter intrinsic time constant
  C_O is the total output capacitance
  V_{dd} is the power rail voltage

τ_e: charge collection single event
time constant (< 1ps)

$\tau_e \ll \tau_i$ implies Single Event Effect (switching)

So at Critical node (Vout) the SEE induced ΔV is:

$i_{SE}(t)$ is the single event photocurrent
$Q_{collected}$ is the total charge delivered to/from the node by the single event photocurrent
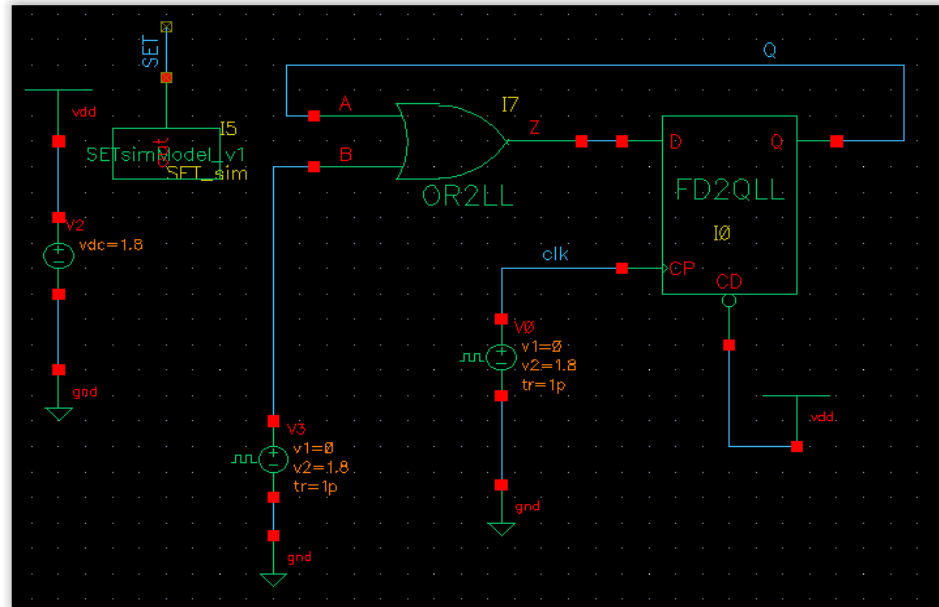C_N is the total nodal capacitance

$$\Delta V = \int \frac{i_{SE}(t)}{C_N}\, dt = \frac{Q_{collected}}{C_N}$$

$$Q_{crit} = C_N \cdot \Delta V_{nm}$$

Q_{crit} is the total charge delivered to/from the node by the single event photocurrent
C_N is the total nodal capacitance
ΔV_{nm} is the node voltage

Extreme Environment Electronics, J.D.Cressler, H.A.Mantooth (eds), CRC Press 2013, chap. 15

What is AFTU?

The <u>A</u>nalog <u>FTU</u> Hardware Debugging System
is a software tool to evaluate the SEE sensitivity
of analog/mixed signal circuits
at transistor level
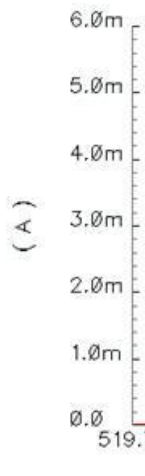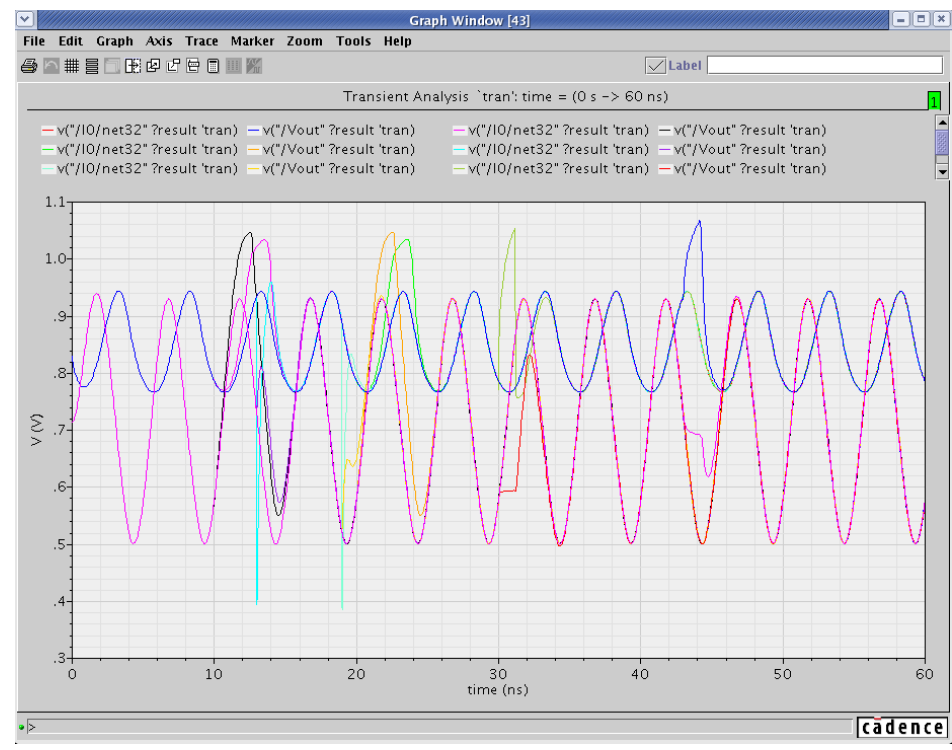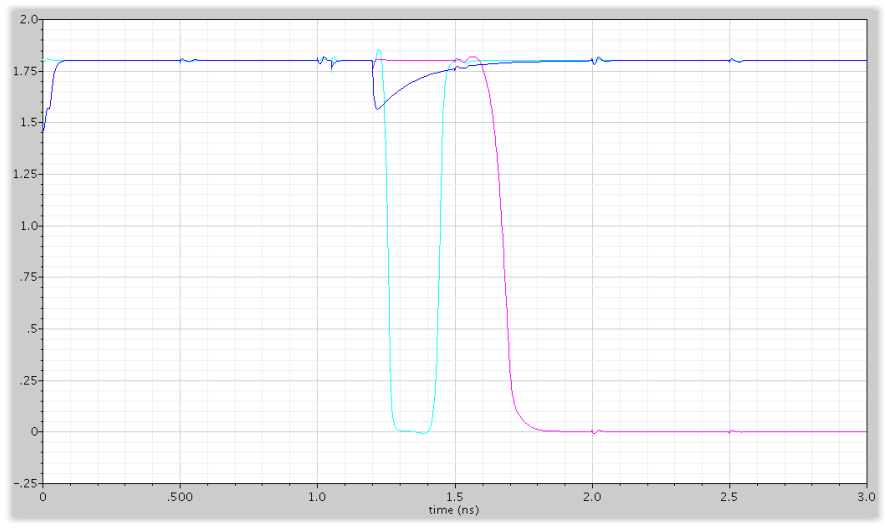
How does it work?

AFTU parses a Spectre design netlist...

...to generate a parametric simulation Ocean script

-Analysis of Transient Effects in Analogue Topologies, F.Marquez, F.Muñoz, F.R.Palomo, M.A.Aguirre and M.Ullán, AMICSA 2012, Noordvijk, Netherlands 26th -28th August 2012, http://microelectronics.esa.int/amicsa/2012/amicsa2012.htm

-Automatic inspection of SET sensitivity in analog cells, F.Márquez, F.Muñoz, M.A.Aguirre, F.R.Palomo and M.Ullán, SMACD'12, Sevilla, Spain, 19th-21st Sept. 2012 http://www2.imse-cnm.csic.es/~smacd2012/SMACD_2012/HOME.html

-AFTU, an analog single event effects automatic analysis tool, F.Marquez, L.Sanz, F.R.Palomo, F. Muñoz and M.A.Aguirre, AMICSA 2014, CERN, Switzerland, 30th June-1st July 2014, https://indico.cern.ch/event/277669/

-Automatic Single Event Effects Sensitivity Analysis of a 13-Bit Successive Approximation ADC, F.Márquez, F.Muñoz, F.R.Palomo, L.Sanz, E.López-Morillo, M.Aguirre and A.Jiménez, **IEEE Transactions on Nuclear Science,62(4) 2015, pp.1609-1616**
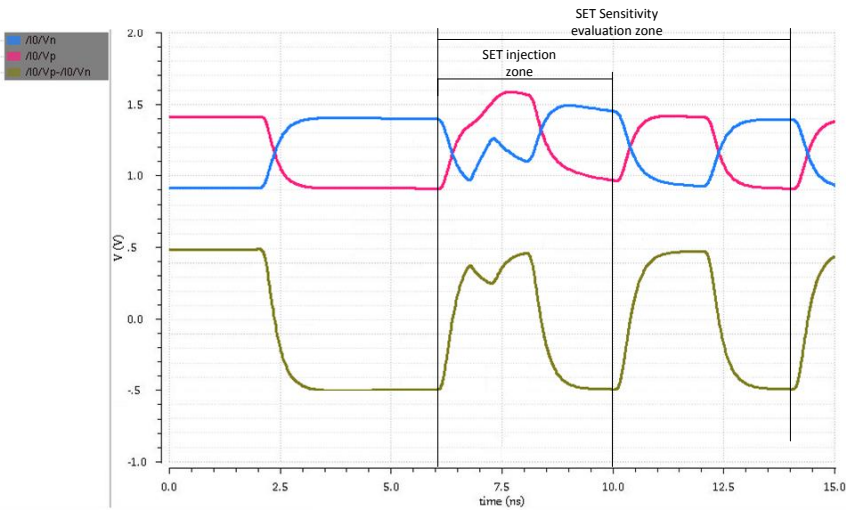
…emulates Single Event Effects…

$$I_{rad} = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{\tau}{\tau_d}} - e^{-\frac{\tau}{\tau_r}}\right)$$

$$Q_c = \frac{\rho \cdot LET \cdot d}{3.6}$$

Injection Current
Default Model

An injection current source at every node or at user selected nodes is the way to emulate the SEE. The injection source model can be changed.
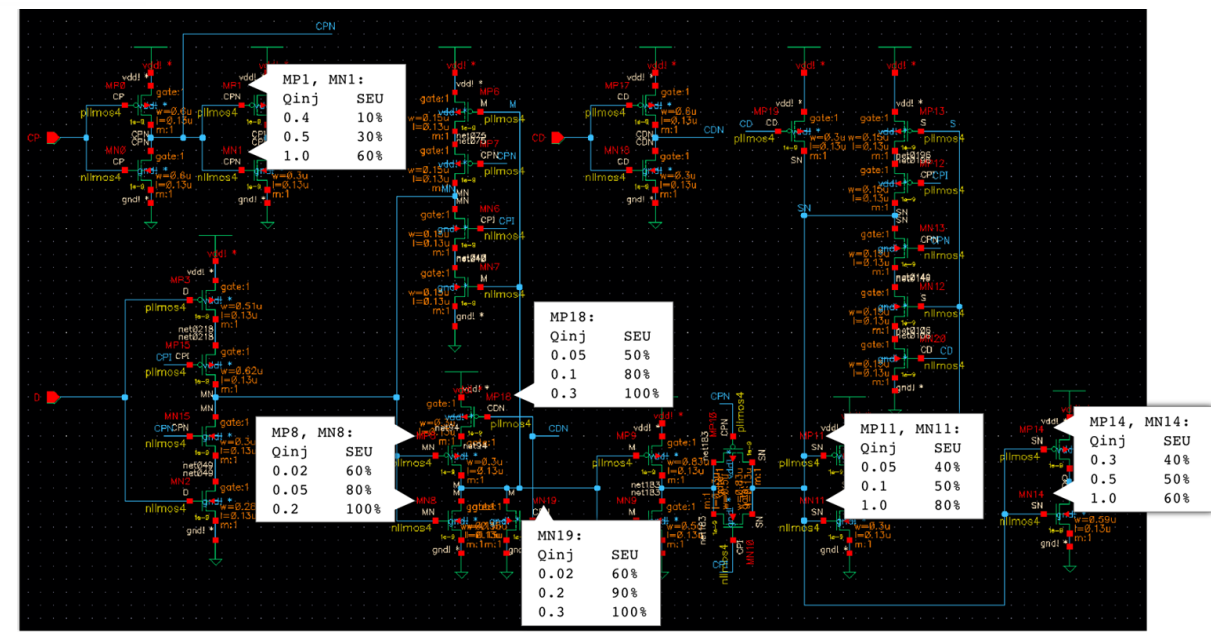
… and evaluates vulnerabilities

- The user defines injection and evaluation zones
- and select the appropriate hard coded heuristic to analyze the parametric simulation results

D-latch circuit , STMicroelectronics 130 nm

- The final result is a list of vulnerabilities (in terms of the heuristic) for each user selected node in the design.
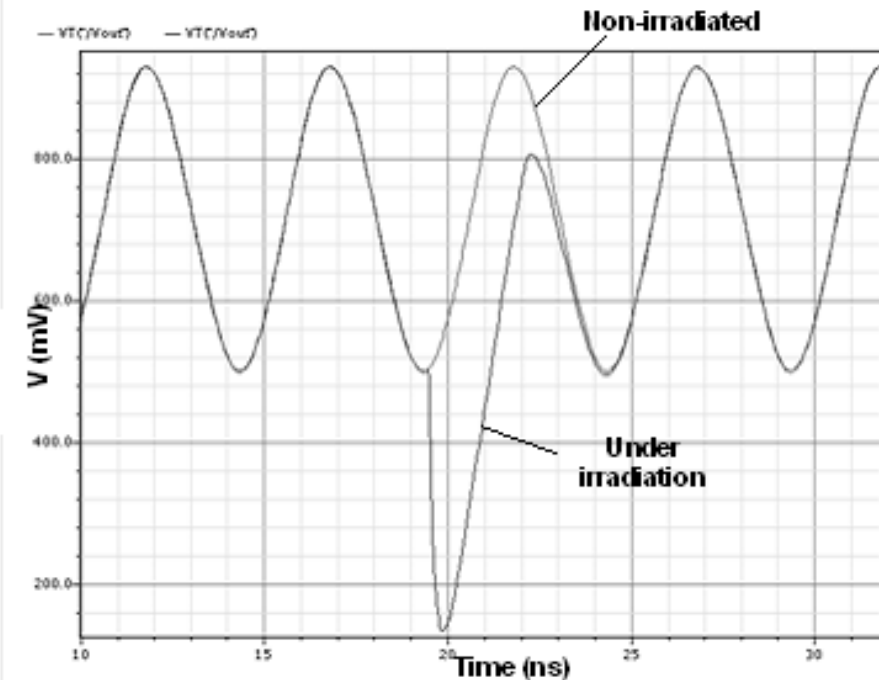
User Web Interface (Fault Injection Campaign)

Hard Coded Heuristics

Deviation Recovery
(ex. analog circuits SET's)

Time Ranges
(ex. digital SEU's & differential circuits SET's)

- Recovery Time
- Signal Voltage Deviation

- Total time between up to 4 signal thresholds

Simulation of SET/SEU in microelectronics

.F.R.Palomo. LHC Rad Effects Workshop 11/30

User Web Interface (Heuristics)

Analysis of FE-I4 DICE structures

- Circuit schematics (interleaved version)
  - Increased robustness against SET/SEU due to DICE structure
  - Only affected by simultaneous impacts at n1,n3 or n2, n4

LOAD line

DICE structure analysis with AFTU

- Impacts at 4 different times (0.5, 1.25, 2.5, 3.25 ns) in every transistor of the DICE
  - Every possible input/output state is studied

DICE structure analysis with AFTU

- Impacts at 4 different times (0.5, 1.25, 2.5, 3.25 ns) in every transistor of the DICE

- According to results, there are 4 classes of transistors:

  ➤ Class I: no effect on the latch output

  ➤ Class II: transient glitch at the latch output, with no permanent effect (SET)

  ➤ Class III: a change of the state at the output (SEU)

  ➤ Class IV: a pair of transistors simultaneously impacted that generate a SEU at the latch output.

DICE structure analysis with AFTU

Qinj	Class	Transistors
0.05 pC	I	All except class II
	II	M10, M11, M9, M3
	III	None
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1)
0.1 pC	I	All except class II
	II	M10, M11, M9, M3
	III	None
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9-M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)
0.2 pC	I	M7, M8, M2, M1, MU1_X_M_u3
	II	M10, M11, M9, M3
	III	M0, M4, M6, M5, MU1_X_M_u2
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)
0.3 pC	I	M7, M8, M2, M1, MU1_X_M_u3
	II	M10, M11, M9, M3
	III	M0, M4, M6, M5, MU1_X_M_u2
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9-M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)

- Impacts in every transistor of the DICE for different values of injected charge

- "Secondary latch" seems safe when simple impacts are performed

DICE structure analysis with AFTU

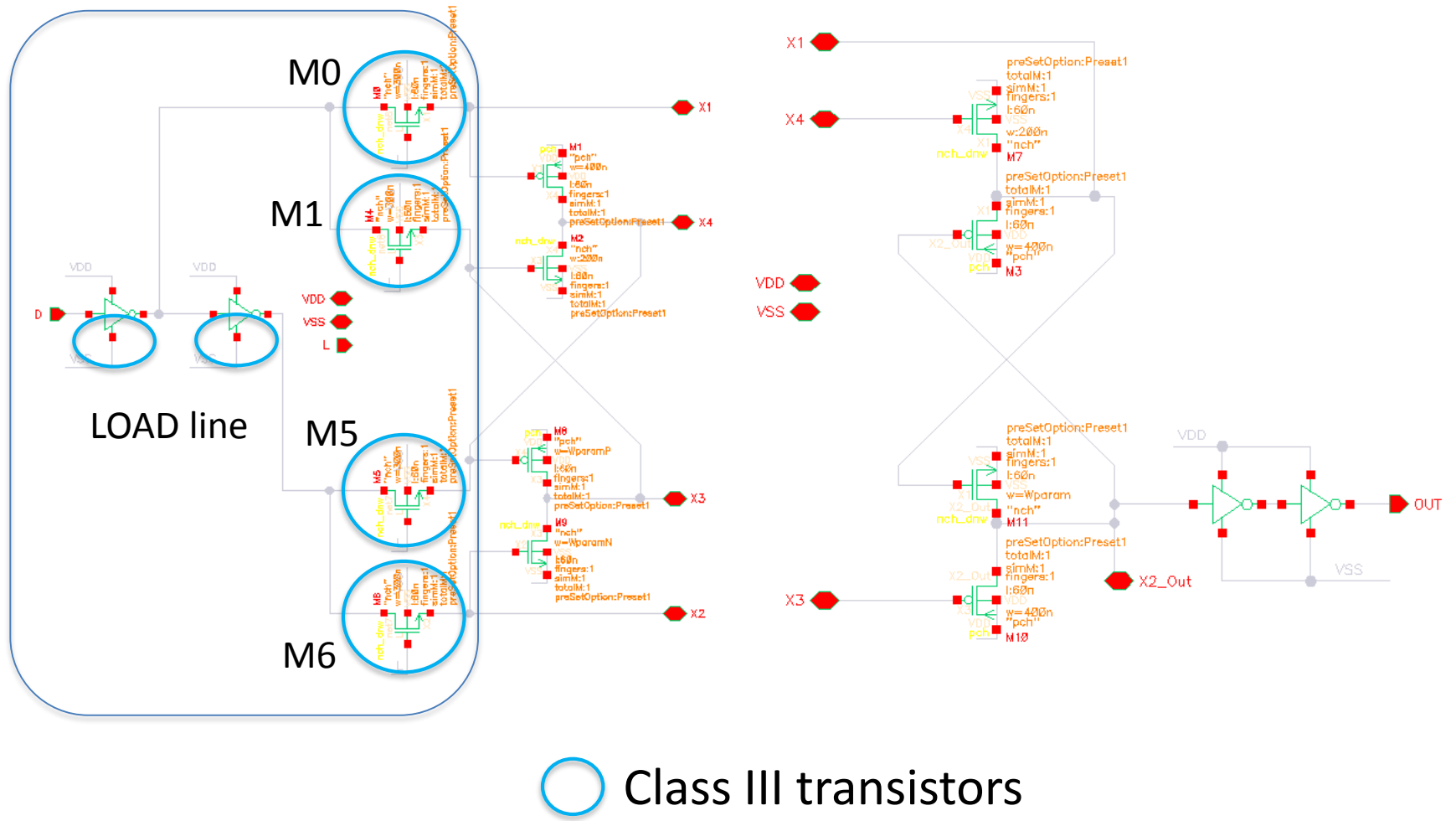| Qinj	Class	Transistors
0.05 pC	I	All except class II
	II	M10, M11, M9, M3
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0.1 pC	I	All except class II
	II	M10, M11, M9, M3
	III	None
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9-M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)
0.2 pC	I	M7, M8, M2, M1, MU1_X_M_u3
	II	M10, M11, M9, M3
	III	M0, M4, M6, M5, MU1_X_M_u2
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)
0.3 pC	I	M7, M8, M2, M1, MU1_X_M_u3
	II	M10, M11, M9, M3
	III	M0, M4, M6, M5, MU1_X_M_u2
	IV	(M11-M8), (M11-M2), (M10-M7), (M10-M1), (M11-M6), (M11-M5), (M10-M0), (M10-M4), (M7-M9), (M7-M0), (M7-M4), (M9-M1), (M9-M0), (M9-M4), (M3-M2), (M3-M5), (M3-M6), (M8-M3), (M8-M6)

- Impacts in every transistor of the DICE for different values of injected charge

- "Secondary latch" seems safe when simple impacts are performed

- DICE structure → No class III transistors expected

DICE structure analysis with AFTU

Class III transistors

DICE structure analysis with AFTU

- A single impact in transistor M0 affects nodes 1 & 3 of DICE latch → SEU (class III)

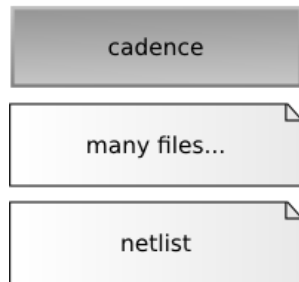# A SET (glitch) in LOAD line produces a cascade of bitflips!

Results

- AFTU predicts that SETs in the LOAD line produce a SEU cascade downstream

- From experiments: they confirm AFTU predictions, see next talk, "SEU/SET results in ATLAS IBL FE-I4-B" by Marcello Bindi

Thanks for your attention
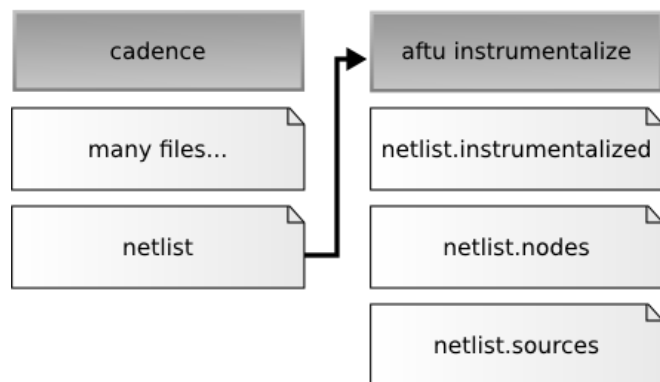fpalomo@us.es

AFTU ToolChain

Before using AFTU:

- The user designs a circuit with Cadence as usual.
- The design is simulated through a testbench.
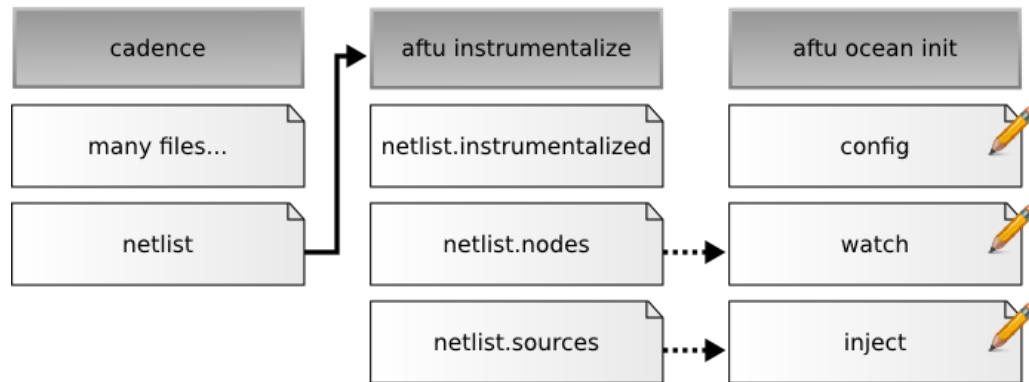- Of all files generated by Cadence, we pick the **netlist**.

AFTU instrumentalize

The instrumentalizer implements a parser for the SPECTRE language

- Replaces the **netlist** with a *functionally identical* one allowing SEE emulation.
- **netlist.nodes** lists all observable circuit nodes.
- **netlist.sources** lists all transistors where an impact can be emulated.
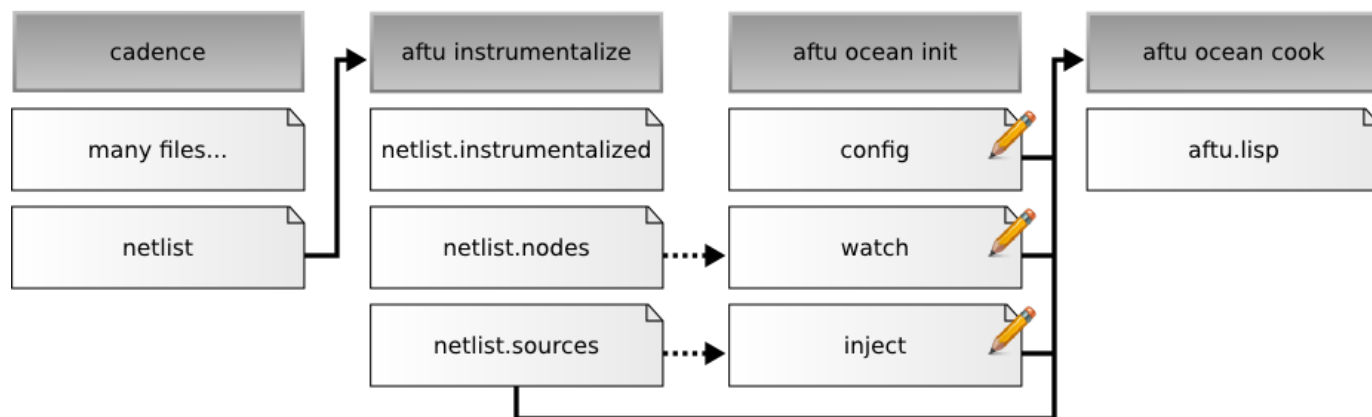
AFTU ocean init

AFTU projects are flexible and give the user many options for analysis.
- **config** contains paths, times, heuristics parameters, initial values…
- **watch** defines all elements in the circuit to be observed during the simulation
- **inject** defines where, when and how much charge we inject (SEE emulation).
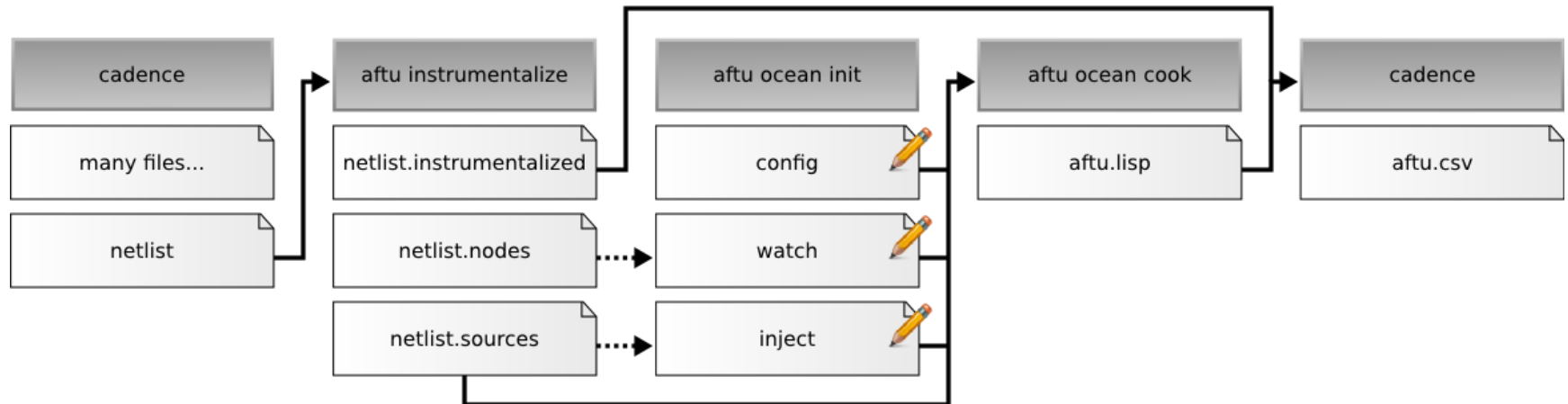
AFTU Ocean cook

From all this data an Ocean simulation script is produced
- Includes all paths and required data.
- Describes the way to perform the user defined test campaign.
- Defines how to analyze the results of the campaign.
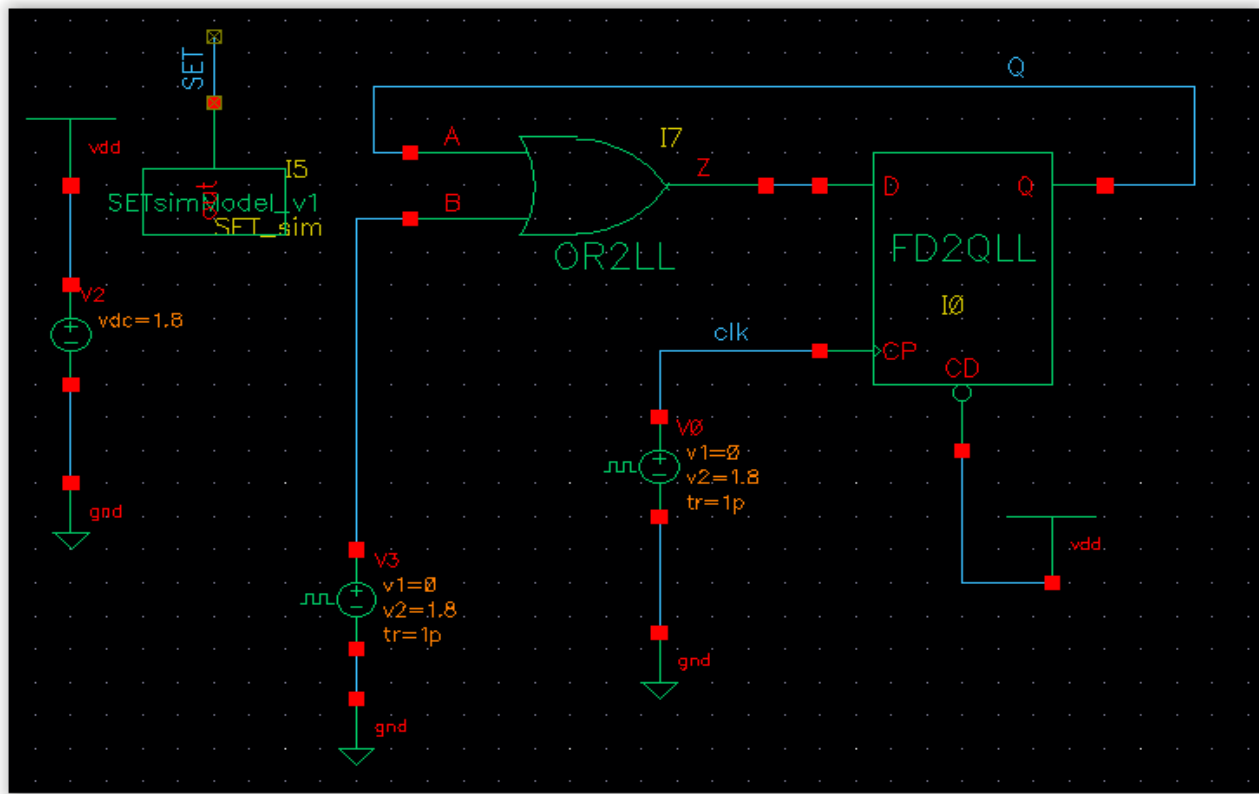
AFTU campaign

Cadence runs the provided script.
It produces a CSV file with the desired statistics.
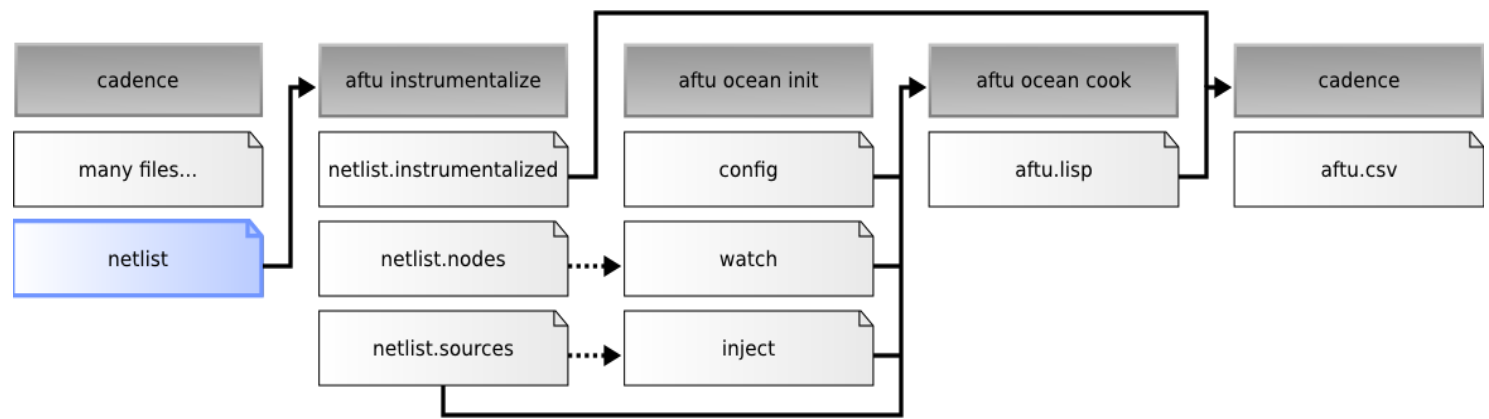This uncovers radiation vulnerabilities in the circuit.

A Practical Example

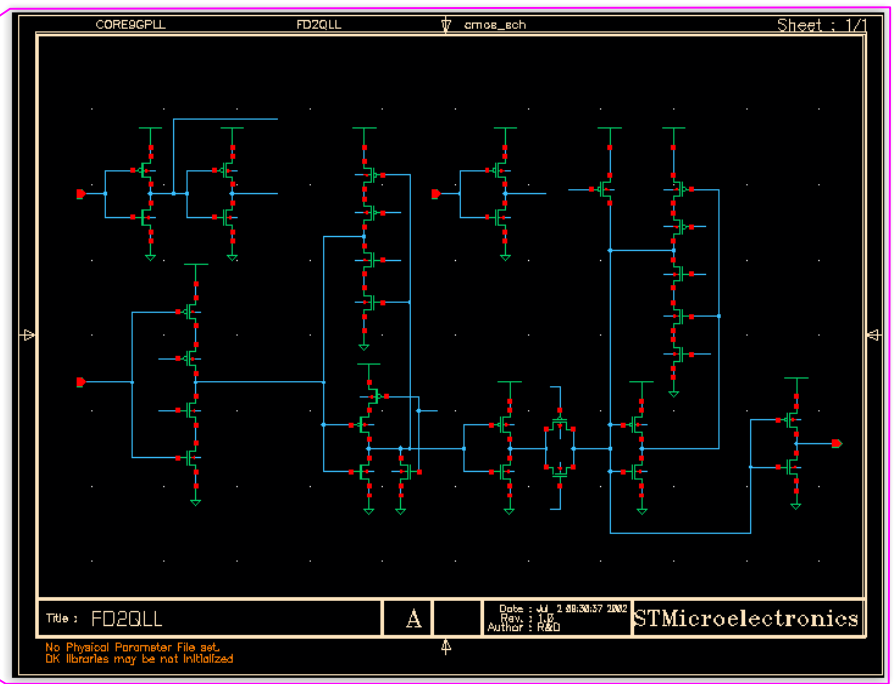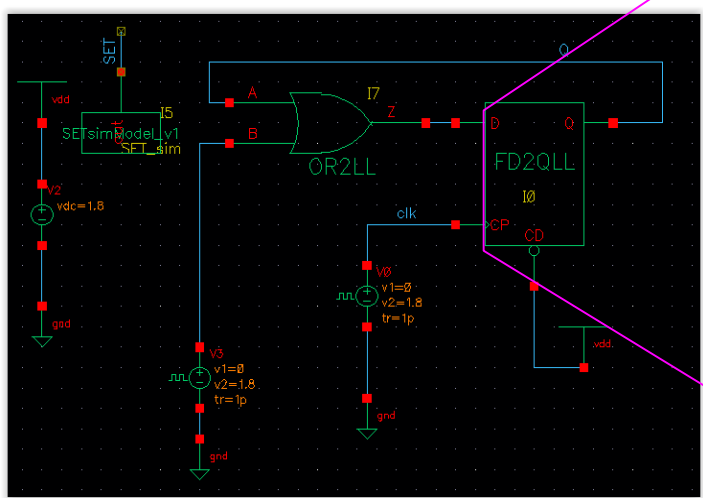## Let's say we have this circuit:

What is the critical charge to produce a SEU?
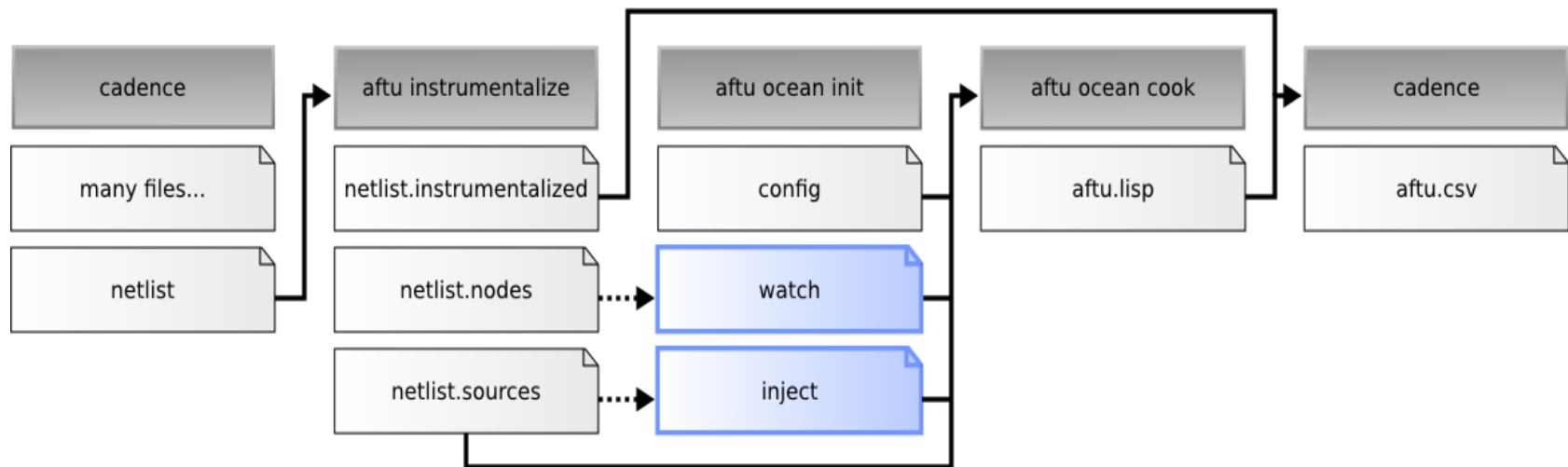
Netlist

D-latch transient testbench and schematic view of the digital cell STMicroelectronics 130 nm

Watch & Inject


```
watch Q = /Q :
        threshold = 0.975 ;
```

```
inject I0_MP19:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n, 1.1n, 1.2n, 1.3n, 1.4n, 1.5n, 1.6n, 1.7n, 1.8n, 1.9n;

    inject I0_MN19:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n, 1.1n, 1.2n, 1.3n, 1.4n, 1.5n, 1.6n, 1.7n, 1.8n, 1.9n;

    inject I0_MP18:
        Q = .025p, .05p, 0.1p, .2p, .5p, .75p, 1p, 1.5p;
        t = 1.0n, 1.1n, 1.2n, 1.3n, 1.4n, 1.5n, 1.6n, 1.7n, 1.8n, 1.9n;
```
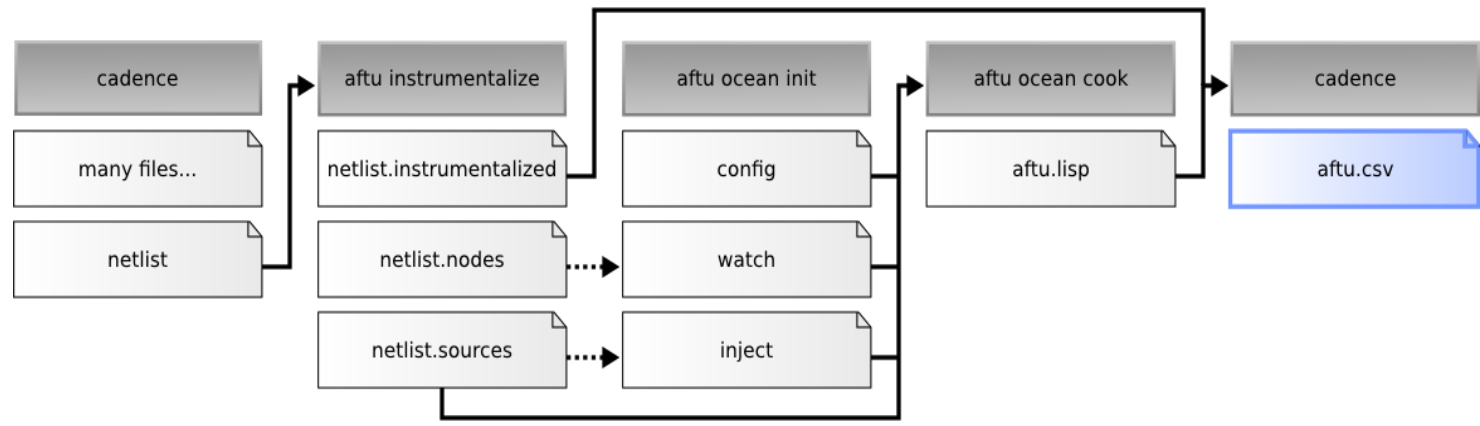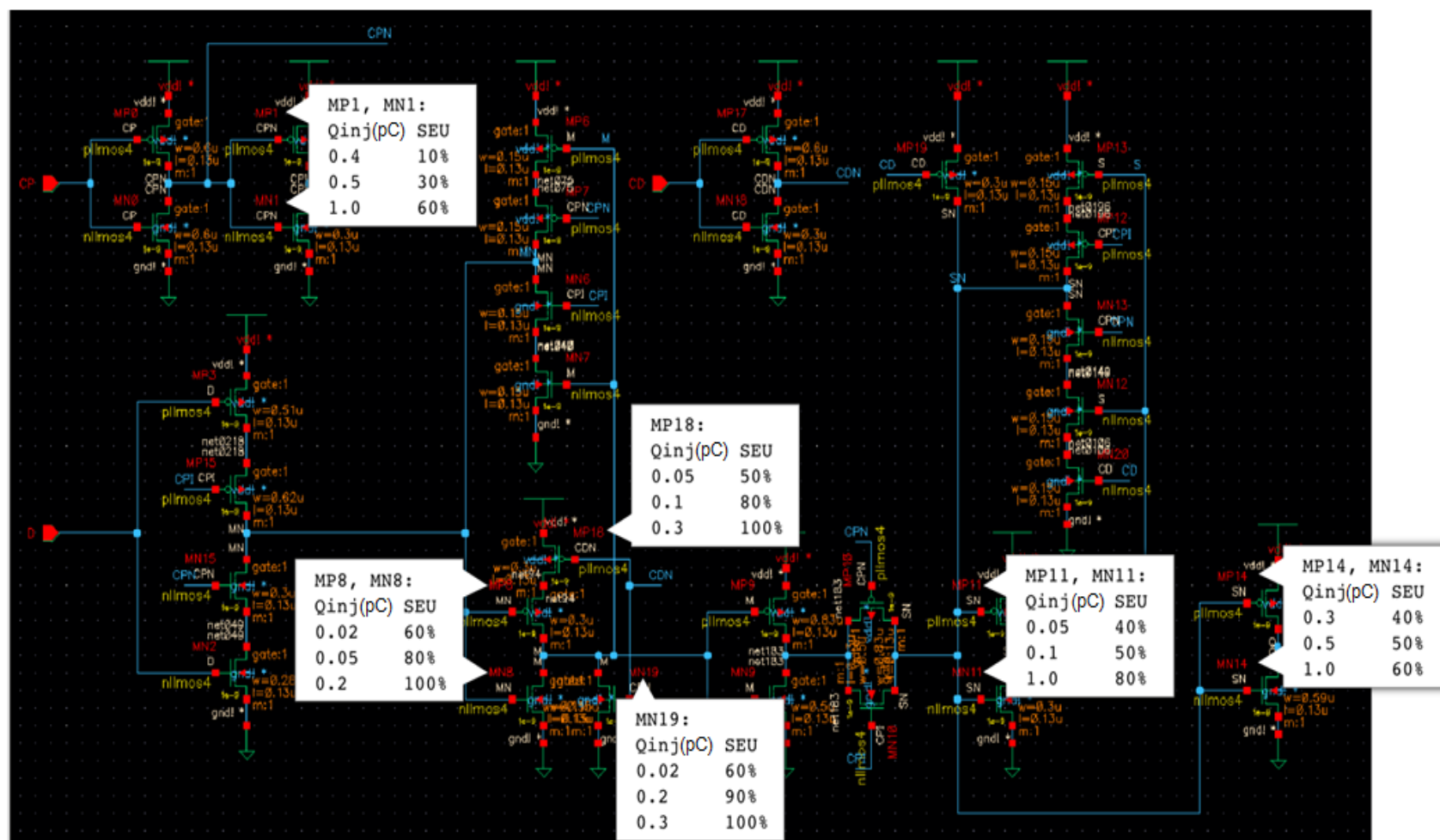
Results


```
Output ImpactNode Qinj  Timp    Trec      Vmax            Output ImpactNode Qinj   Timp     Trec      Vmax

V_Q    I0_MP18  2.5e-14 1e-09   0.000000 0.001941        V_Q    I0_MN11  2.5e-14 1e-09   0.000000 0.006827
       V_Q    I0_MP18  2.5e-14 1.1e-09 0.000000 0.00219
                                                         V_Q    I0_MN11  2.5e-14 1.9e-09 0.000000 0.016568
V_Q    I0_MP18  2.5e-14 1.9e-09 0.000000 0.003664           V_Q    I0_MN11  5e-14   1e-09   0.000000 0.017084
       V_Q    I0_MP18  5e-14   1e-09   2.000000 1.807421
       V_Q    I0_MP18  5e-14   1.1e-09 1.910000 1.807422     V_Q    I0_MN11  5e-14   1.3e-09 0.000000 0.005371
       V_Q    I0_MP18  5e-14   1.2e-09 1.800000 1.807426     V_Q    I0_MN11  5e-14   1.4e-09 1.610000 1.806680
       V_Q    I0_MP18  5e-14   1.3e-09 1.700000 1.807384     V_Q    I0_MN11  5e-14   1.5e-09 1.500000 1.806814
                                                            V_Q    I0_MN11  5e-14   1.6e-09 1.400000 1.805740
       V_Q    I0_MP18  5e-14   1.8e-09 0.000000 0.519730     V_Q    I0_MN11  5e-14   1.7e-09 1.300000 1.802925
       V_Q    I0_MP18  5e-14   1.9e-09 1.100000 1.803023     V_Q    I0_MN11  5e-14   1.8e-09 0.240000 1.404223
```

"Deviation Recovery" heuristic analysis

Results

D-latch circuit , STMicroelectronics 130 nm

For this particular test, we shot at 10 different instants per period to obtain a sensitivity percentage: for example if 7 impacts generate a SEU we have a sensitivity of 70%