SEU/SET results in ATLAS IBL FE-I4B chip during Run 2 operation

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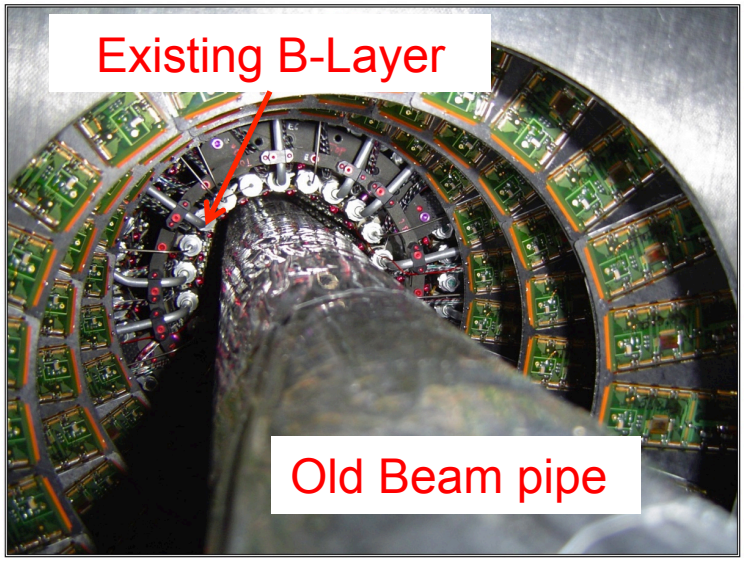
Outlook

- IBL and the FE-I4B chip
- Operational conditions during LHC Run 2
- Effect of Single Event Upset (SEU) /Single Event Transient (SET) in FE-I4 global registers
- Effect of SEU/SET in single pixel registers
- SEU/SET cross section measurements
- Mitigation strategies and test run results
- Conclusions and future plan

The IBL detector

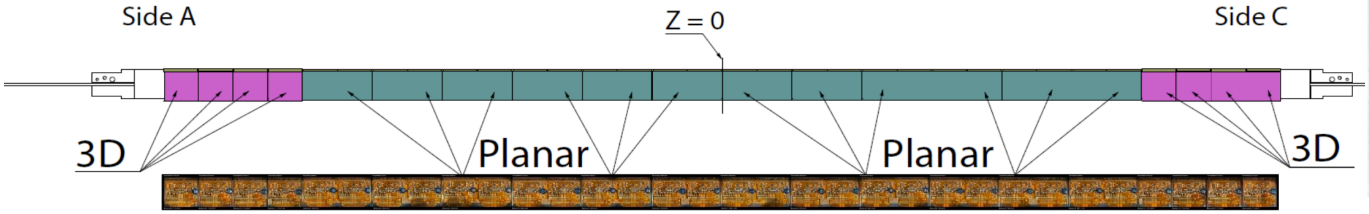
The IBL idea in a nutshell

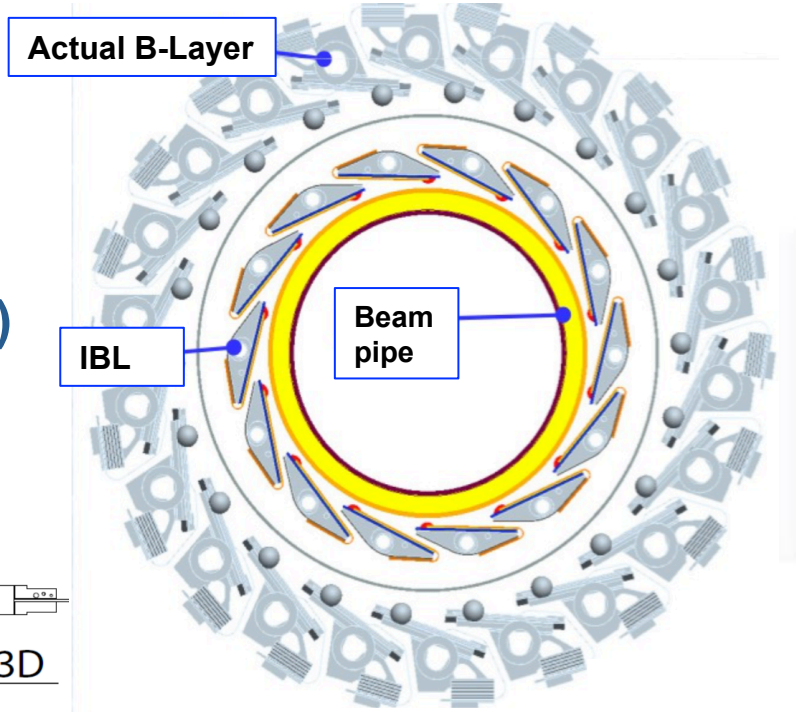
- add a single detector layer built around a new thinner Beryllium beam-pipe (radius 29 mm ➔ 25 mm)
- closer to interaction point (5.05 → 3.27 cm)
- smaller pixel size (50 × 400 → 50 × 250 μm^2)
- IBL + beam pipe and structures : < 2% $X_{0.}$



The IBL layout

- **14 staves** in the **phi** coordinate
- **32 front-end chips** along the **eta (z)** coordinate
- mixed configuration of **planar (75%)** and **3D (25%)** sensors technologies along the staves.
- **~12 million** pixels in total!

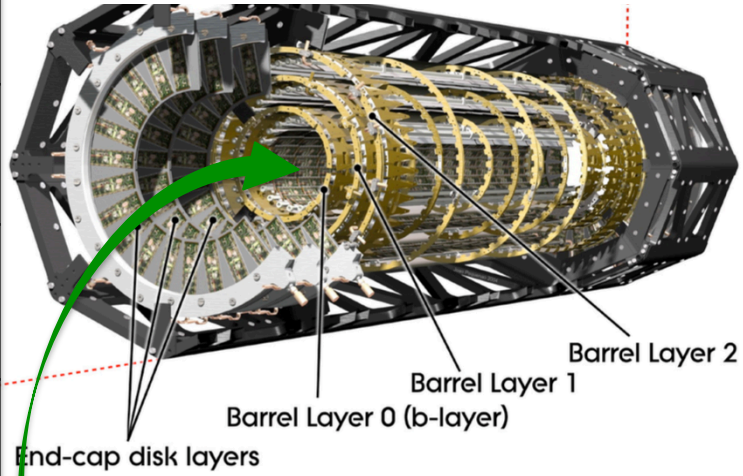


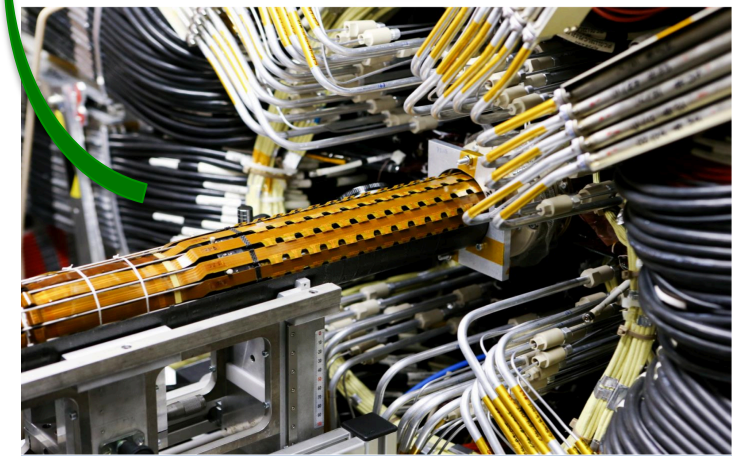


The Pixel (+IBL) detector

	Pixel		IBL
Sensor Technology	n^+-in-n (only planar)		n^+-in-n/n^+-in-p (planar/3D)
Sensor Thickness	250 μm		**200**/230 μm
Front End Technology	FE-I3 250 nm CMOS		FE-I4 **130** nm CMOS
Pixel Size	50 x 400 μm^2 (short side along R-φ)		50 x **250** μm^2 (short side along R-φ)
Radiation Hardness	50 Mrad (500 kGy) ~ 1 x 10^{15} n_{eq}·cm^{-2}		**250 Mrad (2500 kGy)** ~ 5 x 10^{15} n_{eq}·cm^{-2}
Barrel <Radius> Or EndCaps Radius$_{Min}$	B-Layer	50.5 mm	**33 mm**
	Layer 1	88.5 mm	
	Layer 2	122.5 mm	
	EndCaps	88.8 mm	

3 Layers Pixel Detector
since start of **RUN 1 (2010)**



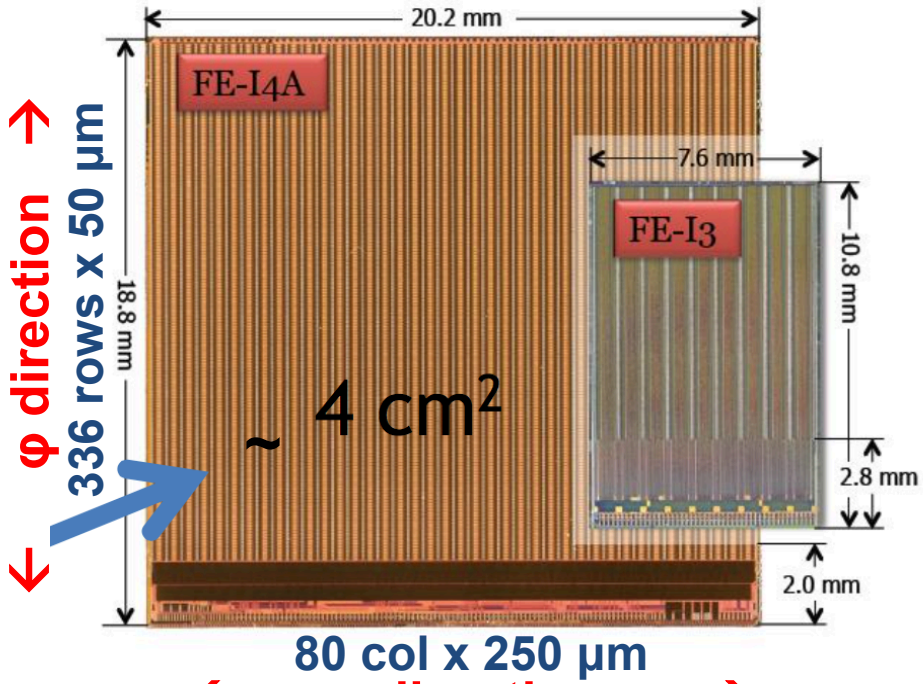


Insertable B-Layer (IBL)
since start of **RUN2 (2014)**

The IBL FE-I4 chip vs Pixel FE-I3

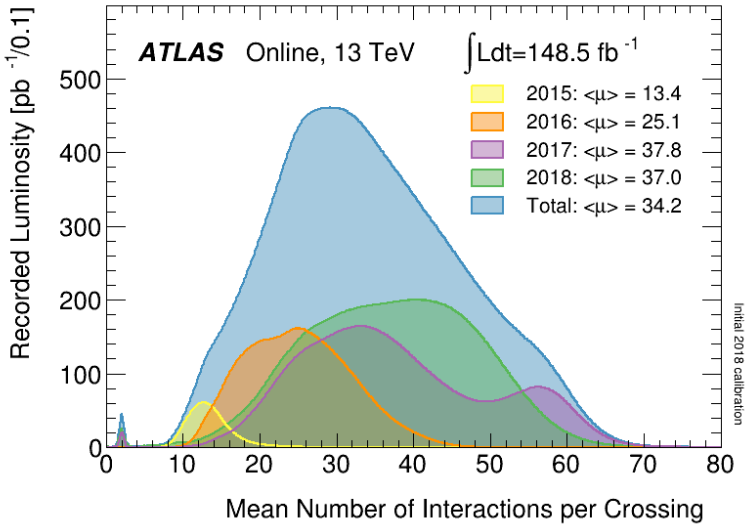
Main features of the new front-end:

- new read-out electronics to face with larger occupancy and radiation
  - ➔ 26880 hybrid pixels arranged in 336 rows (**50 µm pitch**) x 80 (**250 µm pitch**) columns
  - ➔ **8b/10b encoding at 160 Mb/s** (FE-I3 used 40 Mb/s and no encoding)
  - ➔ IBM **130 nm CMOS** process (FE-I3 used 250 nm)
  - ➔ Mostly **std. cell library and std. linear transistors** (FE-I3 used special rad. hard cell library and enclosed transistors)



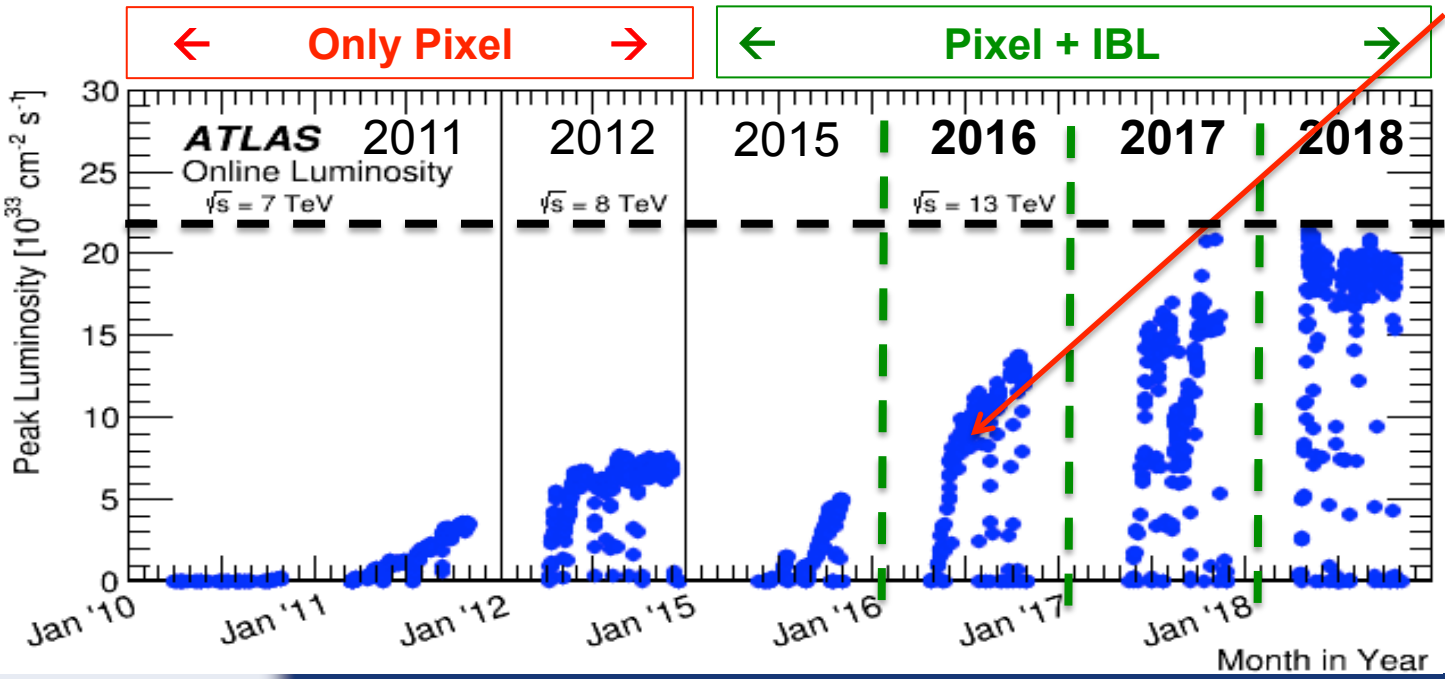
- new read-out architecture
  - ➔ hits collection limited to **Pixel Digital Region, 2x2 pixels matrix** (FE-I3 used Double Column granularity, 2 x 160 pixels matrix)
- larger size (and active area) to reduce the costs (and inefficiencies)
  - ➔ **~ 4 cm² size** (FE-I3 was 0,8 cm²)
  - ➔ **~ 89% of active area** (FE-I3 had 74%)
- max power dissipation < 300 mW/cm²

Tough working conditions for Pixel/IBL



Integrated Luminosity	Pixel (fb^{-1})	IBL (fb^{-1})
Collected up to 2012 (Run 1)	29	0
Collected up to 2018 (Run 1 + Run 2)	189	160
Expected by 2023 (Run 1 + Run 2 + Run 3)	**~430**	**~400**

240 pb^{-1} expected in Run 3 ➔ **LHC Evian Workshop**



- First SEU induced radiation effects visible already in 2016!

Expected peak conditions

- Inst. luminosity **~ 2 • 10^{34} cm^{-2} s^{-1}**
- Pile up **~ 60**
- Lvl1 rate **~100 kHz**.
- *Fill lumi. up to **1 fb^{-1}!***

Fluence vs Integrated dose

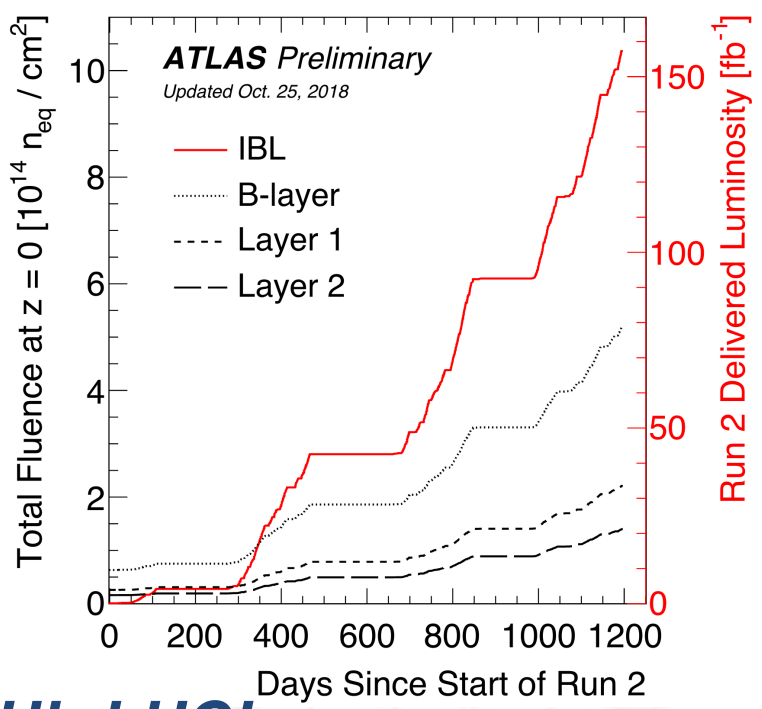
	Pixel*			IBL		
	Integrated Luminosity (fb^{-1})	Fluence B-Layer ($n_{eq} \cdot cm^{-2}$)	Dose B-Layer (Mrad)	Integrated Luminosity (fb^{-1})	Fluence @ z=0 ($n_{eq} \cdot cm^{-2}$)	Dose @ z=32 cm (Mrad)
Run 1 + Run 2	189	~ $5.5 \cdot 10^{14}$	~ 28	160	~ 10^{15}	~ 53
Expected by 2023 Run 1 + Run 2 + Run 3	**~ 430 (~ 240 Run 3)**	**~ 1.1 10^{15}**	**~ 60**	**~400 (~ 240 Run 3)**	**~ $2.5 \cdot 10^{15}$**	**~ 132**

**Assuming, for simplicity, the same Energy of 13 TeV in Run1,Run2 and Run3.*

Number from From Pythia + Fluka

➔ IBL should still be within the FE-I4 specification (250/300 Mrad) in Run 3.

➔ B-Layer will probably exceed FE-I3 limit (50 Mrad) in Run 3.



N.B. Full ATLAS tracker will be replaced at HL-LHC!

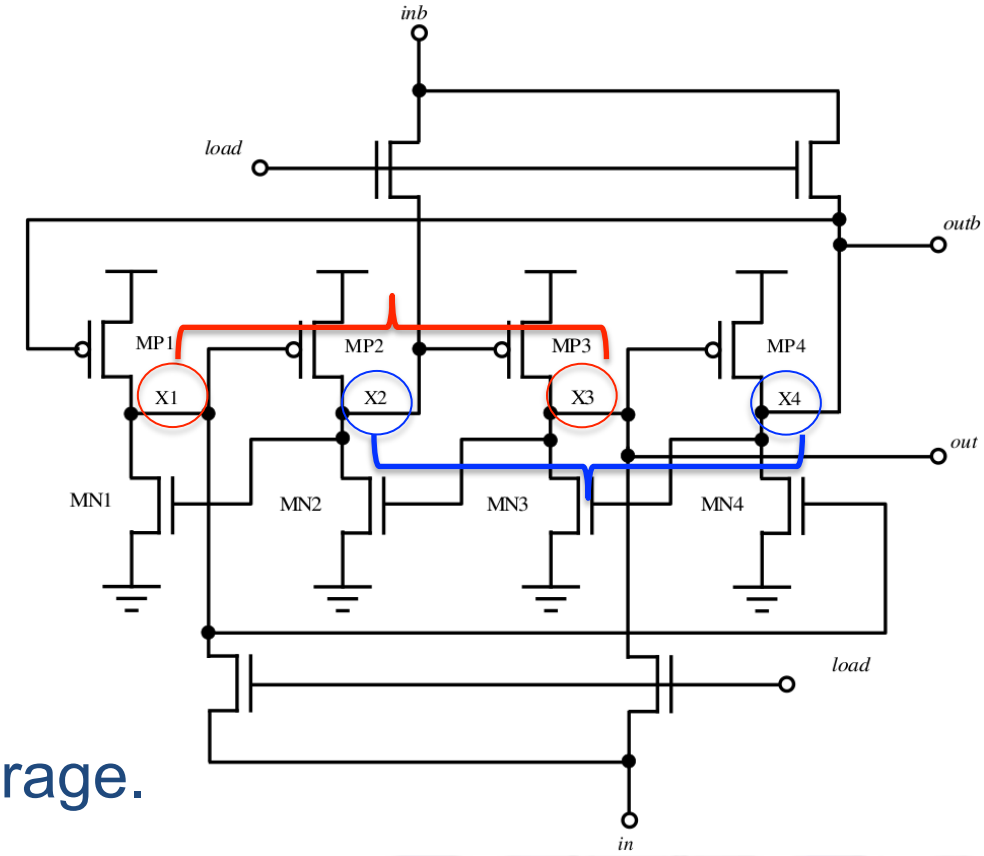
How to make FE-I4 more SEU-tolerant?

Up to ~10^{13} hadrons (E>20 Mev) cm^{-2} fb^{-1} according to PYTHIA/FLUKA simulations.

- Configuration memories based on Dual Interlock Cells (DICE) to mitigate effects of SEU (**smaller capacitance/voltage** for the 130 nm feature)

  ➔ node storage redundancy.

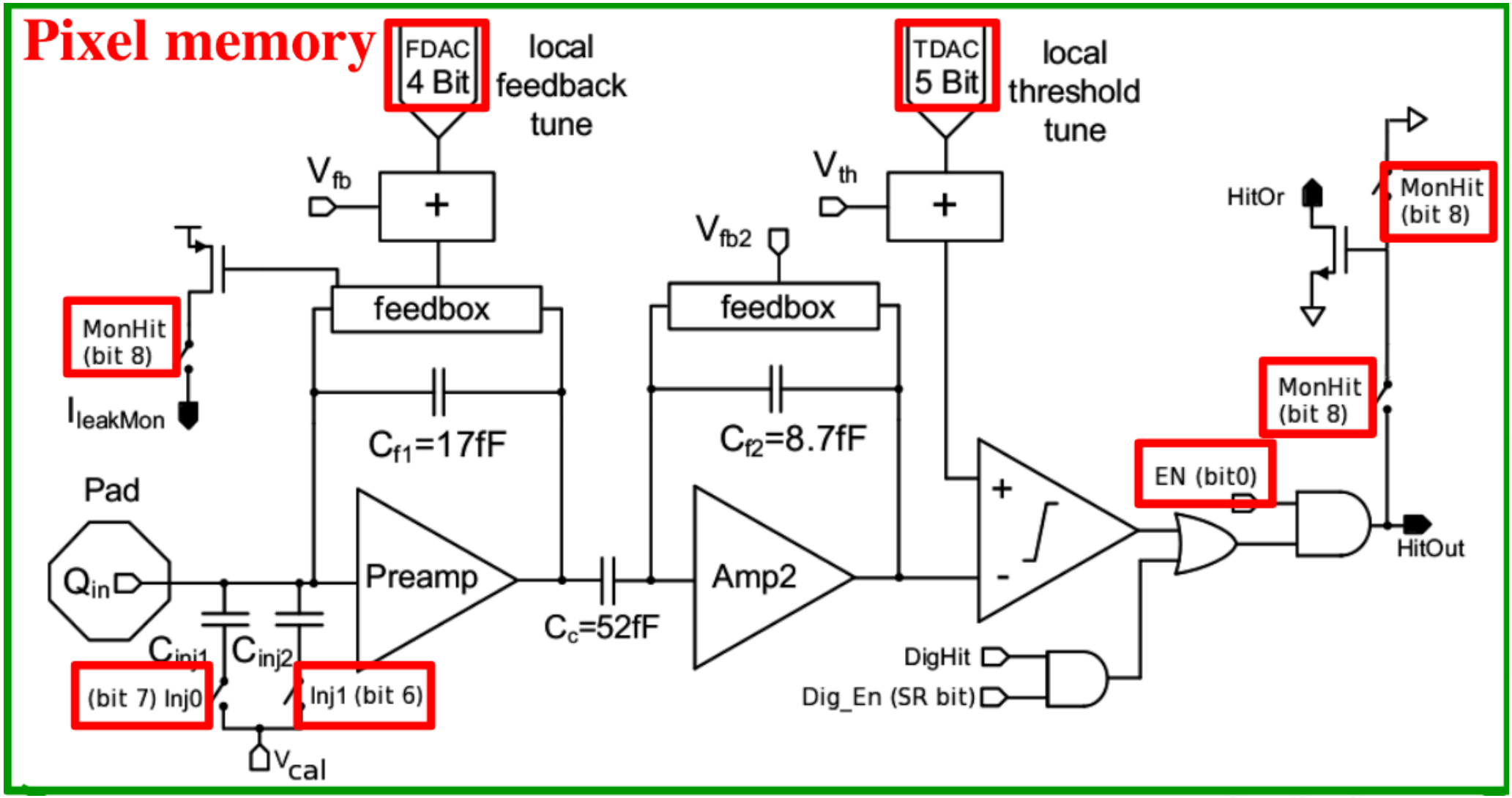
  DICE latch structure ➡



- Charge sharing between adjacent nodes can corrupt data in latches:
  ➔ custom layout design strategies to mitigate such effect …
  ➔ **hardened by design (HDB).**
- Hamming coding data buses and storage.
- Radiation burst detection circuitry if dose exceeds 100 MRad/s.
  ➔ hard reset triggered.

Local pixel registers

Local Pixel Registers: **13 DICE latches per each pixel (12 millions pixels in the entire IBL)**



Local pixel registers

Local Pixel Registers: 13 DICE latches per each pixel (12 millions pixels in the entire IBL)

PxStrobes	Latch controlled in the pixel
[0]	**Output Enable (1 bit)**: set to 1 to include pixel in read-out (enabled pixels) set to 0 to digitally mask the pixel (noisy pixel)
[1:5]	**TDAQ or local Threshold DAC (5 bits)**: single pixel threshold.
[6]	**Large Injection Capacitor (1 bit):** set to 1 to enable charge injection through big capacitor; set to 0 otherwise.
[7]	**Small Injection Capacitor (1 bit):** set to 1 to enable charge injection through small capacitor; set to 0 otherwise.
[8]	**Imon/HitBus(1 bit):** set to 1 to monitor the leakage current set to 0 to include pixel in HitBus logic
[9:12]	**FDAQ or local Feedback DAC (5 bits)**: single pixel feedback.

Used only during Calibration

Indirect impact on noise in data taking..

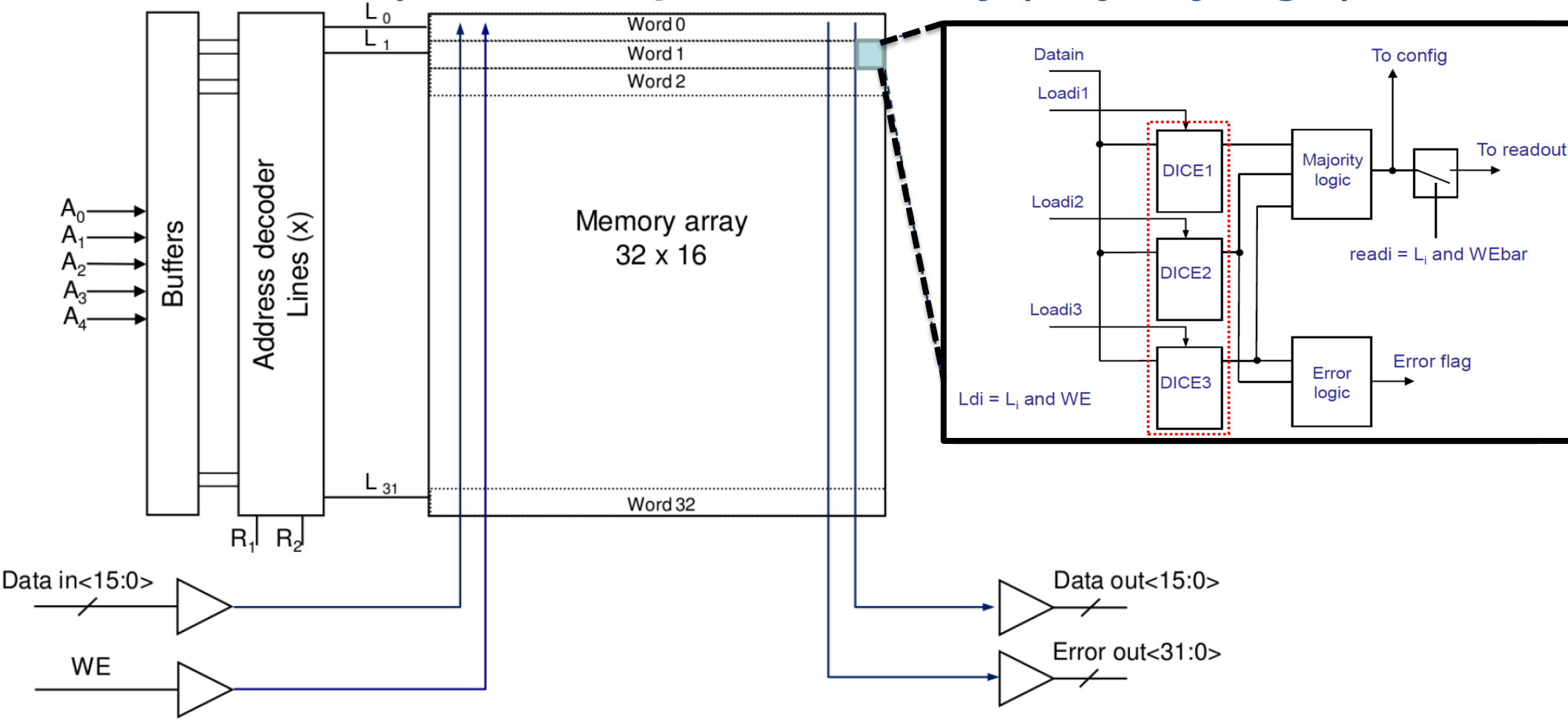
Pixel registers that can have a direct impact in data taking efficiency!

Global chip registers

Global Chip Configuration: RAM block of 32 words of 16 bits each.

- Extra protection added for the global memory (not possible due to space limitation in single pixel):

  ➔ each memory cell has **triple redundancy (majority logic).**

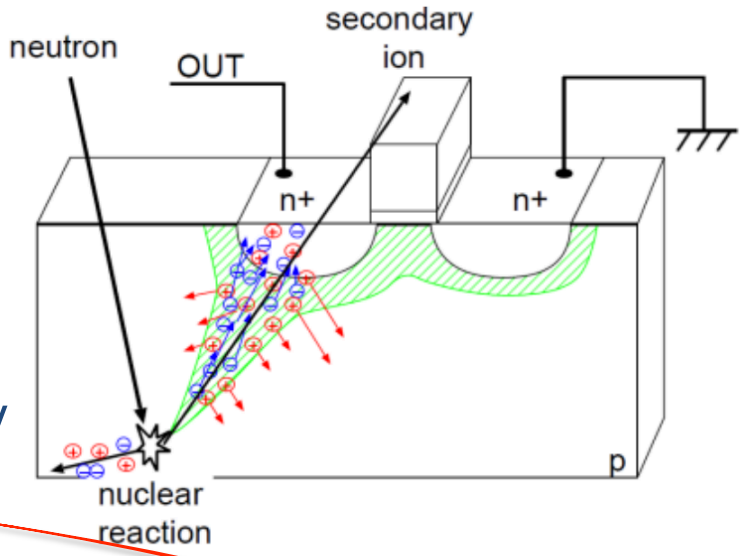


Single Event Upset/Transient

Single Event Upset (SEU)

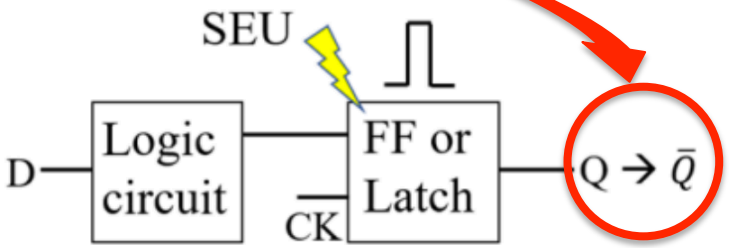
- Circuit with two stable states, 0 or 1 (latch), used to store each configuration bit.
- A relevant amount of charge into a latch **can flip its logic state.**
- In case of highly ionizing recoil nuclei and showers from nuclear interactions of the MIPs in the proximity of the memory cells:

➔ **memory corruption.**



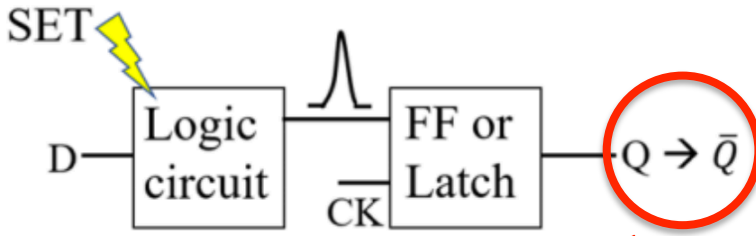
Single Event Transient (SET)

- Transient pulse caused by single event effect (SEE) that propagates in a combinatorial circuit path and eventually be latche in a storage cell.



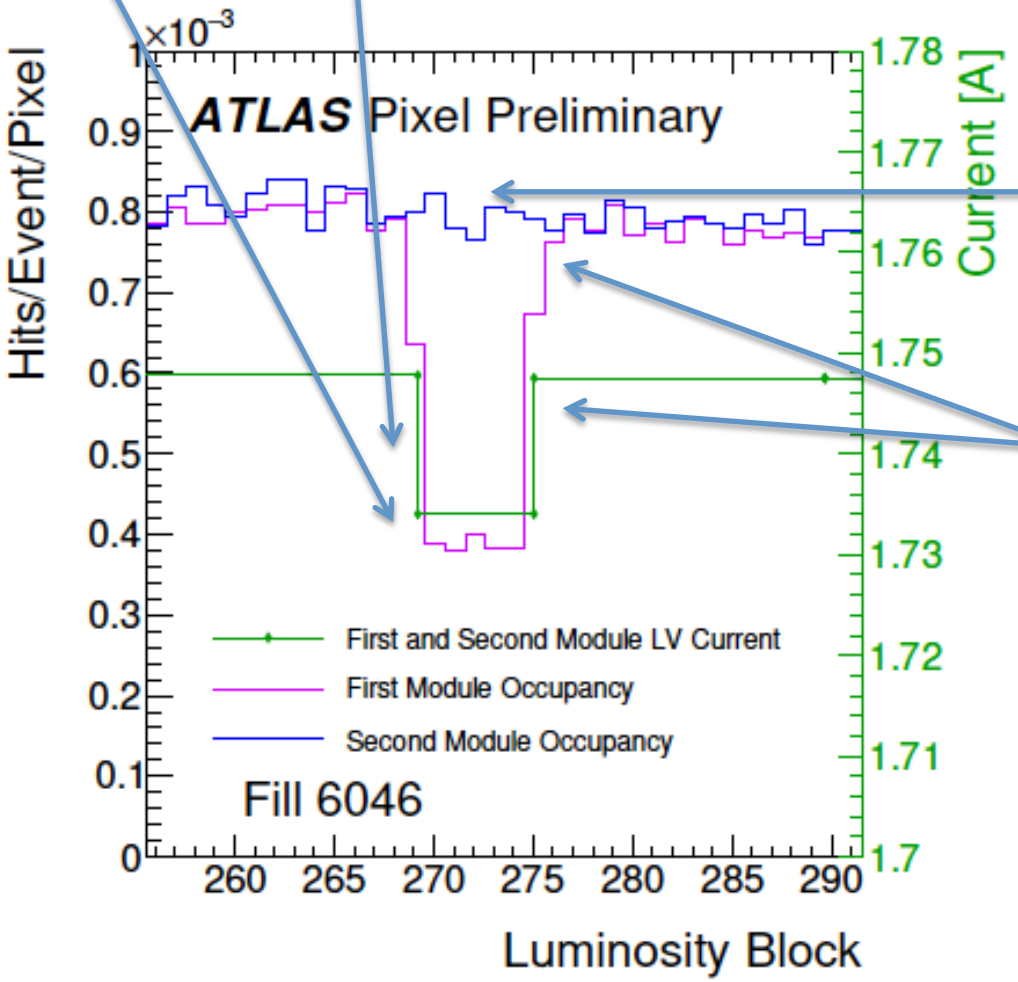
- Glitch on the “LOAD” line of Shift Register (SR):

➔ **memory corruption.**



Global registers SEU/SET effects

- Global register SEU/SET has a strong impact on module operation.
- Both Low Voltage (LV) current consumption and module hit occupancy can be affected.

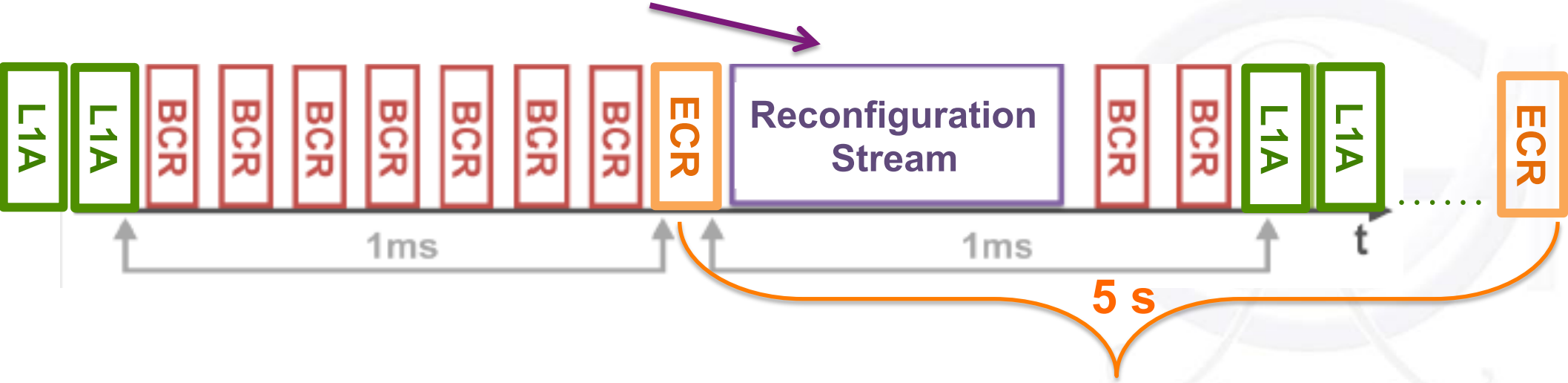


- LV current consumption serves two DAQ modules in IBL:
  - one of the DAQ module was not affected in this case.
- Corrective actions taken to restore the correct operation:
  - module reconfiguration.

Fill from Aug. 2017
Max Luminosity 1.50 x 10^{34} cm^{-2} s^{-1}

Automatic chip reconfiguration

- For convenience, it was decided to perform a **regular reconfiguration of the FE-I4 GRs**.
- How often? **Every 5 s**…Why?
- ATLAS sends to sub-systems Bunch Counter Reset (BCR) every LHC beam revolution time (89.1 μs) and **Event Counter Reset (every 5 s)**
  ➔ keep synchronization between FEs and Off-detector readout.
- Time window of 2 ms available at each ECR
  ➔ decided to **use this "space" without adding extra dead-time**!



- Joint effort of Sw and Fw ➔ deployed successfully in summer 2017.

Single pixel register SEU effects

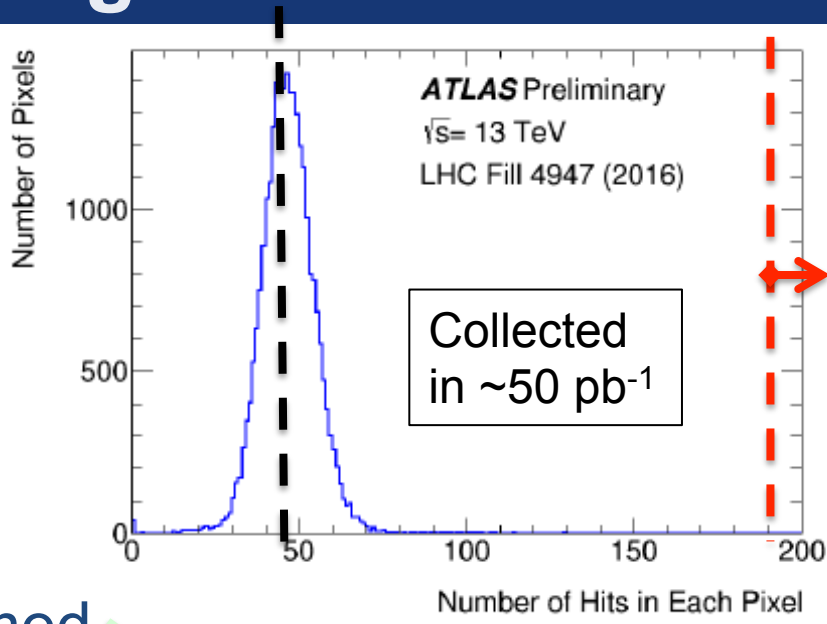
Despite the GR reconfiguration..

- increase of **noisy pixels** (up to +30% average hit occupancy) during the fill

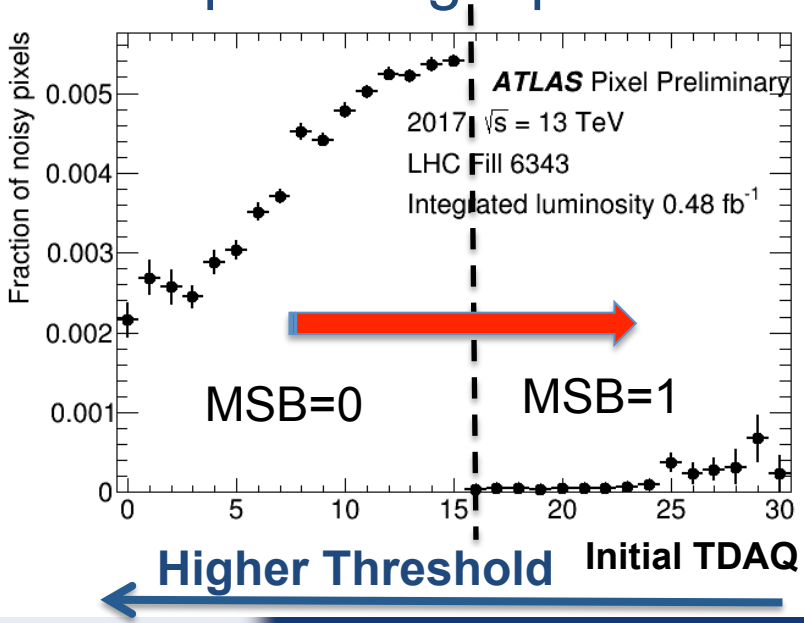
  $\langle hits \rangle_{pixel/50\ pb^{-1}} = 47$

  Noisy pixel if: $\langle hits \rangle_{pixel/50\ pb^{-1}} > 200$

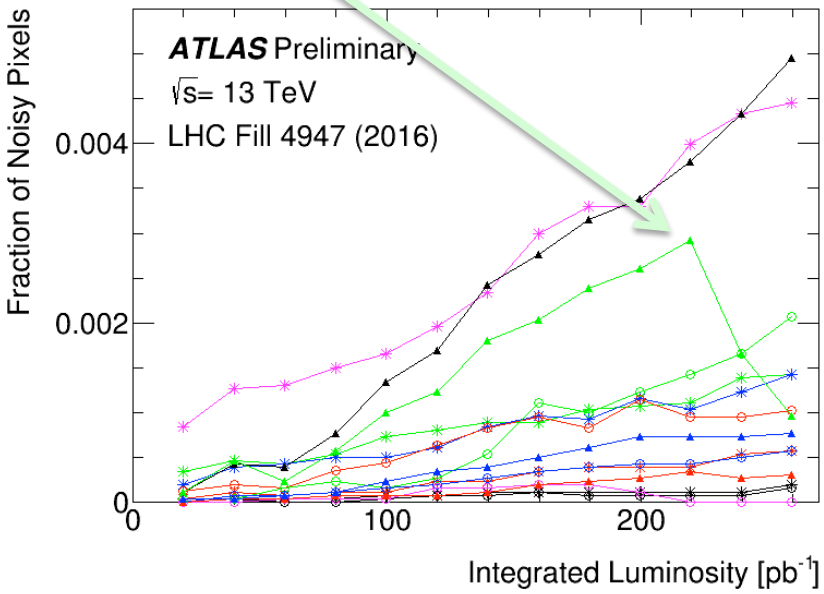
- noise disappears if full FE-I4 reconfig (**including single pixel registers**) performed.



➔bit flip on single pixel threshold (TDAQ) seems to be the main cause.

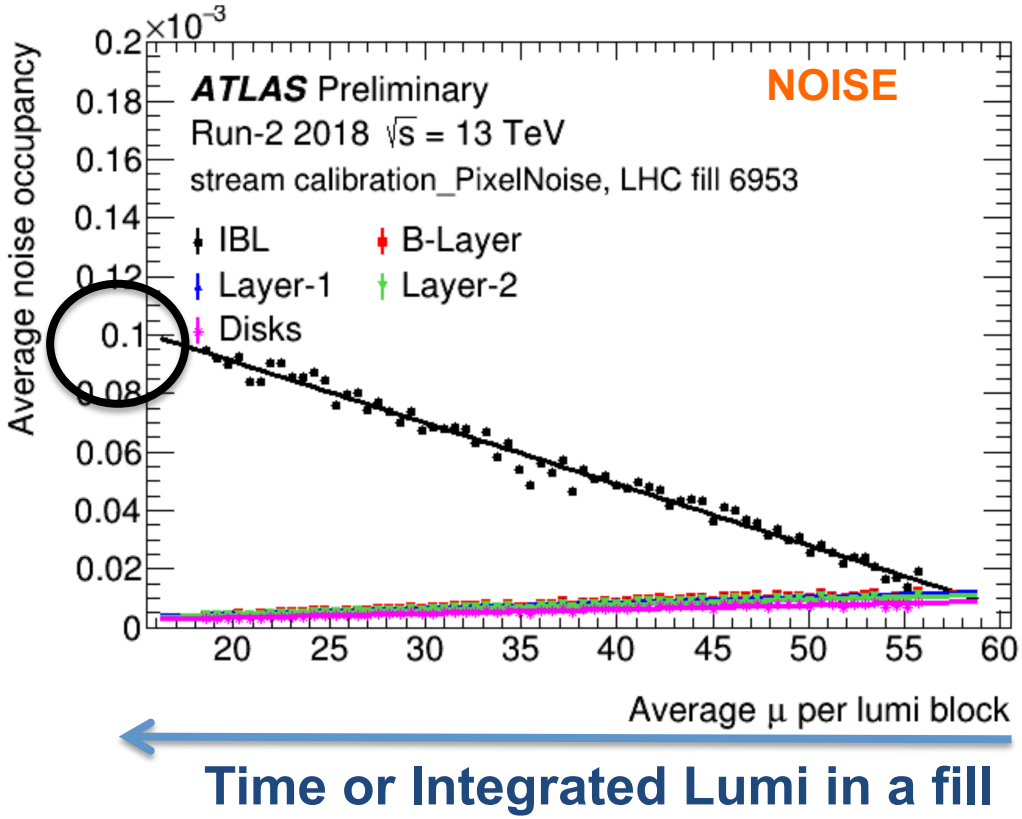


Bit flip in TDAQ MSB (0→1) implies a big decrease of threshold!

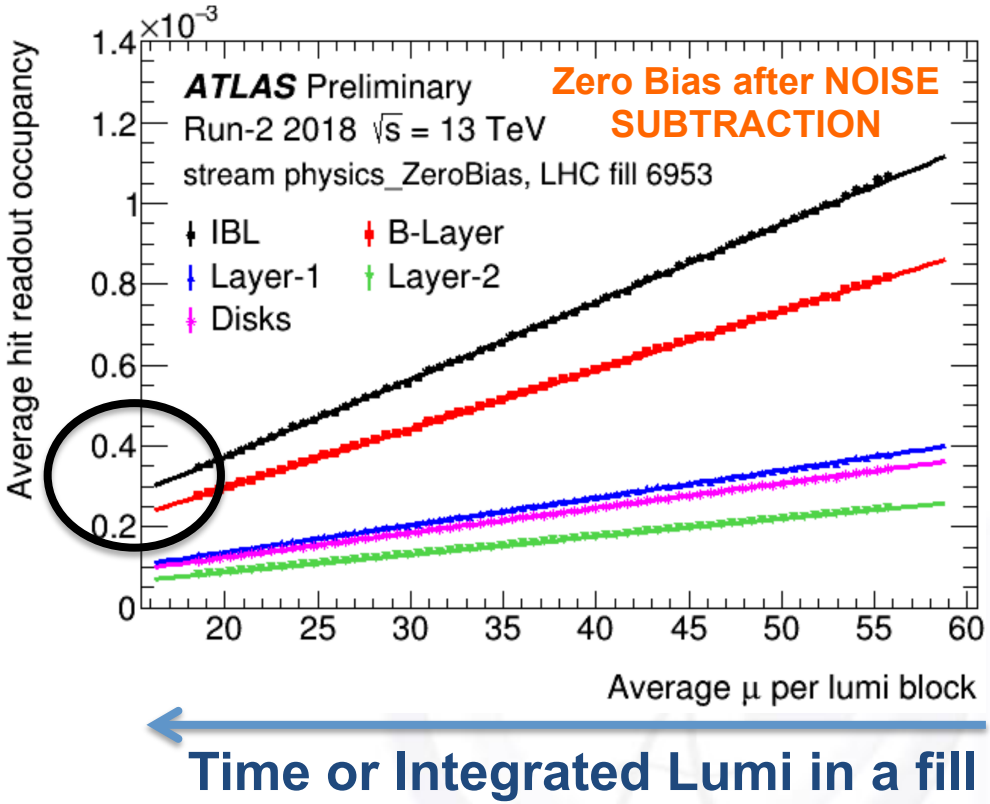


Other way of looking at noise

- Check the average hit occupancy in the empty bunches (~10^{-5}).
- Distribution increase only for IBL (effect not present in other layers) as a function of time: μ (pile up) decreasing along a fill.



Time or Integrated Lumi in a fill



Time or Integrated Lumi in a fill

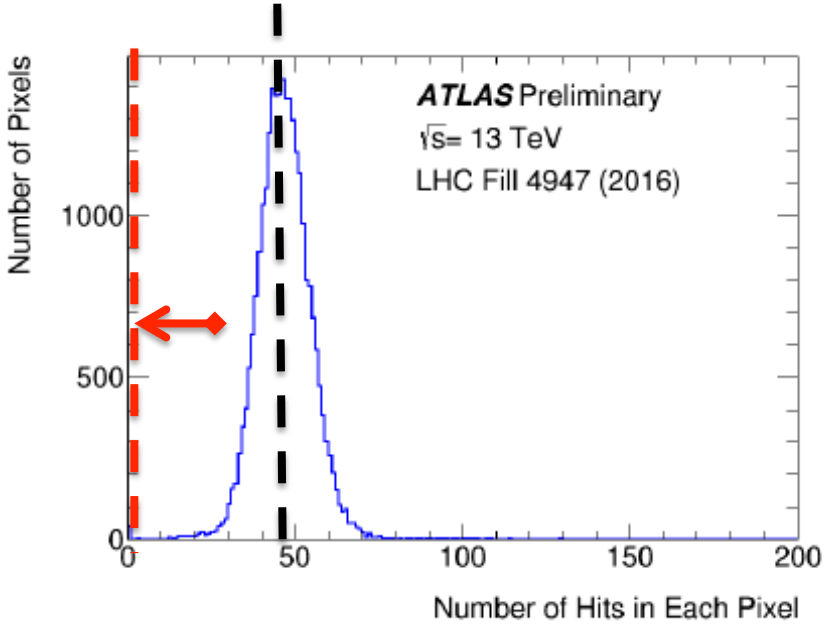
- Artificial increase of occupancy present also in filled bunches (Zero bias).
- At the end of a fill, this corresponds to an extra ~ 30% of occupancy.

Single pixel register SEU effects

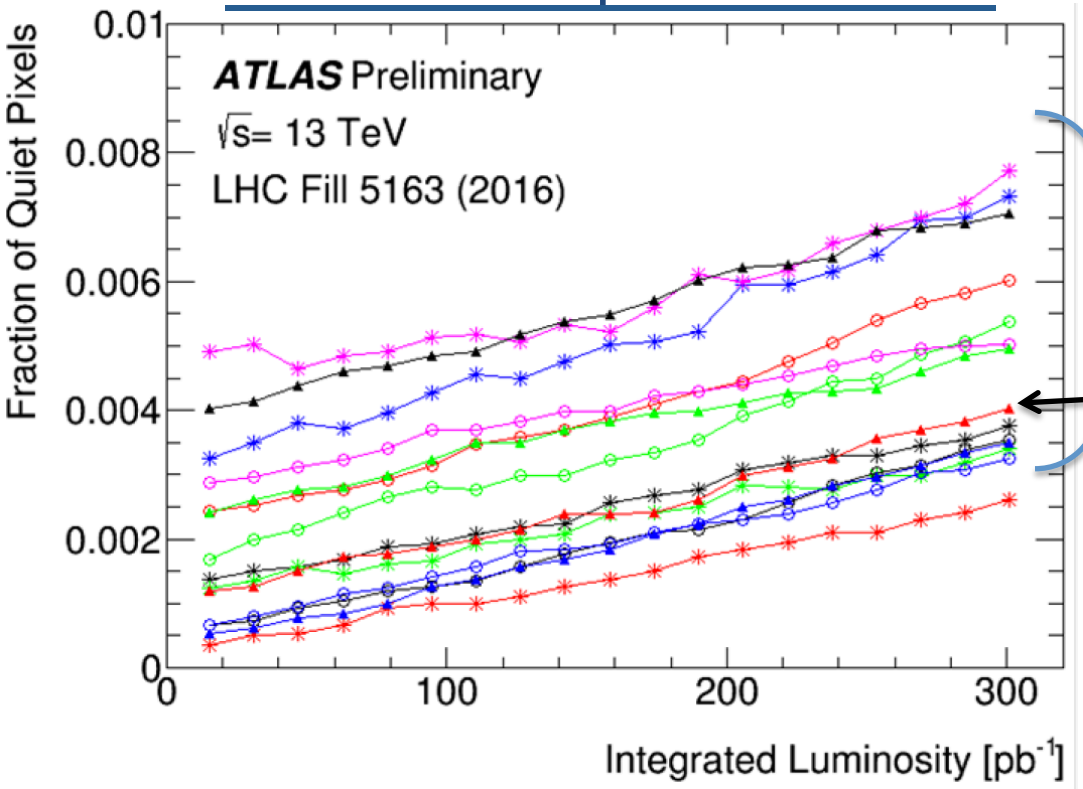
- Similar effect was observed with an increasing of **quiet pixels** (up to 1% of pixels disabled) during the fill.

$$\langle hits \rangle_{pixel/50\ pb^{-1}} = 47$$

Quiet pixel if: $\langle hits \rangle_{pixel/50\ pb^{-1}} = 0$



Enable bit flips from 1 → 0



- Similar behavior observed for different FEs at **different η region**.

Test beam results.

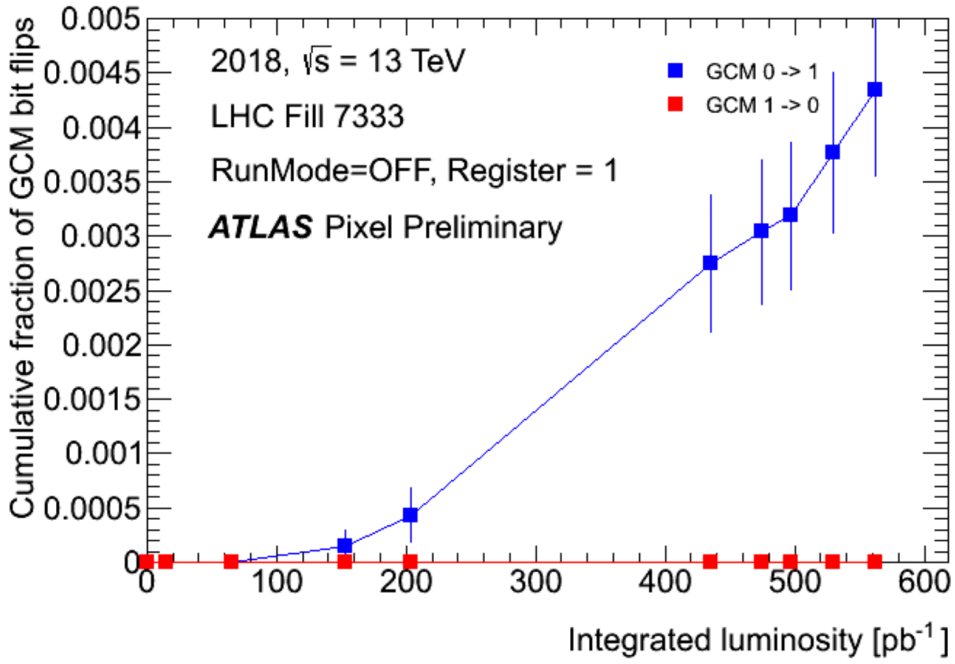
- Typically **~10 $^{-3}$ pixel/FE-I4** masked (disabled.. or masked) at the start of the Run.

Quantifying bit flips in GR

- Exploiting FE-I4 functionality to read-back GR and local pixel laches during a fill:
  - 12 FEs under tests, disabled from the start of the run, no-reconfig
  - 3D modules…out of tracking acceptance ➔ no impact on physics.
- Registers read-back performed several times before and during the fill.
- Shift registers were always reloaded with “1” during the tests:

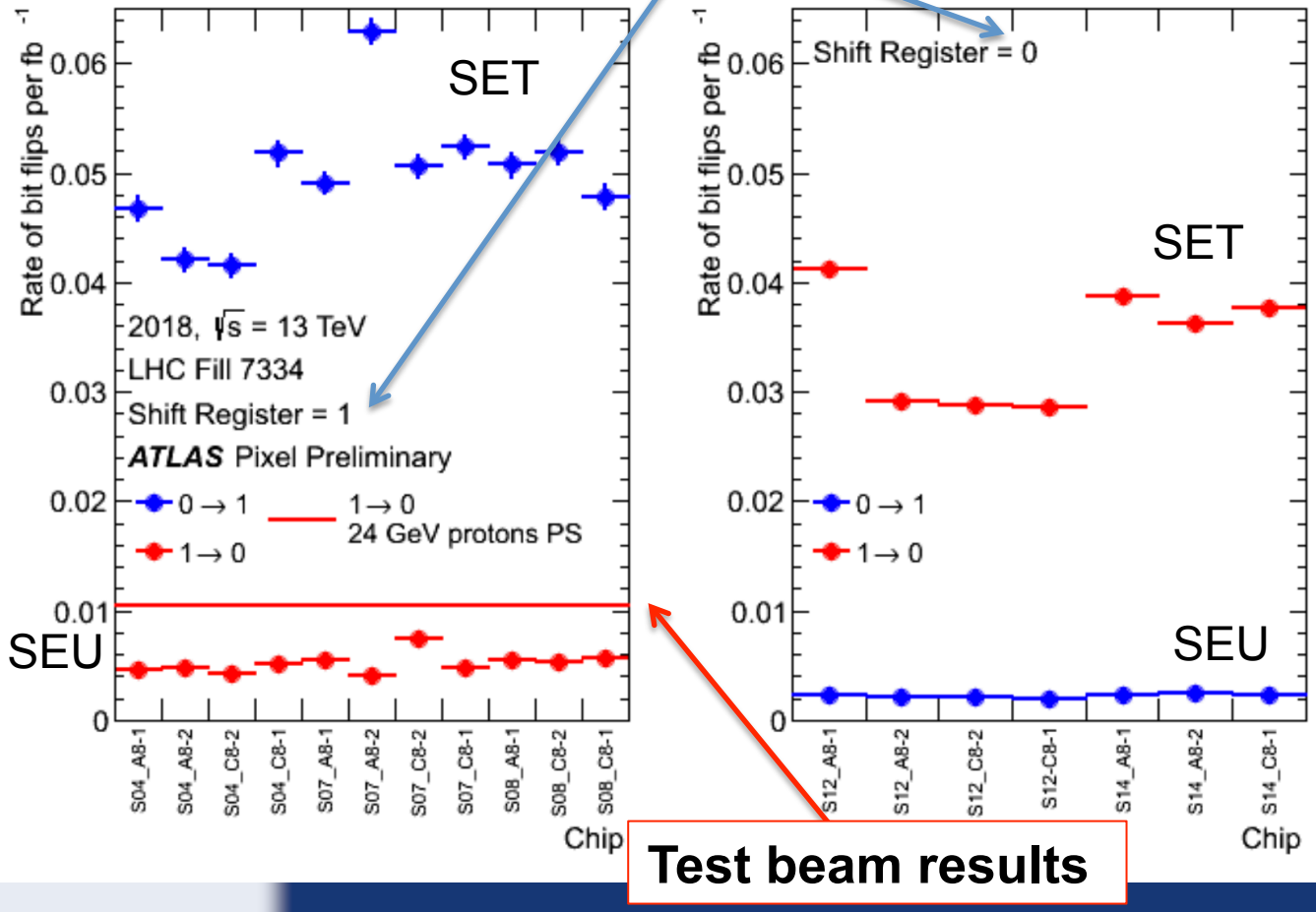
➔ much higher rate of 0→1 transitions (SET glitches) respect to 1→0 transitions (memory SEU).

➔ triple redundancy with majority logic in FE-I4 global memories seems to work!

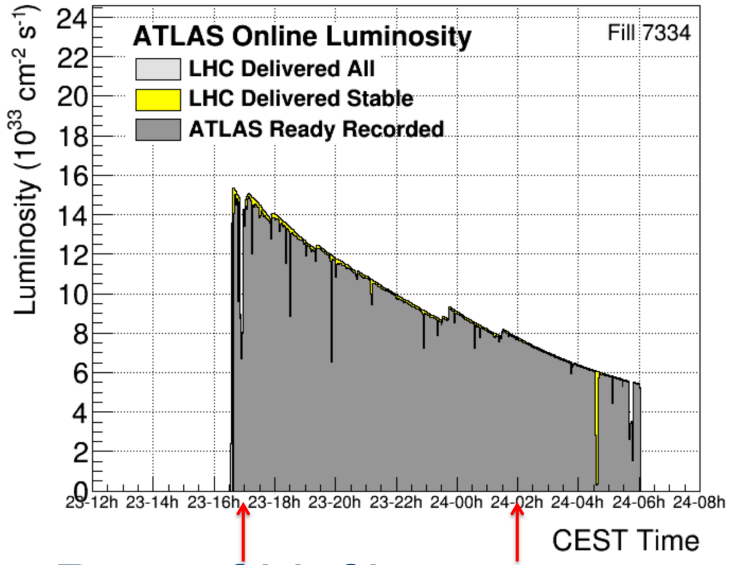


Local pixel register read-back

- Similar exercise for local pixel register read-back:
  - only two readings for this test
  - some FE-s loaded with **1** in the shift register
  - some FE-s loaded with **0** in the shift register



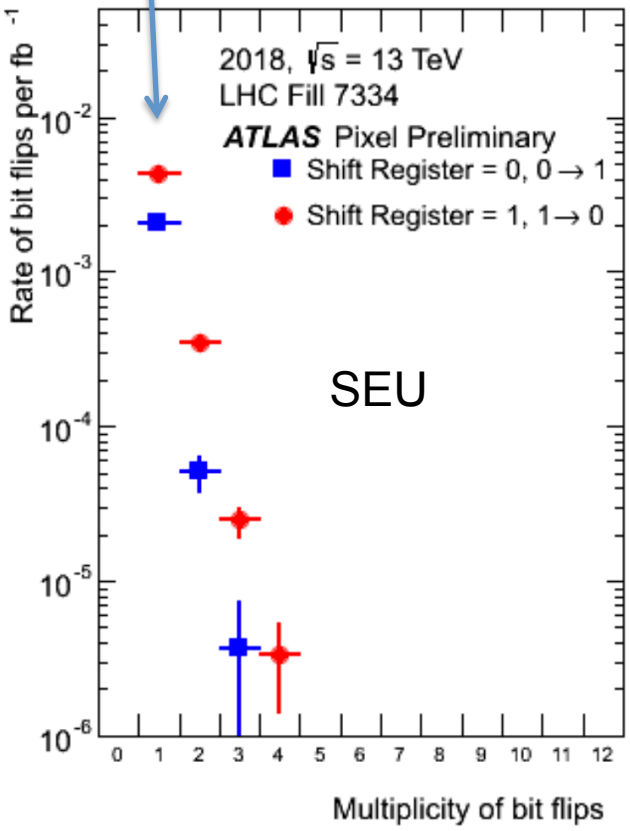
Test beam results

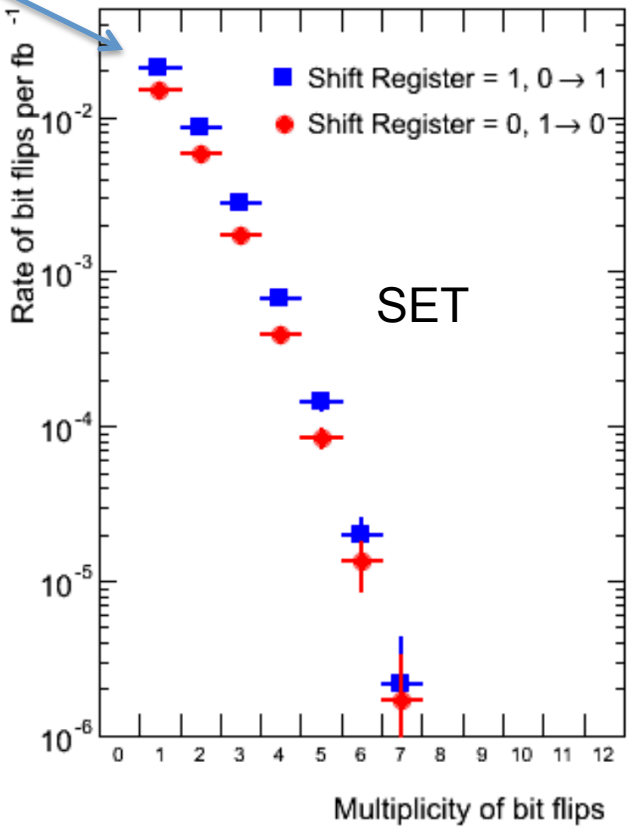


- Rate of bit flips mostly from SET (glitches) on the LOAD lines:
  - SR = **1** : 0→**1**
  - SR = **0** : 1→**0**
- Lower rate due to real memory SEU:
  - SR = **1** : 1→**0**
  - SR = **0** : 0→**1**

Rate of (multiple) bit flips

- Multiple bit flips (more than one latch flipped) per single pixel could indicate a glitch on the common LOAD line
  ➔ distribution peaked at one bit flip per pixel
    ➔ glitch on the LOAD line mainly related to individual DICE latch.
- Long tail in the multiplicity
  ➔ probably small contribution from glitches common to several bits.





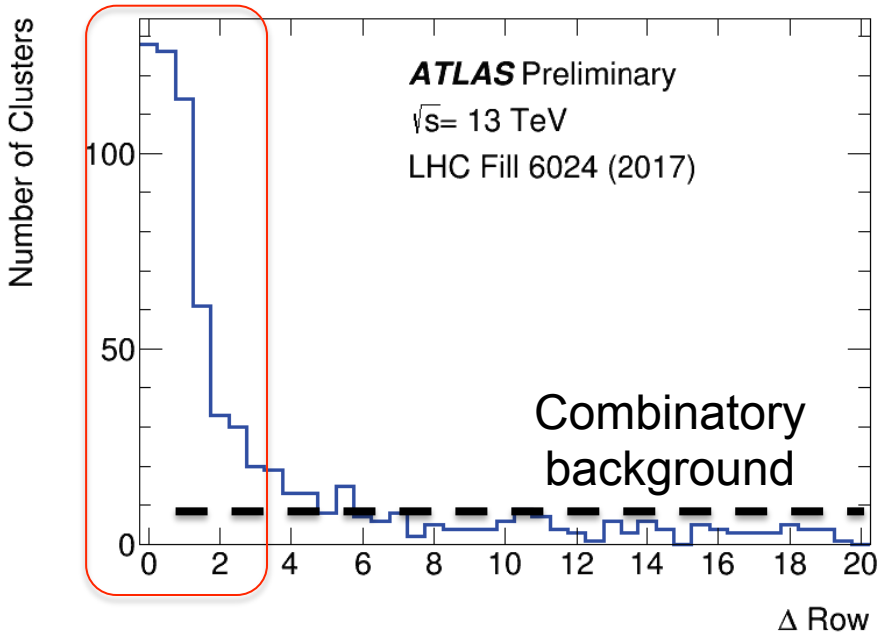
- Differences between the opposite transition: “chip to chip” process variations, tuning and particle flow differences.

Integrated luminosity:
0.35 fb^{-1}
Mean luminosity:
$1.1 \cdot 10^{34}$ cm^{-2} s^{-1}

Broken cluster studies

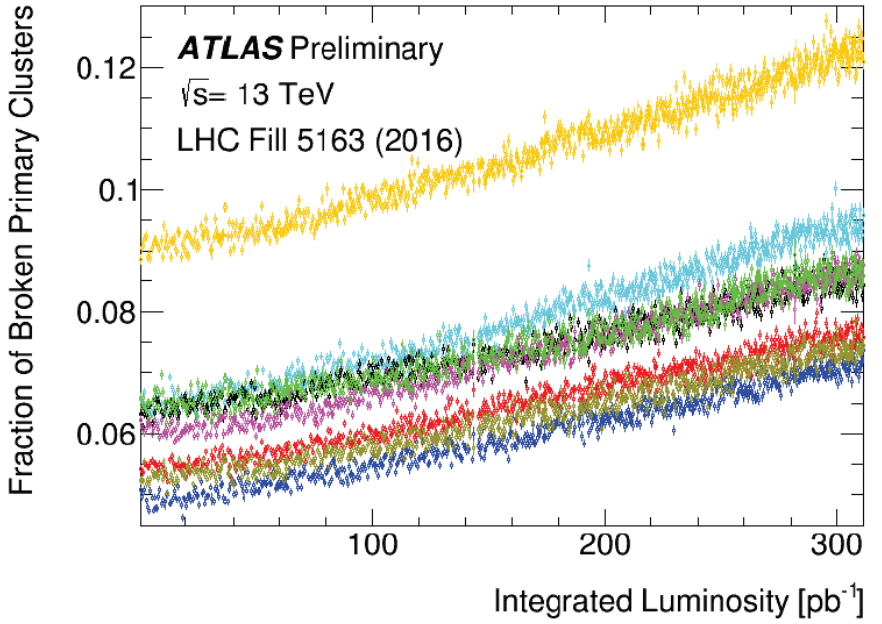
- Quiet pixels can lead to long clusters getting split by the clustering algorithm

  ➔ **broken clusters** meaning two clusters with 1-pixel gap along z-direction and $\Delta_{row} < 3$ where Δ_{row} = center-to-center cluster distance in r-φ plane



- Flat combinatory background, number of broken clusters from Δ_{Row} fit.

- Linear increase with integrated luminosity
  - initial offset represents the number of disabled/dead pixels.



SEU mitigation tests

- Thread on the PowerPC Sw (ROD FPGA embedded system) that fills the off-detector FIFOs (1 per each module) with different content before each ECR.
- Not enough time during ECR (1 ms time window) to fully reconfigure all the pixel memories in the entire module

  ➔ the content will depend on the ECR number

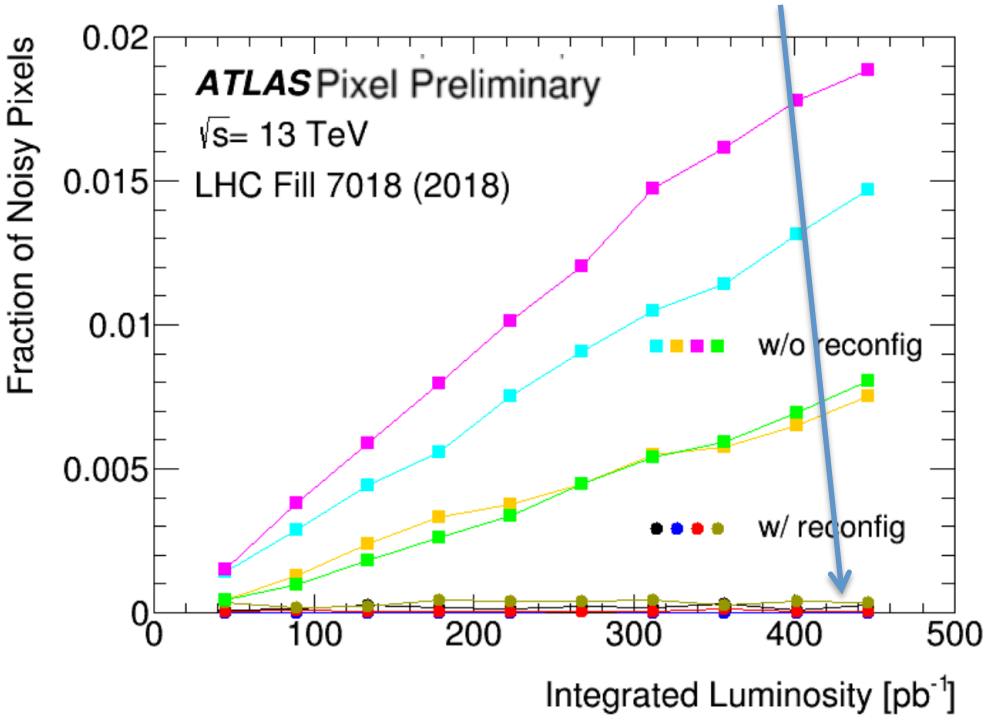
  ➔ configuring only one FE-I4 Double Column (only **1 out of 40 DC**) per module.
- Sets of measurements with current probe in our test lab to establish the intensity and frequency of the current spikes induced by the reconfiguration commands:
  ➔ decided to reconfigure not more than **3 out of 13 latches** each time.
- The full detector being reconfigured after **~130 ECRs → ~11 minutes**

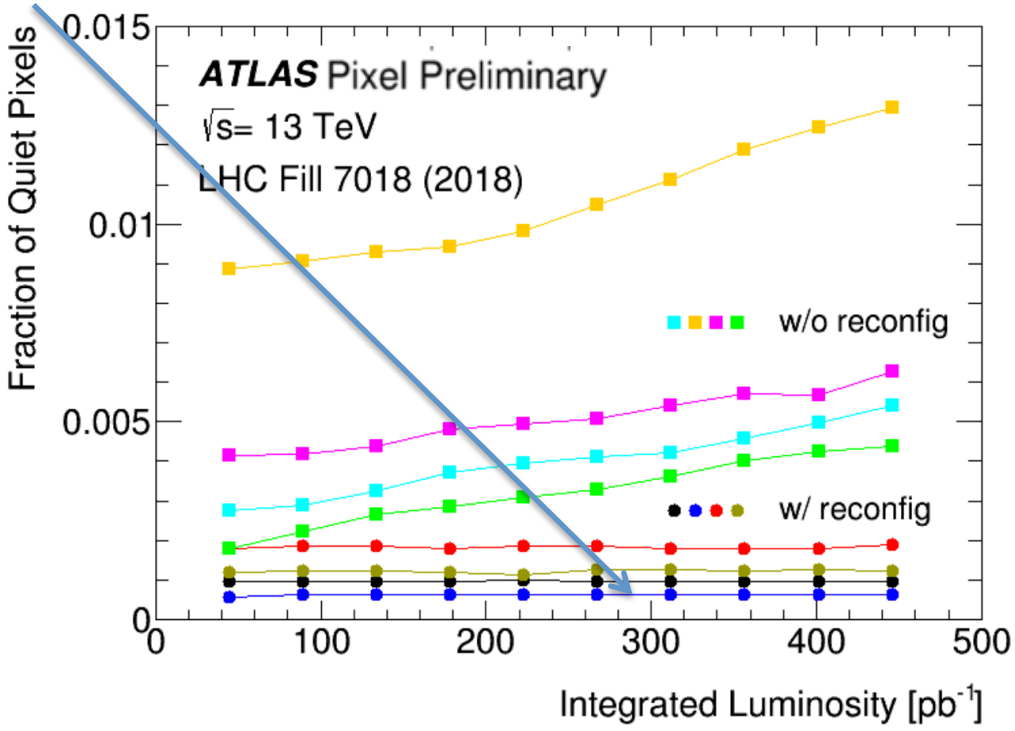
  ➔ anticipation of the ITK trickle reconfiguration concepts.

Test reconfig in local pixel registers

- Activated in few test runs (not completely deployed due to SW instabilities).
- The full reconfiguration process takes 11 minutes.
- Only 4 3D modules rings were reconfigured (the other 4 were not reconfigured and used as a reference)

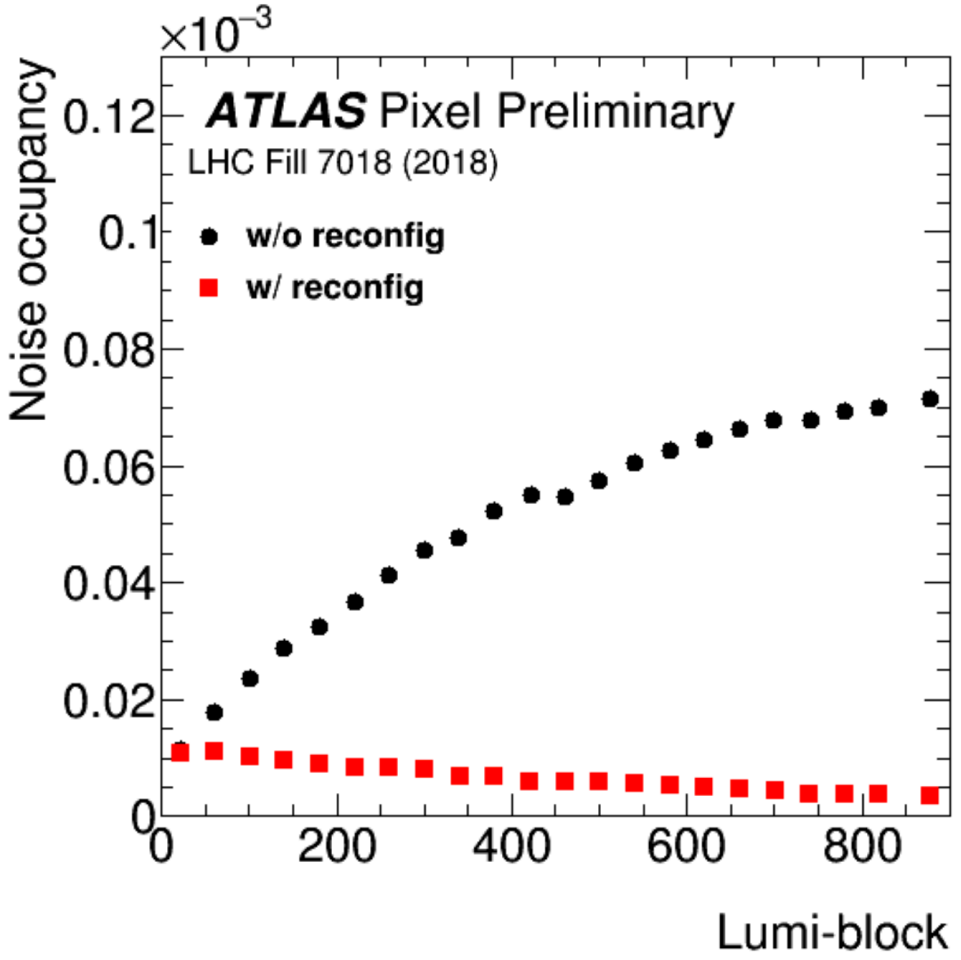
➔ **stable number for fraction of noisy and quite pixels!**





Test reconfig in local pixel registers

- Similar positive effect visible on the noise occupancy stream (hit occupancy in empty bunches)
- Overall noise with pixel-reconfig active is actually decreasing as a function of time (1 Lumi-Block = 60 s)
  - slight dependency on the colliding bunches luminosity (>=5 BC earlier)

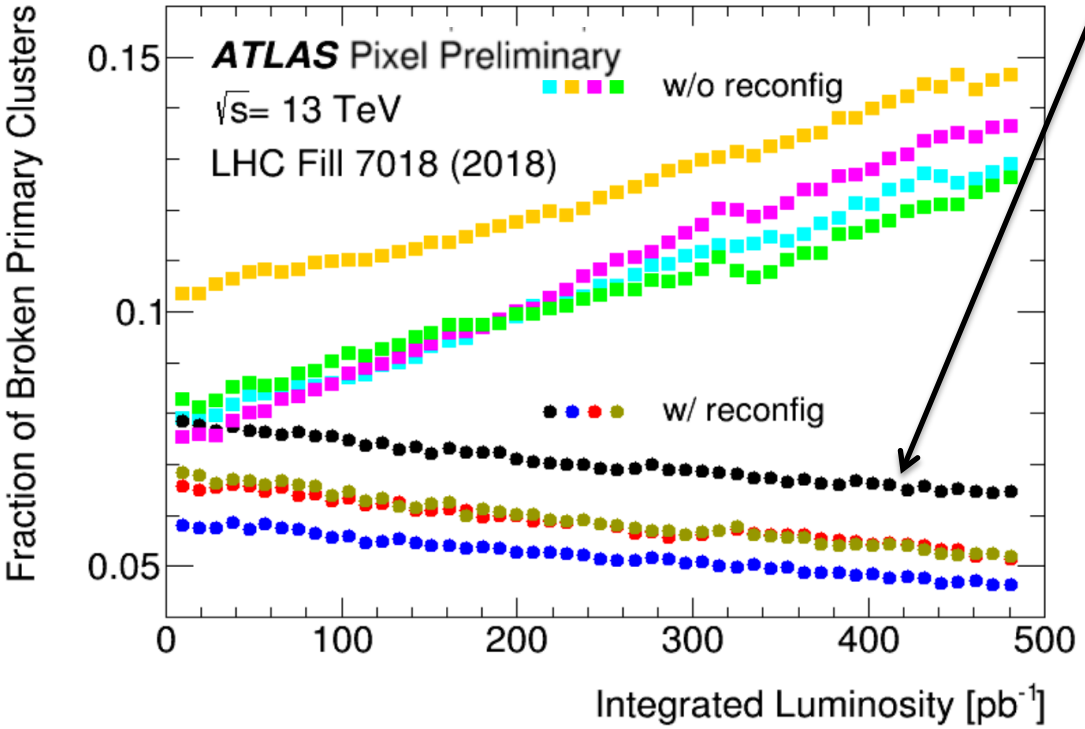


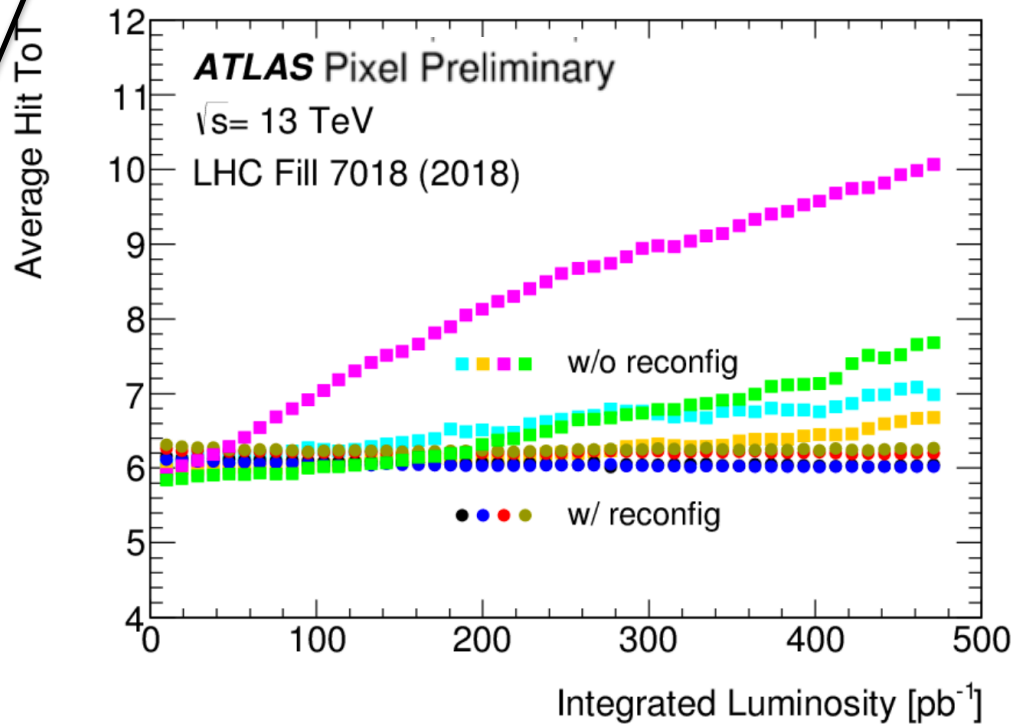
Test reconfig in local pixel registers

- Effect visible also on the fraction of broken clusters.
- More time is needed to collect an XX amount of luminosity when the instant luminosity is lower (typically at the end of the fill)

  ➔ more reconfigurations happening in such integrated luminosity bins.

  ➔ decreasing trend as a function of integrated lumi.
- Effect on Time Over Threshold (TOT) of the pixel hits also visible.

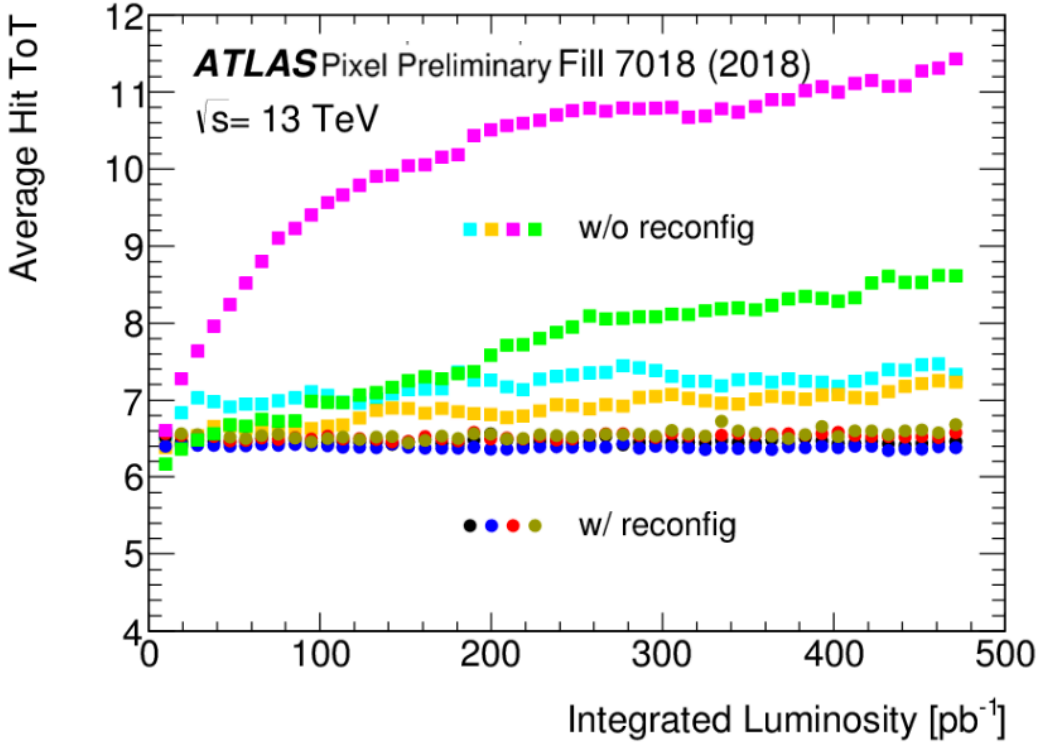


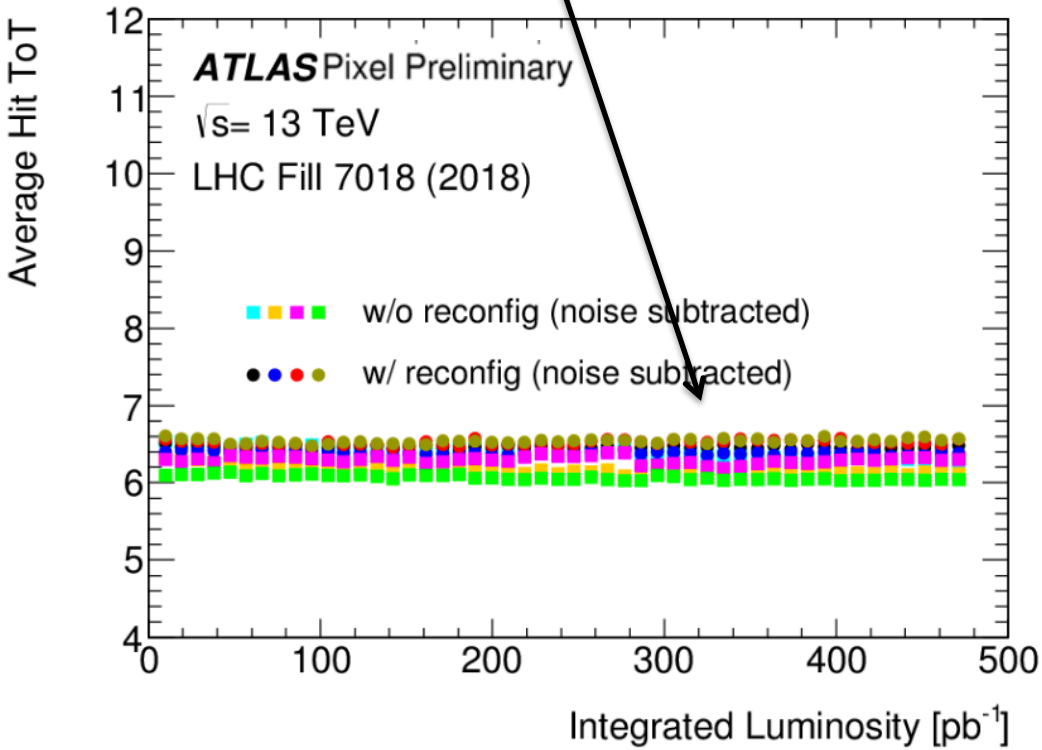


Effect of noise increase

- A drift of the TOT could be also coming from de-tuning of FDAQ registers (feedback regulators).

- In reality, it is connected to noisy hits that distorts the average TOT distribution ➔ flat distribution after noisy hits subtraction!



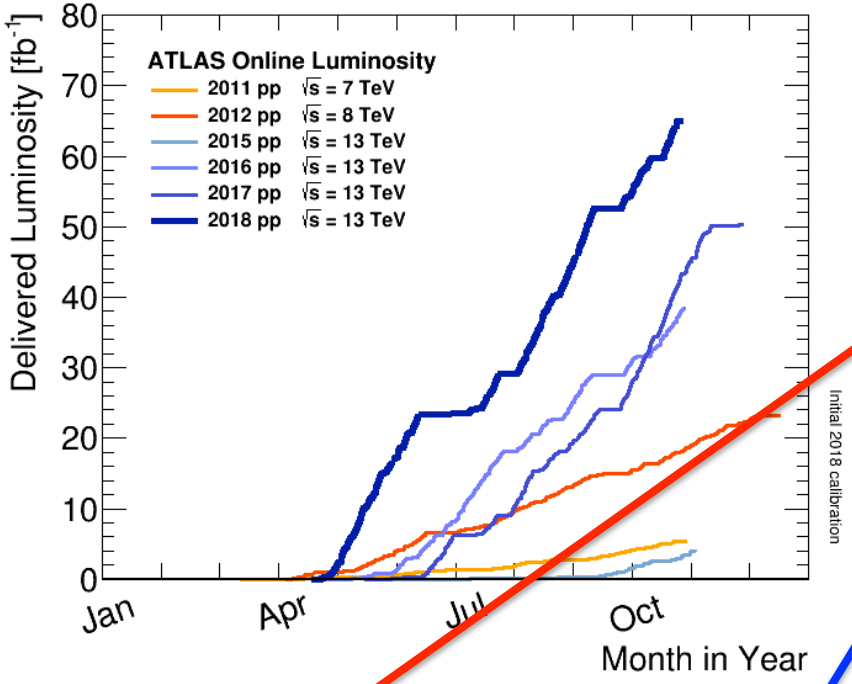


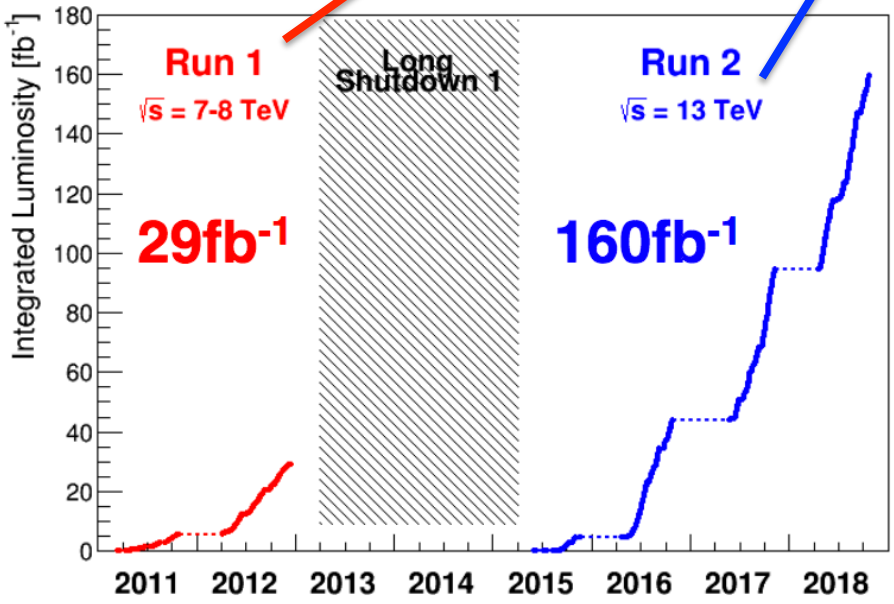
Conclusions and future plans

- IBL FE-I4 affected by SEU/SET for global and single pixel registers.
- **Impact** on data taking mostly **coming from global register** upset.
- Pixel memory read-back results confirms that the FE-I4 SEUs are dominated by **SET (glitches) that create fake "LOAD" signals**:
  - 0 ➔ 1 flips dominating when SR loaded with "1"
  - 1 ➔ 0 flips dominating when SR loaded with "0"
- The bit-flip multiplicity distributions are peaked at one flip per pixel ➔ glitch on the LOAD line is **mainly related to single DICE latch**.
- Clear **improvements from regular reconfiguration of the single pixel latches** during test run in 2018.
- Considering the increase of integrated lumi in Run 3 fills (longer leveling time at high luminosity/flux), **single pixel reconfiguration mandatory for a smooth FE-I4 (IBL) operation!**
- Plant to **expand to FE-I3** the periodic global register reconfiguration.
- Paper in preparation for the early spring…

Back -up

LHC Run1/Run2 working conditions

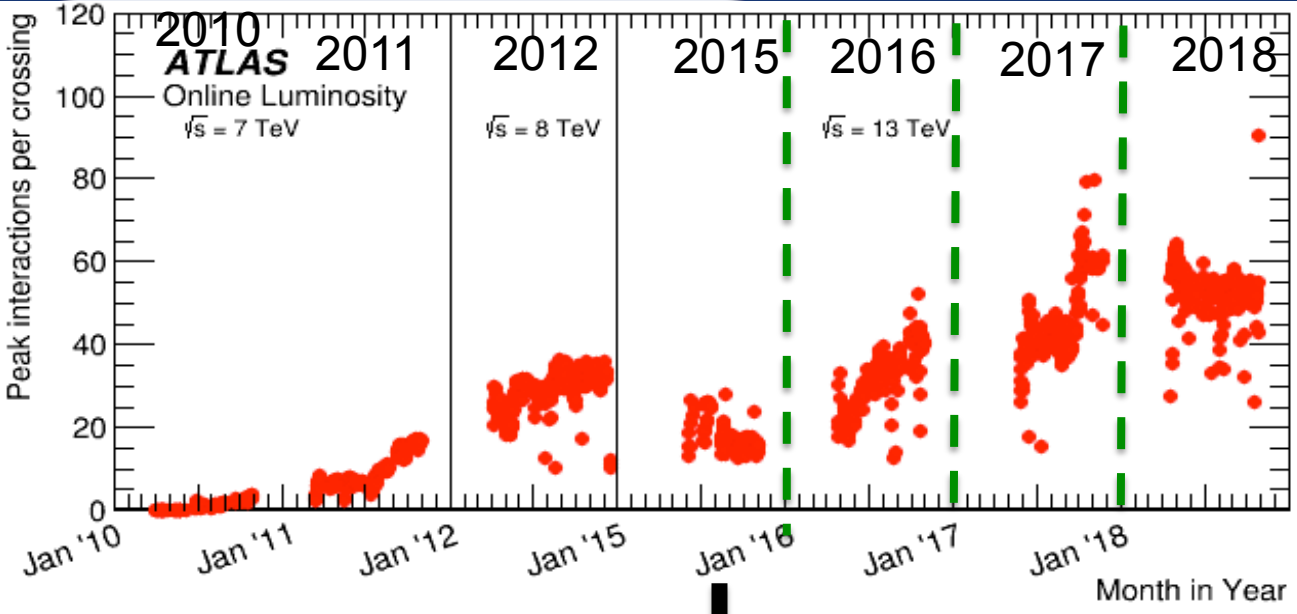


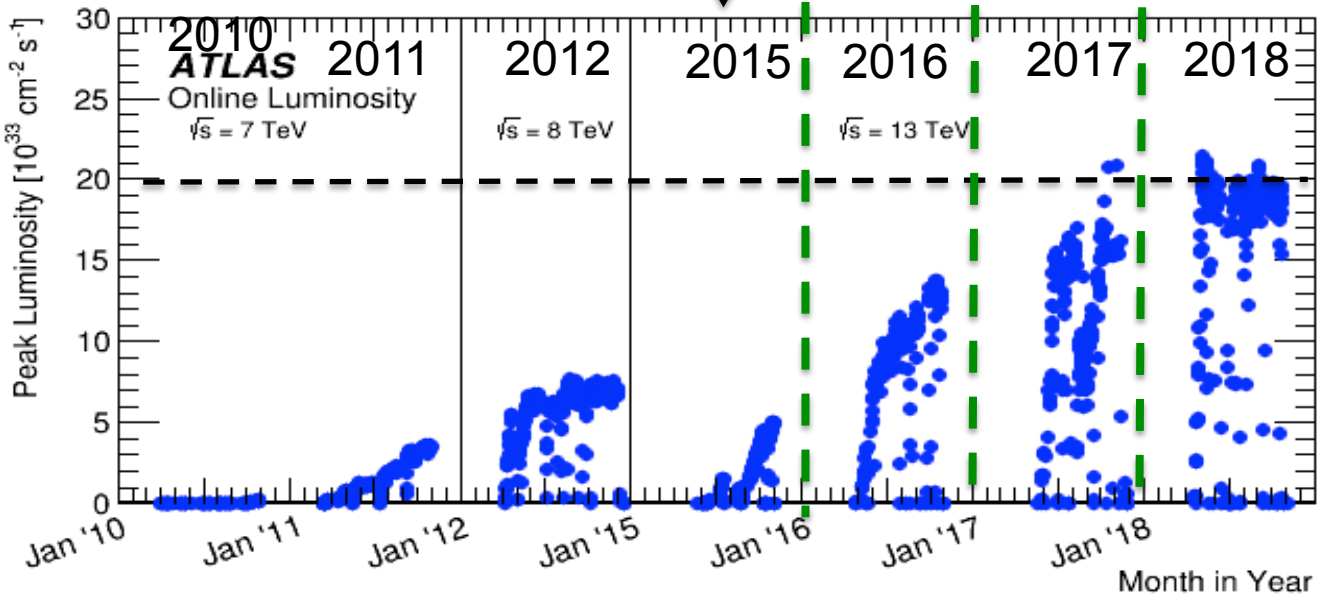


Period	Int. Luminosity [fb^{-1}]
Run 1	29.2
Run 2: 2015	4.2
Run 2: 2016	39.7
Run 2: 2017	50.2
Run 2: 2018	66
Total Run 1+ 2	189

- Increasing instantaneous luminosity:
  - up to 2-2.2 • 10^{34} cm^{-2} s^{-1}
- Bunch crossing spacing:
  - from 50 to 25 ns
- Pile-up conditions:
  - from 10 to 60 interaction per BX
- Increasing fill integrated luminosity:
  - up to 700 pb^{-1}.

Evolution of LHC parameters





If the LHC ring is fully populated…

(most of the time 2556 colliding bunches are present)

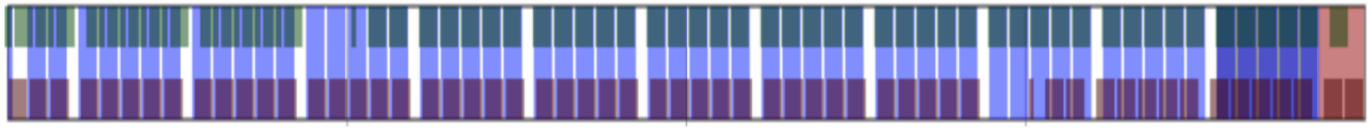
➔ **Luminosity scales with pile-up!**

Run 3 baseline

Run-III PROSPECTS	up to now	2021	2022	2023	up to triplet replacement
beam energy [TeV]		7			
integrated lumi [fb^{-1}]	**190**	25	90	120	**425**

Baseline: BCMS (OKish @ 1.8e11 p/b for 195 W/cell in high load sectors)

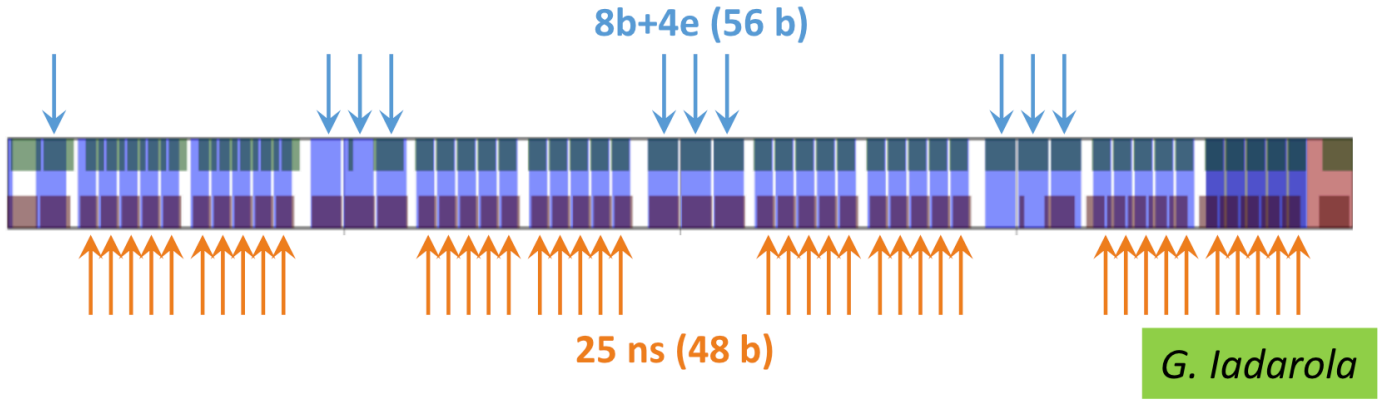
5x48 b/inj, **2736 collisions in ATLAS/CMS**, 2250/2376 in Alice/LHCb



Back-up: MIXED scheme (needed for 25% missing cryo-cooling capacity)

25ns_2492b_2484_1949_2131_240bpi_13inj_800ns_bs200n_run3study

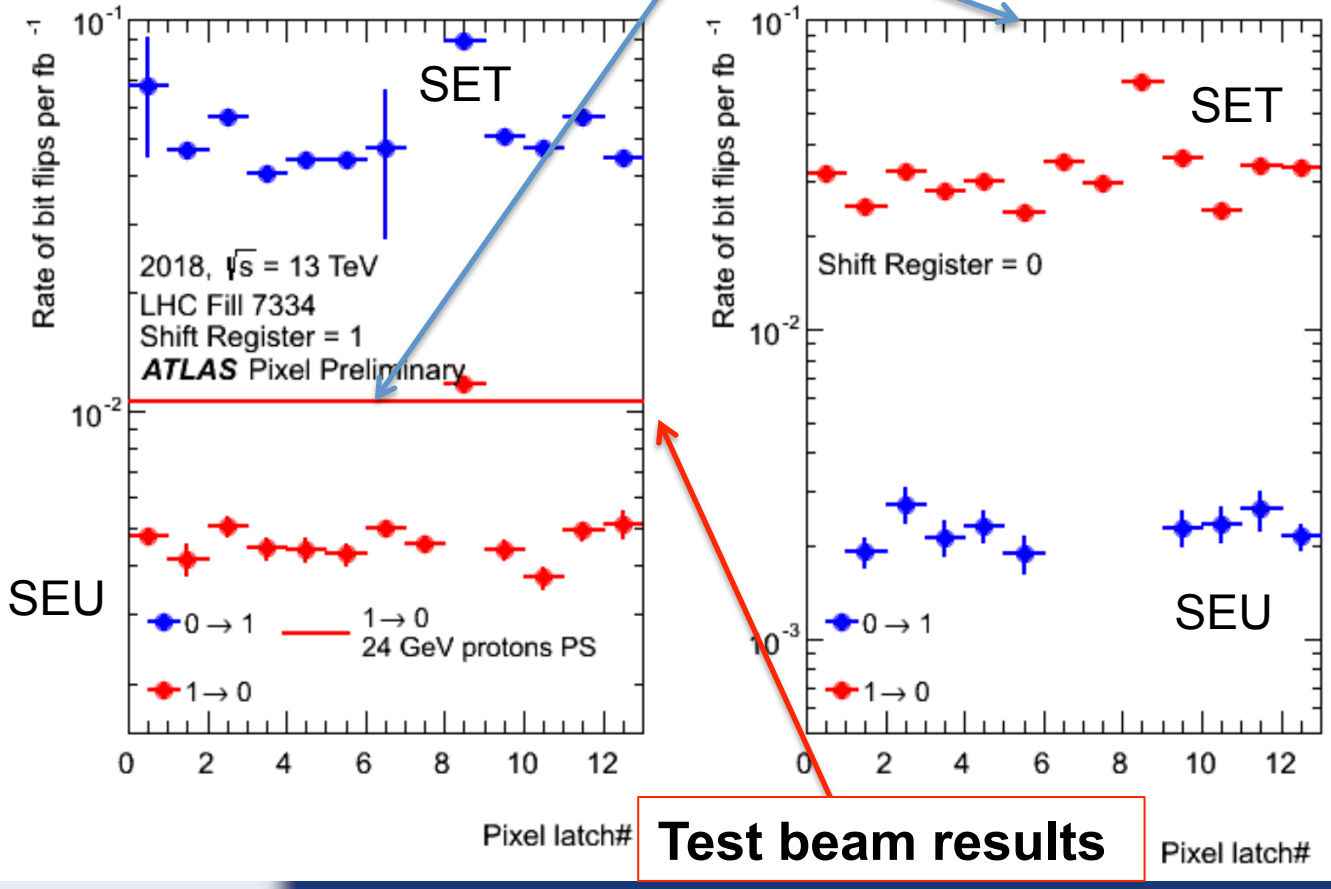
9.2% less collisions at IP1/5 compared to pure BCMS scheme



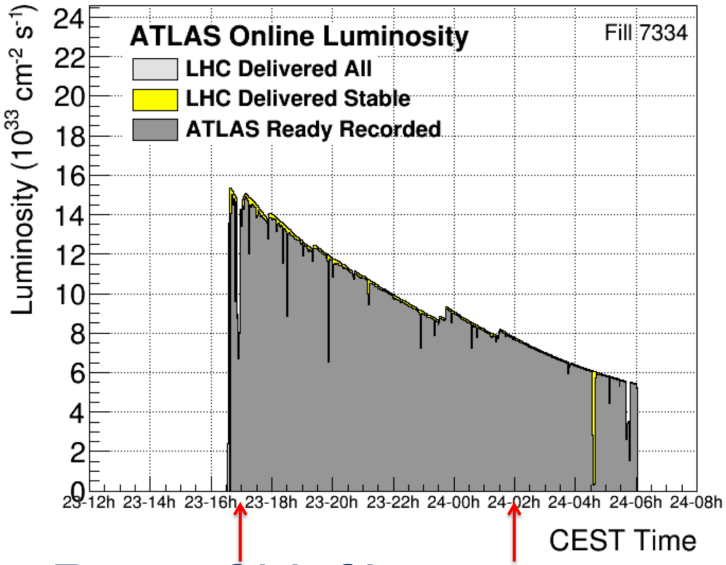
G. Iadarola

Local pixel register read-back

- Similar exercise for local pixel register read-back:
  - only two readings for this test
  - some FE-s loaded with **1** in the shift register
  - some FE-s loaded with **0** in the shift register



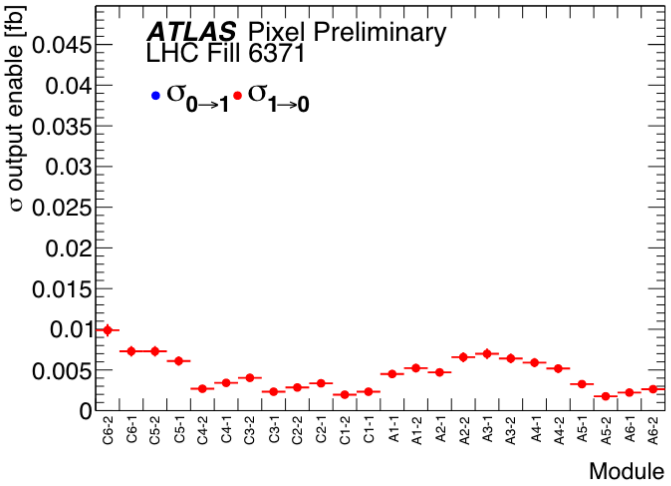
Test beam results

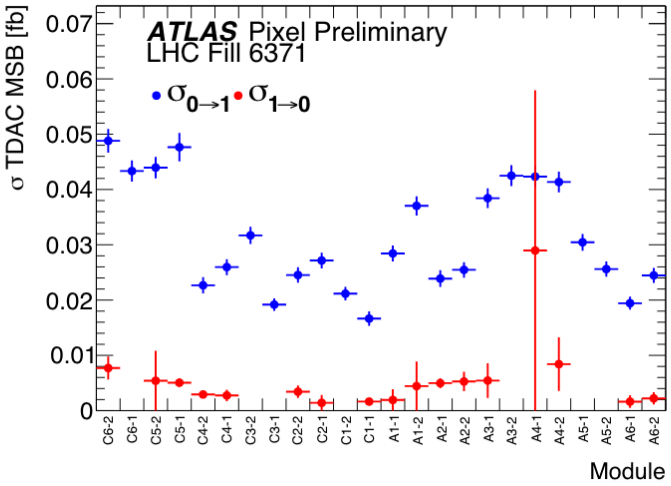


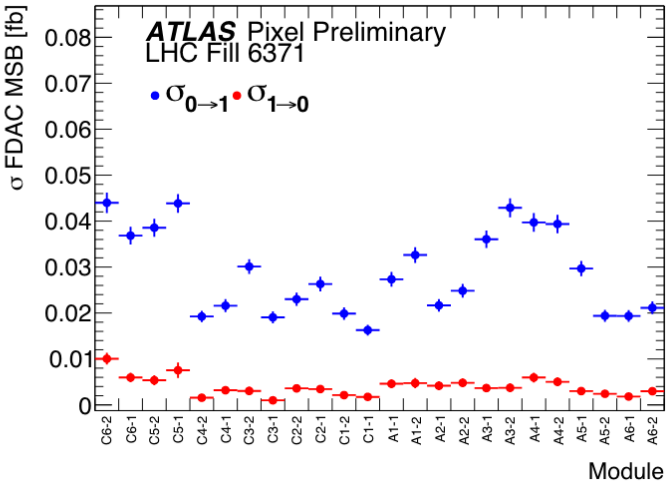
- Rate of bit flips mostly from SET (glitches) on the LOAD lines:
  - SR = **1** : 0→**1**
  - SR = **0** : 1→**0**
- Lower rate due to real memory SEU:
  - SR = **1** : 1→**0**
  - SR = **0** : 0→**1**

Read back results

- Local pixel register read-back at the begin and at the end of a fill (planar modules)





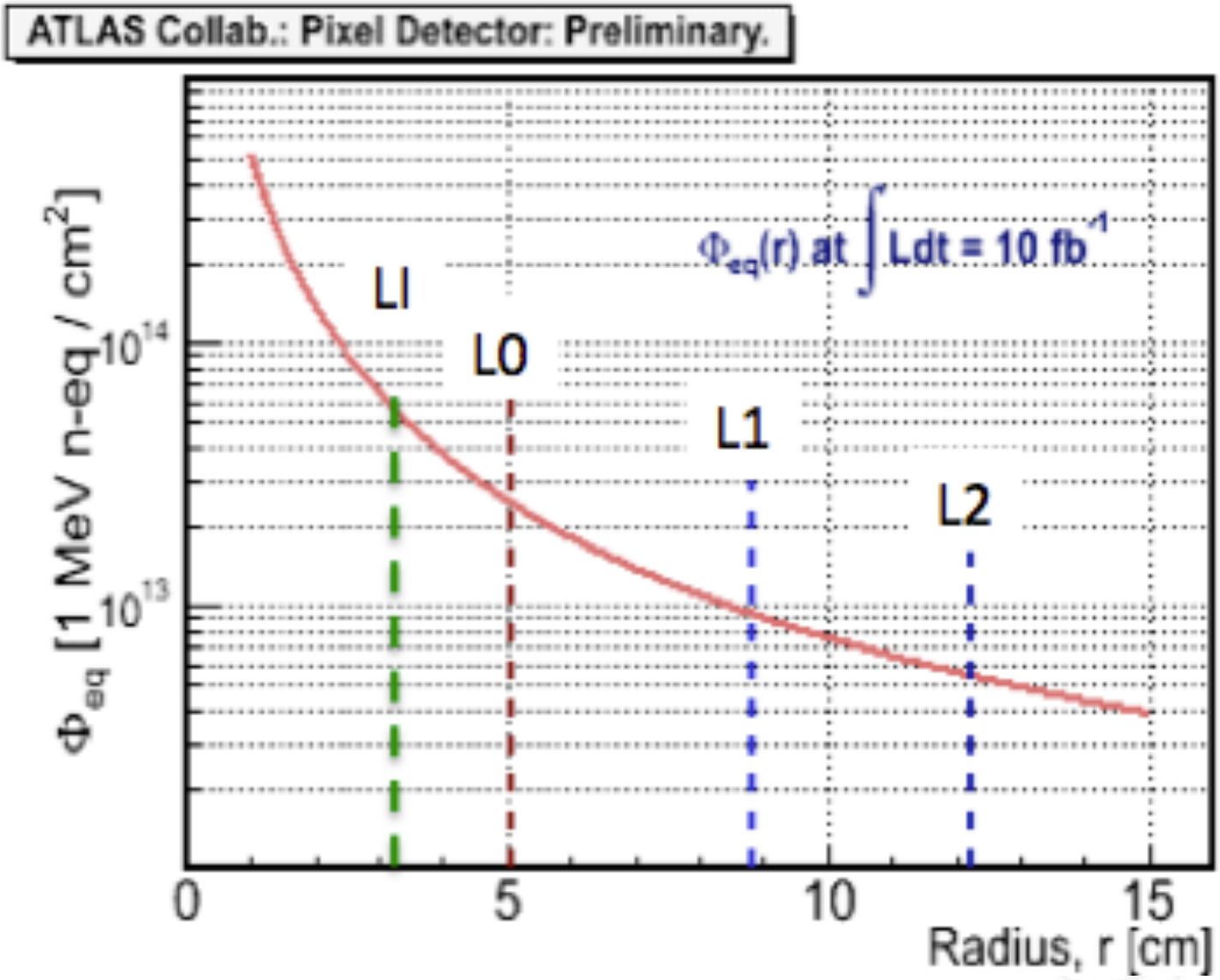


- The cross section for a latch to perform a 0→1 (1→0) flip computed for each planar module FE-I4 for the output **Enable bit**, the **TDAC MSB** and the **FDAC MSB**.

- The cross section is computed by dividing the number of 0s (1s) that are changed into 1s (0s) at the end of the run by the integrated luminosity of LHC Fill 6371 and dividing by the number of initials 0s (1s), under the assumption that the amount of SEUs depends linearly with respect of the accumulated luminosity.

- The 0 → 1 cross section is set to 0 for the output enable because almost all pixels in a sensor have this bit set at 1 and a measurement of such transition is not possible for this latch

Fluence in various layers



Comparisons of FE-I3 vs FE-I4

	FE-I3	FE-I4
Pixel Size	$50 \times 400 \mu m^2$	$50 \times 250 \mu m^2$
Pixel Array	18×160	80×336
Chip Size	$7.6 \times 10.8 mm^2$	$20.0 \times 18.6 mm^2$
Active Fraction	74%	89%
Analog Current	$16 \mu A$/pixel	$10 \mu A$/pixel
Digital Current	$10 \mu A$/pixel	$10 \mu A$/pixel
Analog Supply Voltage	1.6V	1.5V
Digital Supply Voltage	2.0V	1.2V
Data Rate	40Mb/s	160Mb/s

Item	Value	Units
Pixel size	50×250	μm^2
Bump pad opening diameter	12	μm
Input	DC-coupled -ve polarity	
Maximum charge	100,000	e^-
DC leakage current tolerance	100	nA
Pixel array size	80×336	Col $\times$ Row
Last bump to physical chip edge on 3 sides	≤ 100	μm
Last bump to physical edge on bottom	≤ 2.0	mm
Normal pixel input capacitance range	100-500	fF
Edge pixels input capacitance range	150-700	fF
In-time threshold with 20 ns gate (400 pF)[1]	≤ 4000	e^-
Hit-trigger association resolution	25	ns
Same pixel two-hit discrimination (time)	400	ns
Single channel ENC sigma (400 fF)	< 300	e^-
Tuned threshold dispersion	< 100	e^-
Charge resolution	4	bits
ADC method	ToT	
Radiation tolerance (specs met at this dose)	300	Mrad
Operating temperature range	-40 to $+60$	°C
Average hit rate with $< 1\%$ data loss	400	MHz/cm^2
Readout initiation	Trigger command	
Max. number of consecutive triggers	16	
Trigger latency (max)	6.4	μs
Maximum sustained trigger rate	200	kHz
External clock input (nominal)[2]	40	MHz
Single serial command input (nominal)[2]	40	Mb/s
Single serial data output (nominal)[2]	160	Mb/s
Output data encoding	8b/10b	
I/O signals	LVDS	

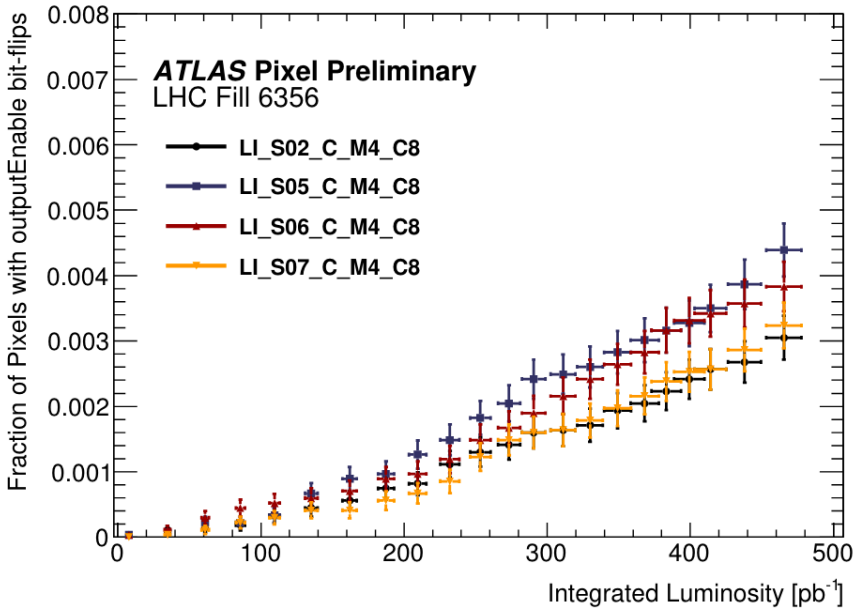
1: At discriminator output. Digital hit detection in region will reduce sensitivity to time-walk.

2: Nominal operating frequencies. The design includes 20% frequency margin in general and $\approx$100% for the data output.

Test beam results

- Beam testing in 2012 before the installation of IBL (24 GeV proton beam at CERN)
- Chip under test is perpendicularly held to the radiation beam:
  1. Disable all pixels (Set Enable bit = 0)
  2. Inject beam (flip 0➔1 happening…)
  3. Count firing pixels (count Enable bit=1)

➔ SEU cross section measured by beam testing **$1.1 \cdot 10^{-15}$ cm^2**



Shown for four different FE-I4 front ends placed on various IBL 3D modules as a function of the integrated luminosity of the fill.

The horizontal error bars are obtained by applying 2.4% systematic uncertainty on the integrated luminosity measurement, while the vertical bar is the statistical error.

The errors are correlated among the points