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Software Design L1: Parallelism in a Modern HEP Data Processing Framework

Thursday 19 September 2019 08:45 (1 hour)

Even though the miniaturization of transistors on chips continues like predicted by Moore's law, computer hardware starts to face scaling issues, so-called performance 'walls'. Probably, the best known is the 'power wall', which limits clock frequencies. Amongst others, a way of increasing processor performance remains now to integrate many cores in the same chip. At the same time, the upcoming LHC upgrade will increase the required CPU power drastically. Both problems challenge the current way of software design in high energy physics (HEP). Developers in high energy physics are forced to re-think their ways of software design and need to move to massively parallel applications. This lecture will explain the current HEP software design, the hardware and physics issues that need to be tackled, and possible approaches to achieve the required level of parallelization.

Summary

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