How to do ultrafast Deep Neural Network inference on FPGAs

Report of Contributions

https://indico.cern.ch/e/FPGA4HEP

Contribution ID: **1** Type: **not specified**

What is HLS4ML?

Wednesday, 6 February 2019 09:15 (1h 15m)

An introduction to the HLS4ML framework

Presenter: NGADIUBA, Jennifer (CERN)

Contribution ID: **2** Type: **not specified**

Optimize FPGA design: quantization and parallelization with HLS4ML

Wednesday, 6 February 2019 13:30 (1 hour)

Presenter: NGADIUBA, Jennifer (CERN)

Contribution ID: **3** Type: **not specified**

Model acceleration on cloud FPGAs

Wednesday, 6 February 2019 16:00 (1 hour)

Presenter: NGADIUBA, Jennifer (CERN)

Contribution ID: **4** Type: **not specified**

Firmware implementation with SDAccel

Wednesday, 6 February 2019 11:00 (1 hour)

Export HLS design to firmware with Xilinx SDAccel on Amazon cloud.

Contribution ID: **5** Type: **not specified**

Welcome

Wednesday, 6 February 2019 09:00 (15 minutes)

Presenter: AARRESTAD, Thea (Universitaet Zuerich (CH))

Contribution ID: **6** Type: **not specified**

Registration

Wednesday, 6 February 2019 08:30 (30 minutes)

Contribution ID: **7** Type: **not specified**

Optimize FPGA design: model compression

Wednesday, 6 February 2019 14:30 (1 hour)