14.4. Readout systems for innovative calorimeters

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WP 14.4

January 10, 2019

- **Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors**

Milestone 58: Definition of optical and electrical coupling of readout, interface functionality and DIF design

Verification: DIF data sheets
Date: Months 24, delivered

MS58	Definition of optical and electrical coupling of readout, interface functionality and DIF design	14	M24	13/04/2017	Achieved	Report (http://cds.cern.ch/record/2259907)

describes status for AHCAL DIF (produced), SDHCAL DIF (in design) and SiECAL DIF (aim for 2018)

Test bench for ASIC tests (no deliverable/milestone)

Description of subtask 14.4.2: "This activity includes test benches for front-end ASICs of highly granular calorimeters as e.g. those developed in WP4. The test bench is a prototype for mass tests for LC Experiments capable to serve experiments with similar front-end electronics."

Status: testboard for AHCAL ASIC (SPIROC2E) in BGA package built, has been used for the "mass testing" for the ASICs for the next large prototype (~600 ASICs)

Deliverable 14.5: Common running of calorimeter prototypes

Deliverable: Data acquisition system to allow for a common data taking of different highly granular calorimeter prototypes in beam tests at CERN and DESY. These tests should provide data files containing events synchronised between the subsystems.

Date: Month 36

Status: done (see talk by Katja)

D14.5	Common running of calorimeter prototypes	WP14	M36	18/05/2018	Achieved	Report

Deliverable 14.6: Adaptation of readout system for operation in compact LC detectors

Date: Month 44

Status: Document delivered 19/12/2018 received minor comments (most already adressed)

SiECAL

- talk by Jimmy Jeglot

AHCAL DIF:

- space constraints less stringent than for ECAL
- current generation of interfaces already designed with limited space in mind
- no further optimisation planned at the moment

SDHCAL DIF

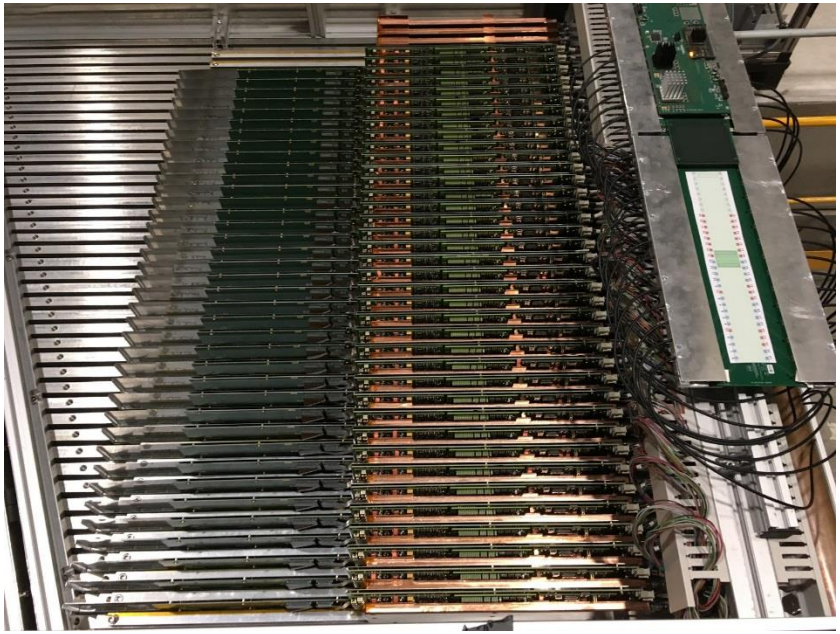
- provided by Mary-Cruz and Imad

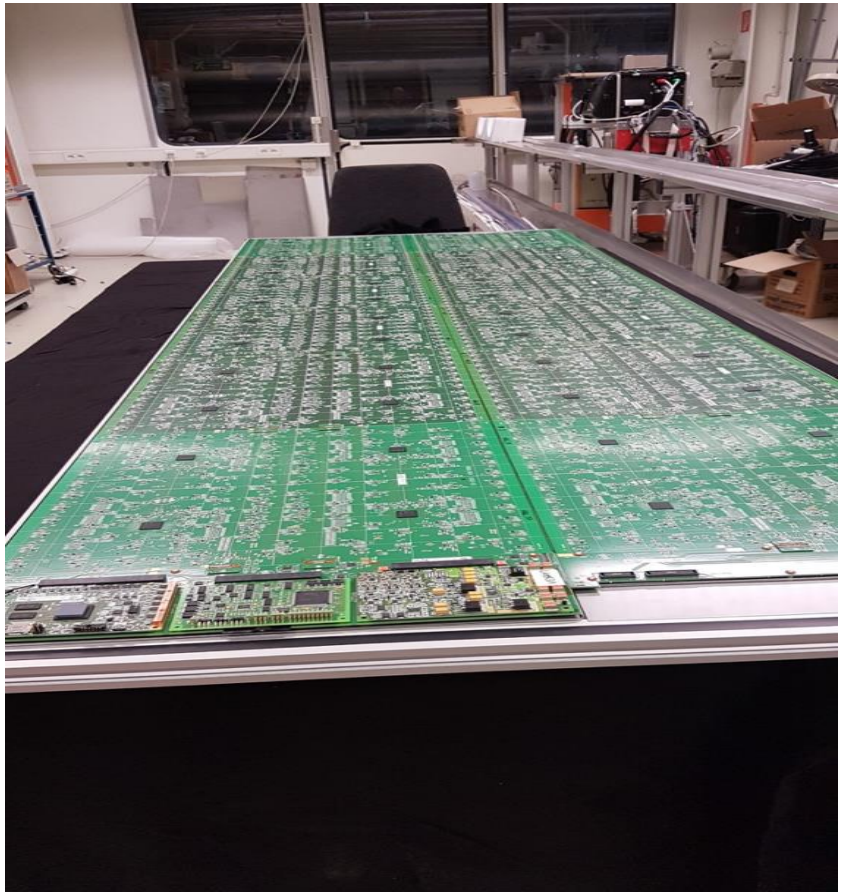
AHCAL DIF: Use in Beam and Lab tests

50 DIFs produced and used:

- **39 layers of the large AHCAL technological prototype (2*2 HBUs, several beam periods in 2018)**
- **large layer: 2*6 HBUs (ongoing, full size is 3*6 HBUs)**

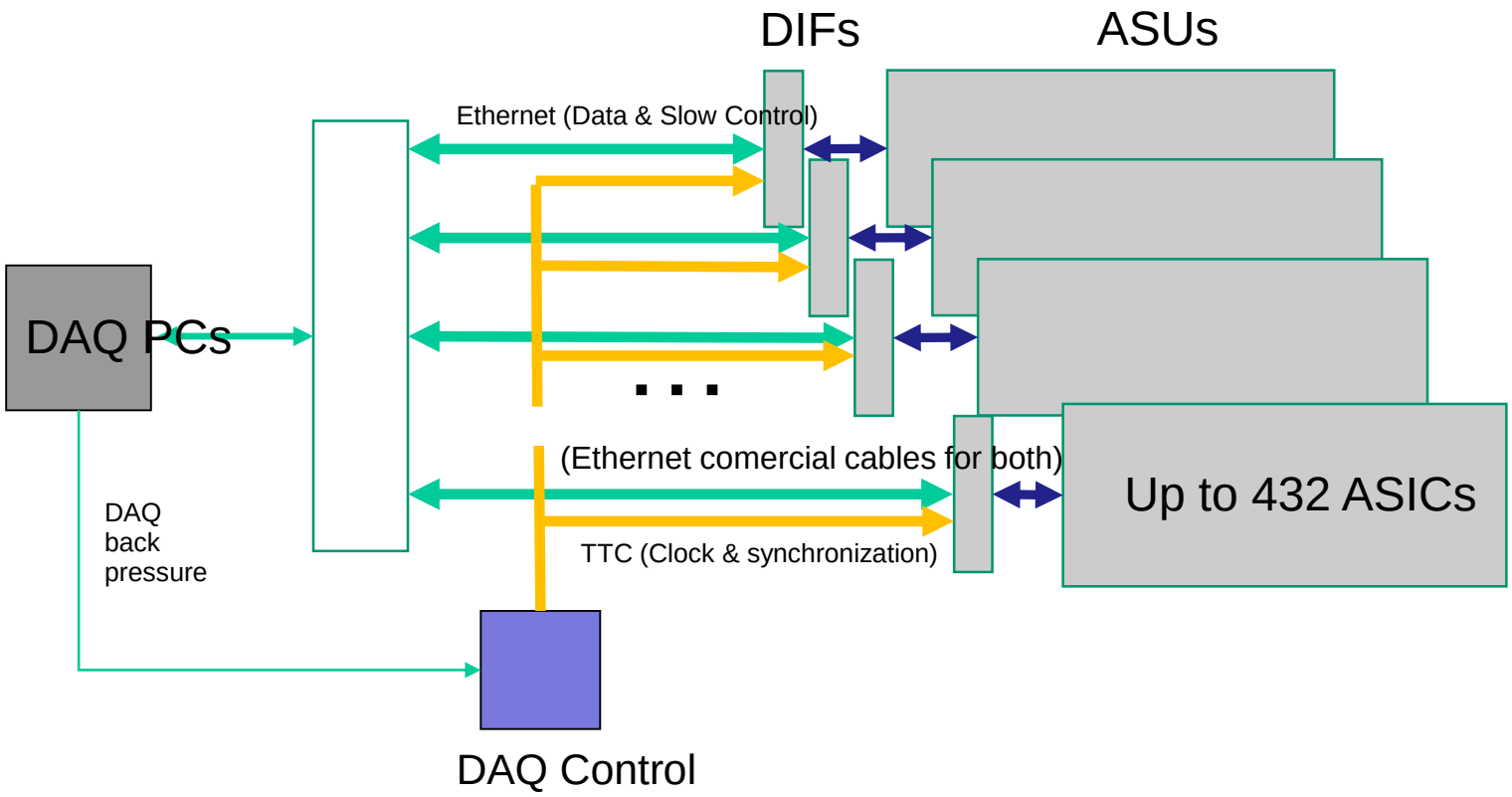
Reliable operation, fulfilling requirements

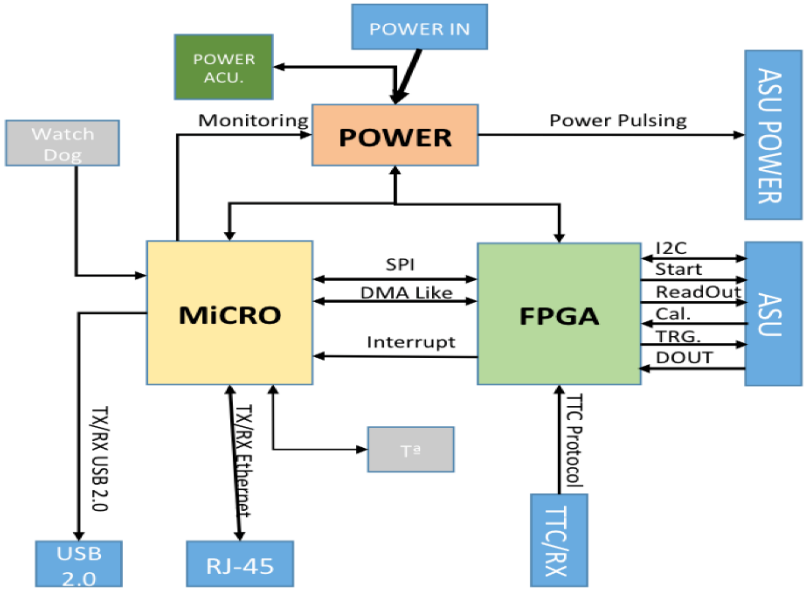




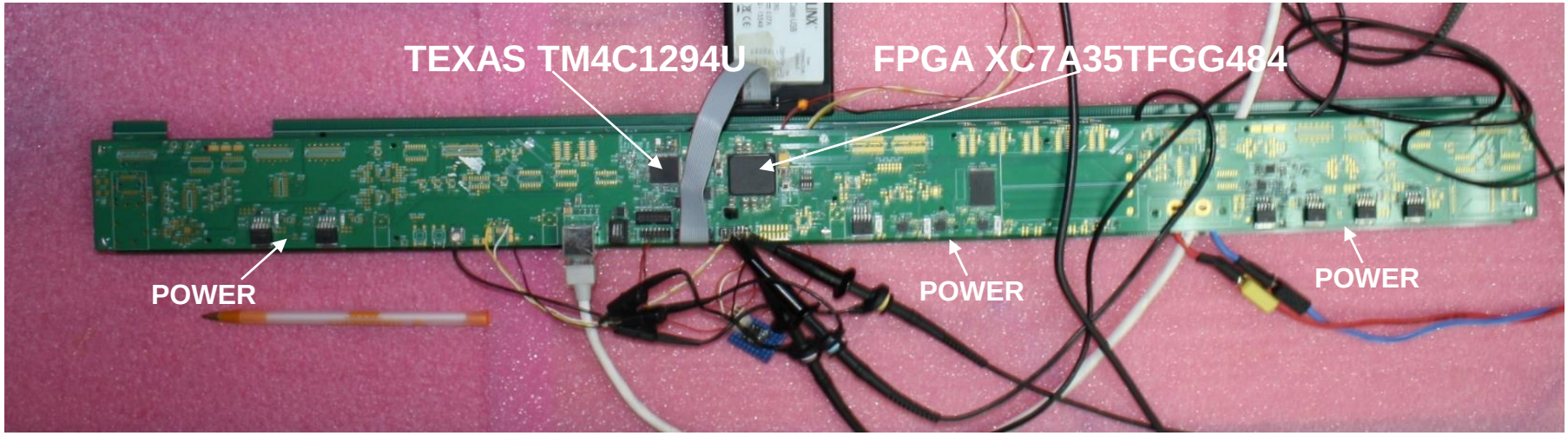
DIF sends DAQ commands (config, clock, trigger) to front-end and transfer their signal data to DAQ. It controls also the ASIC power pulsing

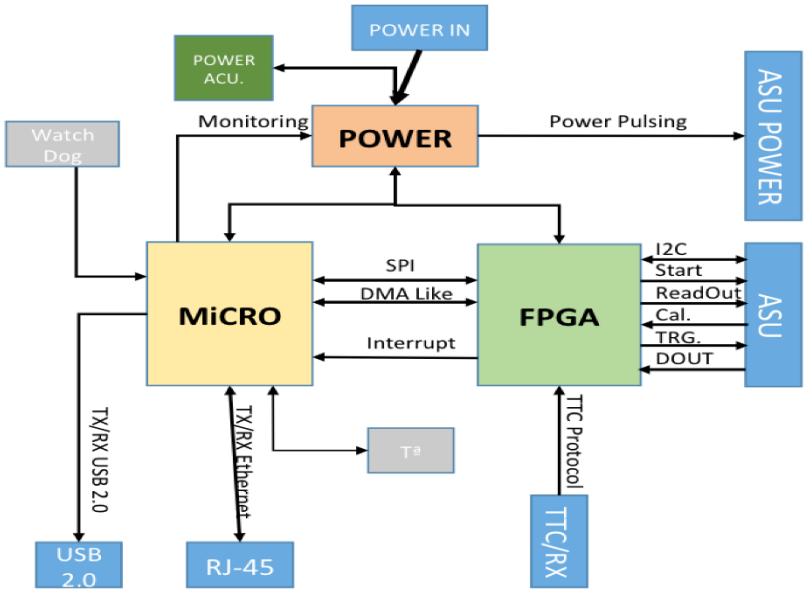
New SDHCAL DIF : capable to deal with up to 432 ASICs while having a size compatible with ILD size requirements. It has standard Ethernet bus (data & slow control) and TTC (clock & synchronization) link with possibility of GBT link.





- Only **one DIF per plane** (instead of **three**)
- DIF handle up to **432 HR3 chips** (vs **48 HR2** in previous DIF)
- HR3 **slow control** through **I2C bus (12 IC2 buses).** Keeps also **2 of the old slow control buses as backup & redundancy**.
- **Data transmission to/from DAQ** by **Ethernet**
- **Clock and synchronization** by **TTC** (already used in LHC)
- **93W Peak power supply** with super-capacitors (vs **8.6 W** in previous DIF)
- Spare I/O connectors to the FPGA (i.e. for GBT links)
- Upgrade **USB 1.1** to **USB 2.0**





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DIF Firmware was developed and it is currently tested on several connected large SDHCAL slabs