Karlsruhe Institute of Technology

HELMHOLTZ
RESEARCH FOR GRAND CHALLENGES

A novel centralized slow control and board management solution for ATCA blades based on the Zynq Ultrascale+ System-on-Chip

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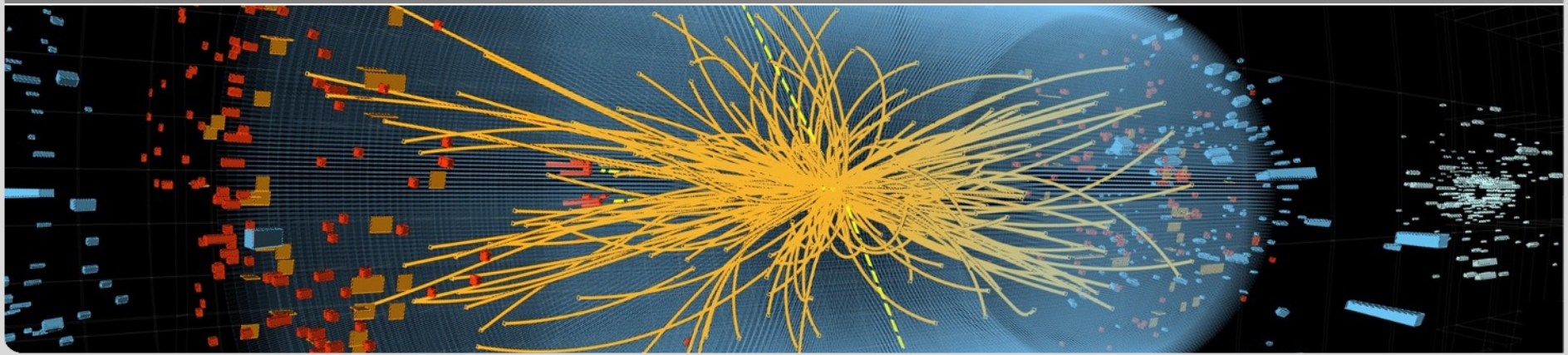
Helmholtz Research Field Matter



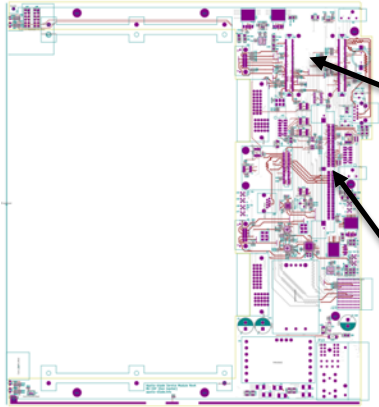
Context & motivation

Observations

- DAQ boards become increasingly complex (# and speed of links, processing power)
- More management tasks to perform (slow control, calibration, commissioning)
- Adding processor modules is a trend (to cope with these tasks)

Examples (CMS L1 track trigger dev boards)

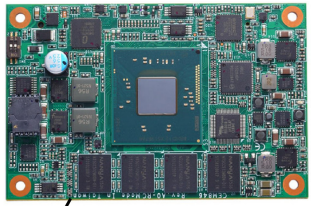
Apollo



Enclustra ZX1 SoC

CERN-IPMC

Boston University, Cornell University

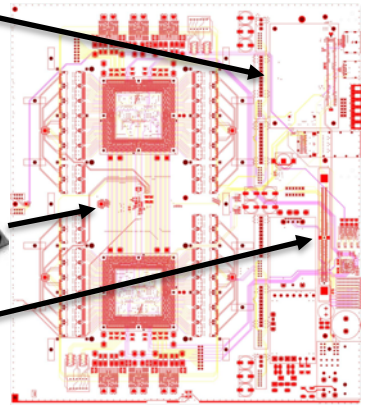


X86 based COMexpress

Service
FPGA

CERN-IPMC

Serenity



Imperial College London

See also L1 Track Finding talk Thu 11:15 - https://indi.to/8bDv2

Integrated platform management approach

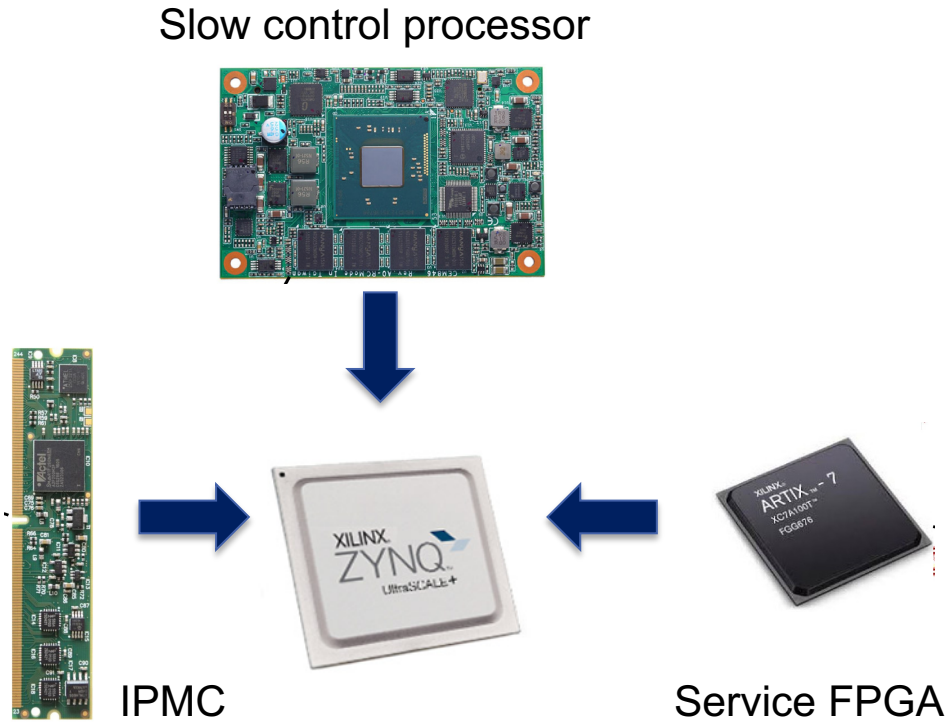
Typical components

- IPMC (ATCA board management)
- CPU module (slow control)
- Service FPGA (glue logic)

Isn’t one single component for all management tasks enough?

Possible solution Xilinx Zynq US+

- Higher Integration (safe space)
- More (SW driven) flexibility
- But: higher complexity in single device



Xilinx Zynq Ultrascale+ as control module

Zynq Ultrascale+ MPSoC

- 2 processor domains (APU and real-time)
- FPGA
- Plethora of integrated peripherals
  (PCIe, Eth, I2C, UART, USB, …)
- **Various power domains → partial power-up**

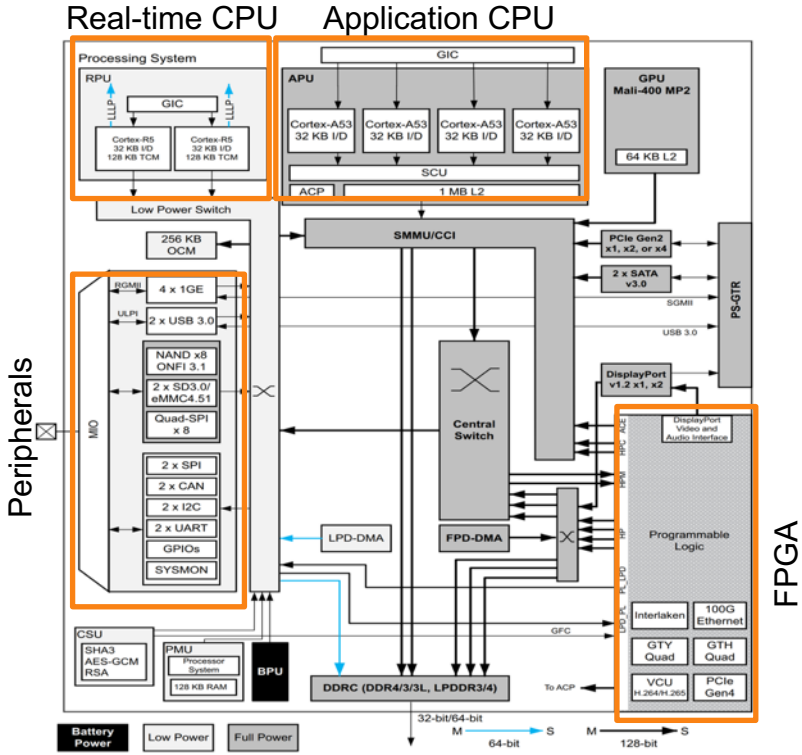


Figure 2-1: **Zynq UltraScale+ MPSoC Device Hardware Architecture**

Xilinx Zynq Ultrascale+ as control module

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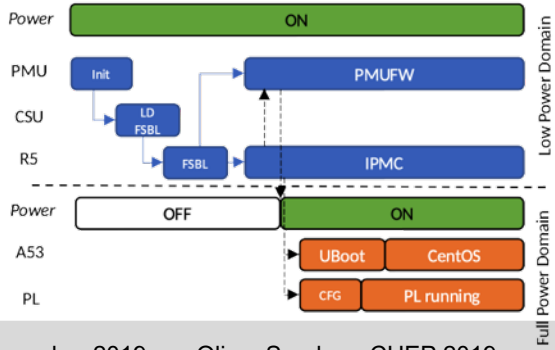
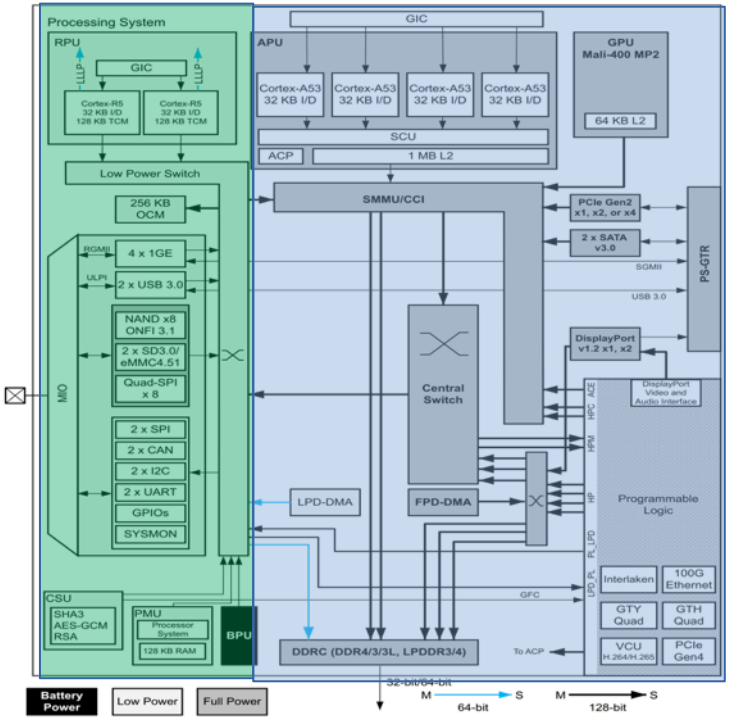
Partitioning

- LPD: IPMC (standalone/RTOS) on ARM-R5, TCM
- FPD: Slow Control (Linux) on ARM-A53 quad cores
- FPGA for services with HW support





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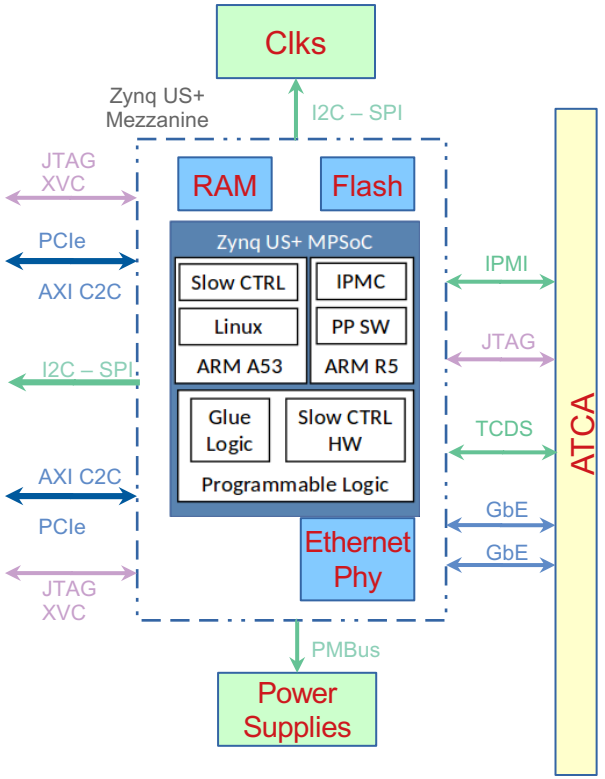
Interfaces

- Xilinx Virtual Cable JTAG
- Link to main FPGA(s) via
  PL-MGTs (PCIe or AXI C2C)
- I2C-SPI to configure board components
- PMBus for Power Supplies
- Eth and I2C backplane connection



Proof of principle – hardware

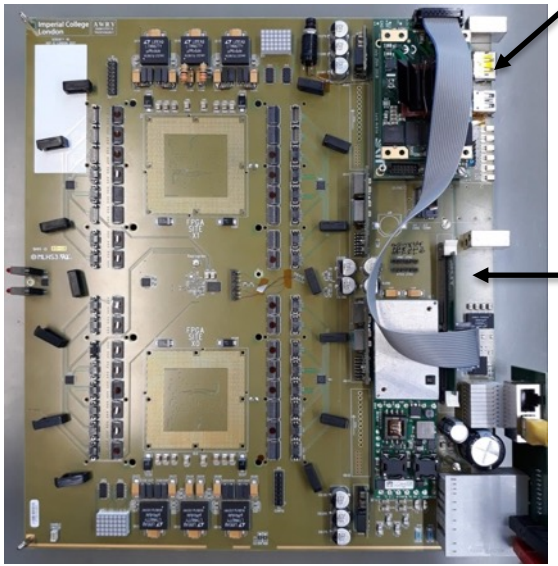
- Based on Serenity (Imperial College)

Hardware

- Trenz Elektronik TE0803 Module (Zynq US+ 4eg)
- Trenz Adapter
  - Interface Trenz to COM Express
  - Additional IPMC features (I2C buffers, Eth Phy, EEPROM, SDCard…)
  - Interface to SO-DIMM adapter
- SO-DIMM Adapter
  - access to IPMC backplane signals

Trenz 0803

Trenz Adapter



Serenity

SO-DIMM adapter

Proof of principle – software components

Vivado / firmware

- Custom hardware project (MIOs, AXI C2C & XVC)
- Custom isolation configuration

Platform software (patches)

- PMUFW (power management & error handling)
- First stage boot loader (split of power domains and boot procedure)
- PSU_init (split of power domains)

Xilinx SW does not use power domains

Pigeon Point IPMC software

- Received BMR-ZNQ-VPX with ATCA extensions from PP
- Modifications to ATCA state machine (to boot Linux)
- IPMC configuration to match adapter hardware and Serenity (req. for all IPMCs incl. CERN)

Petalinux

- Device tree modifications (assignment of peripherals to IPMC)

IPMC on Serenity – test results

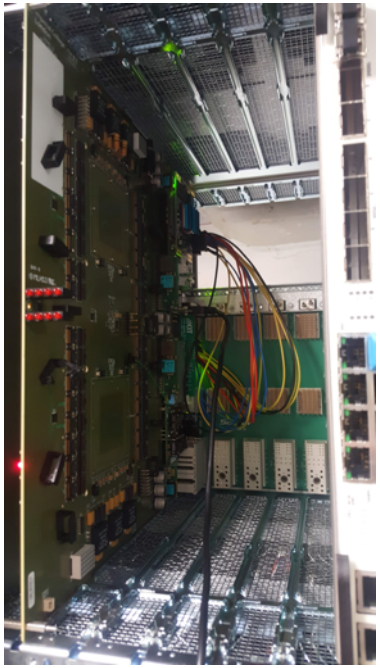
Configuration: Serenity, shelf manager, switch

Following functions verified

- IPMC boot
- Communication with shelf manager
- Board activation/deactivation
- Power-up/power-down sequence
- Reading of IPMC sensor values
- Cold reset
- Initiating boot of Linux
- Coexistence of Linux & IPMC
- JTAG on Linux (XVC)
- …

Limitations

- Zynq US+ powered through 3.3 V standby
  → but it is enough so far (<10 W)
- APU handling not fully integrated into IPMC SW



Example - board activation

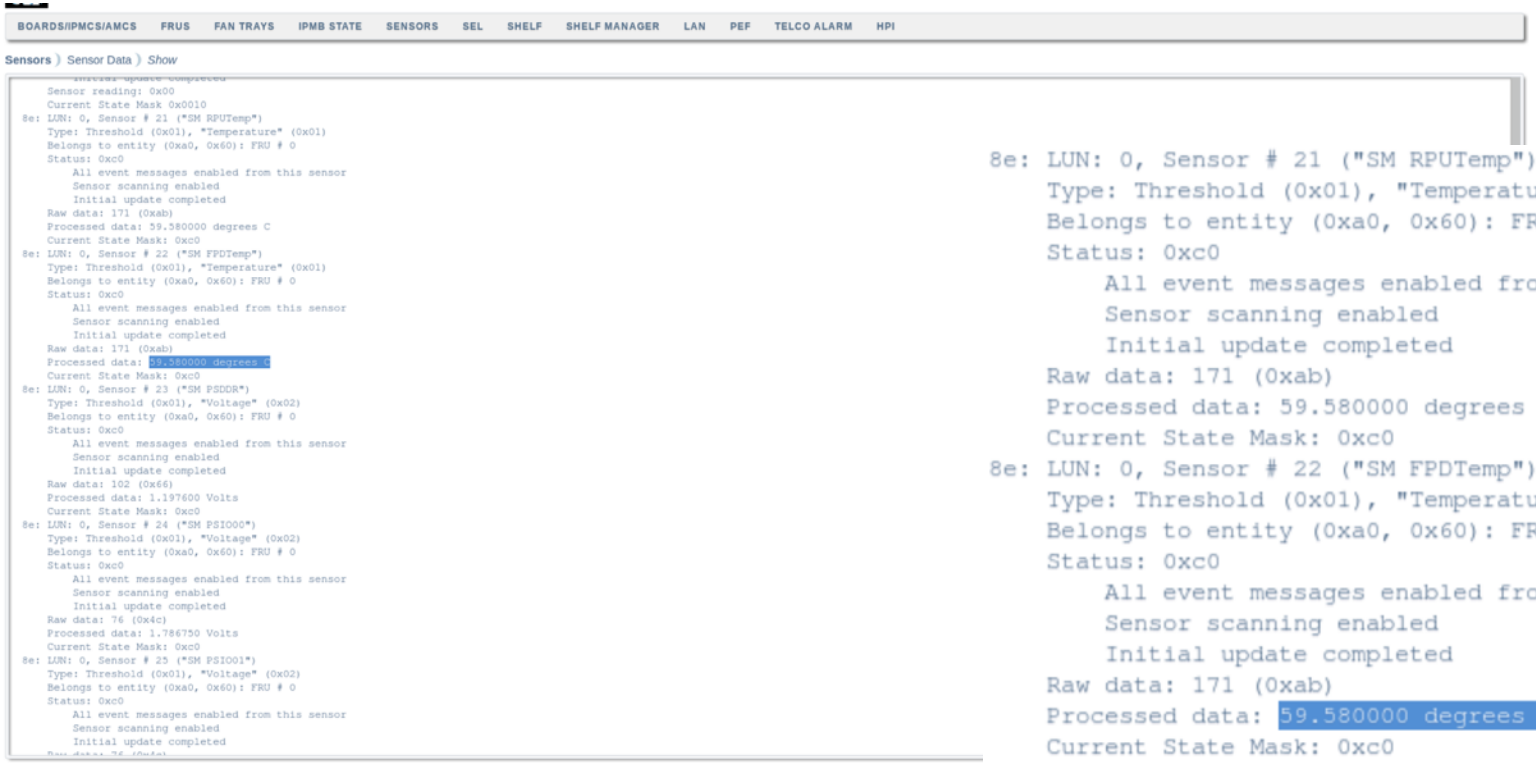
BOARDS/IPMCS/AMCS | FRUS | FAN TRAYS | IPMB STATE | SENSORS | SEL | SHELF | SHELF MANAGER | LAN | PEF | TELCO ALARM | HPI

BOARDs/IPMCs/AMCs ⟩ Board ⟩ *Show*

```
Pigeon Point Shelf Manager Command Line Interpreter

Physical Slot # 7
8e: Entity: (0xa0, 0x60) Maximum FRU device ID: 0x01
    PICMG Version 2.3
    Hot Swap State: M4 (Active), Previous: M3 (Activation In Process), Last State Change Cause: Normal State Change (0x0)
    Device ID: 0x12, Revision: 0, Firmware: 1.08 (ver 1.0.8), IPMI ver 2.0
    Manufacturer ID: 00400a, Product ID: cbda, Auxiliary Rev: 00000000
    Device ID String: "BMR-ZNQ+A2F-ATCA"
    Global Initialization: 0xc, Power State Notification: 0xc, Device Capabilities: 0x2d
    Controller provides Device SDRs
    Supported features: 0x2d
        "Sensor Device" "SEL Device" "FRU Inventory Device" "IPMB Event Generator"
    Links:
    8e: Base Interface (0x00), Channel: 1
        Link: Disabled Ports: 1
    8e: Base Interface (0x00), Channel: 2
        Link: Disabled Ports: 1
    8e: Fabric Interface (0x01), Channel: 1
        Link: Disabled Ports: 1
    8e: Fabric Interface (0x01), Channel: 2
        Link: Disabled Ports: 1
    8e: Update Channel Interface (0x02), Channel: 1
        Link: Disabled Ports: 1

8e: FRU # 0
    Entity: (0xa0, 0x60)
    Hot Swap State: M4 (Active), Previous: M3 (Activation In Process), Last State Change Cause: Normal State Change (0x0)
    Device ID String: "BMR-ZNQ+A2F-ATCA"
    Site Type: 0x00, Site Number: 07
    Current Power Level: 0x01, Maximum Power Level: 0x01, Current Power Allocation: 50.0 Watts

8e: FRU # 1
    Entity: (0xf2, 0x60)
    Hot Swap State: M4 (Active), Previous: M3 (Activation In Process), Last State Change Cause: Normal State Change (0x0)
    Device Type: "FRU Inventory Device behind management controller" (0x10), Modifier 0x0
    Device ID String: "BMR-ZNQ ChassisF"
    Current Power Level: 0x01, Maximum Power Level: 0x01, Current Power Allocation: 0.0 Watts
```

```
8e: FRU # 0
    Entity: (0xa0, 0x60)
    Hot Swap State: M4 (Active), Previous: M3 (Activ
    Device ID String: "BMR-ZNQ+A2F-ATCA"
    Site Type: 0x00, Site Number: 07
    Current Power Level: 0x01, Maximum Power Level:

8e: FRU # 1
    Entity: (0xf2, 0x60)
    Hot Swap State: M4 (Active), Previous: M3 (Activ
    Device Type: "FRU Inventory Device behind manage
    Device ID String: "BMR-ZNQ ChassisF"
    Current Power Level: 0x01, Maximum Power Level:
```

Example - sensor reading




```
8e: LUN: 0, Sensor # 21 ("SM RPUTemp")
    Type: Threshold (0x01), "Temperature" (0x01)
    Belongs to entity (0xa0, 0x60): FRU # 0
    Status: 0xc0
        All event messages enabled from this sensor
        Sensor scanning enabled
        Initial update completed
    Raw data: 171 (0xab)
    Processed data: 59.580000 degrees C
    Current State Mask: 0xc0
8e: LUN: 0, Sensor # 22 ("SM FPDTemp")
    Type: Threshold (0x01), "Temperature" (0x01)
    Belongs to entity (0xa0, 0x60): FRU # 0
    Status: 0xc0
        All event messages enabled from this sensor
        Sensor scanning enabled
        Initial update completed
    Raw data: 171 (0xab)
    Processed data: 59.580000 degrees C
    Current State Mask: 0xc0
```

Next steps towards integrated IPMC

Hardware

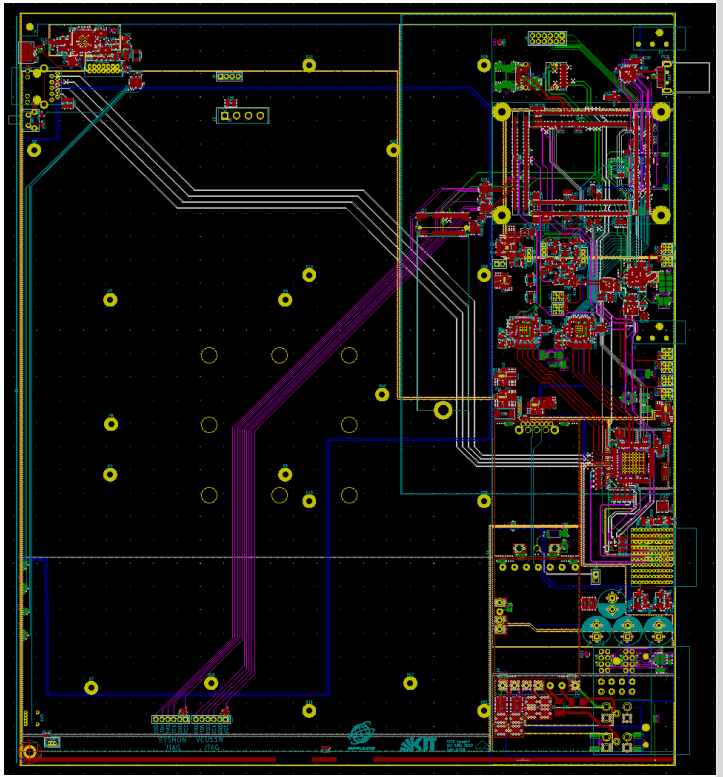
- ATCA-IPMC test board (layout finished)
- ATCA FPGA board - EureKA Maru (layout phase)
- Custom Zynq US+ module (in discussion)

Software & testing

- Add missing IPMC functionality (sensors, handling of FPD, …)
- Continue testing

Lessons learned / observations

- Pigeon Point IPMC software acts nicely on Zynq US+
- Few limitations/modifications for (Peta-)Linux
- Limited Xilinx tool/SW support for domain handling
- Such platform use is not well documented by Xilinx (yet)
- Automation for patches required (Xilinx or custom)



Conclusions

- Realizing all management functionality in a single MPSoC is an exciting solution for next generation boards in the DAQ chain
- Proof of principle successfully built and tested
  (Test at CERN planned week after CHEP)
- However, Xilinx tools lack support for power domains
- Solution for smooth (automatic) integration of IPMC code in a design required