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## The CMS Data Acquisition System for the Phase-2 Upgrade

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The upgraded High Luminosity LHC, after the third Long Shutdown (LS3) will provide an instantaneous luminosity of  $7.5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  (levelled), with a pileup of up to 200 interactions per bunch crossing. During LS3, the CMS Detector will undergo a major upgrade to prepare for the Phase-2 of the LHC physics program, starting around 2026. The upgraded CMS detector will be read out at an unprecedented data rate of up to 50 Tb/s with an event rate of 750 kHz, selected by the level-1 hardware trigger, and an average event size of 7.5 MB. Complete events will be analysed by the High Level Trigger (HLT) using software algorithms running on standard processing nodes, and selected events will be stored permanently at a rate of up to 7.5 kHz for offline processing and analysis. This paper will present, the baseline design of the DAQ and HLT systems for Phase-2, taking into account the projected evolution of high speed network fabrics for event building and distribution, and the anticipated performance of general purpose CPU.

A DAQ and Timing Hub (DTH) board acts as an interface between the synchronous clock-driven domain of the back-end electronics of the sub-detectors and the asynchronous data-driven domain of the commercial networking and processing equipment for the event building and selection.

The design of the DTH in ATCA standard will be outlined and results from measurements with the prototype board will be presented. Firstly, results on distribution of clock, trigger and fast-control data will be shown. Secondly, results on the data flow from aggregating back-end electronics end-points into sub-events and transfer over simplified TCP/IP from the FPGA into multiple 100 Gbps Ethernet network ports and PC hosts will be covered.

### Consider for promotion

Yes

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